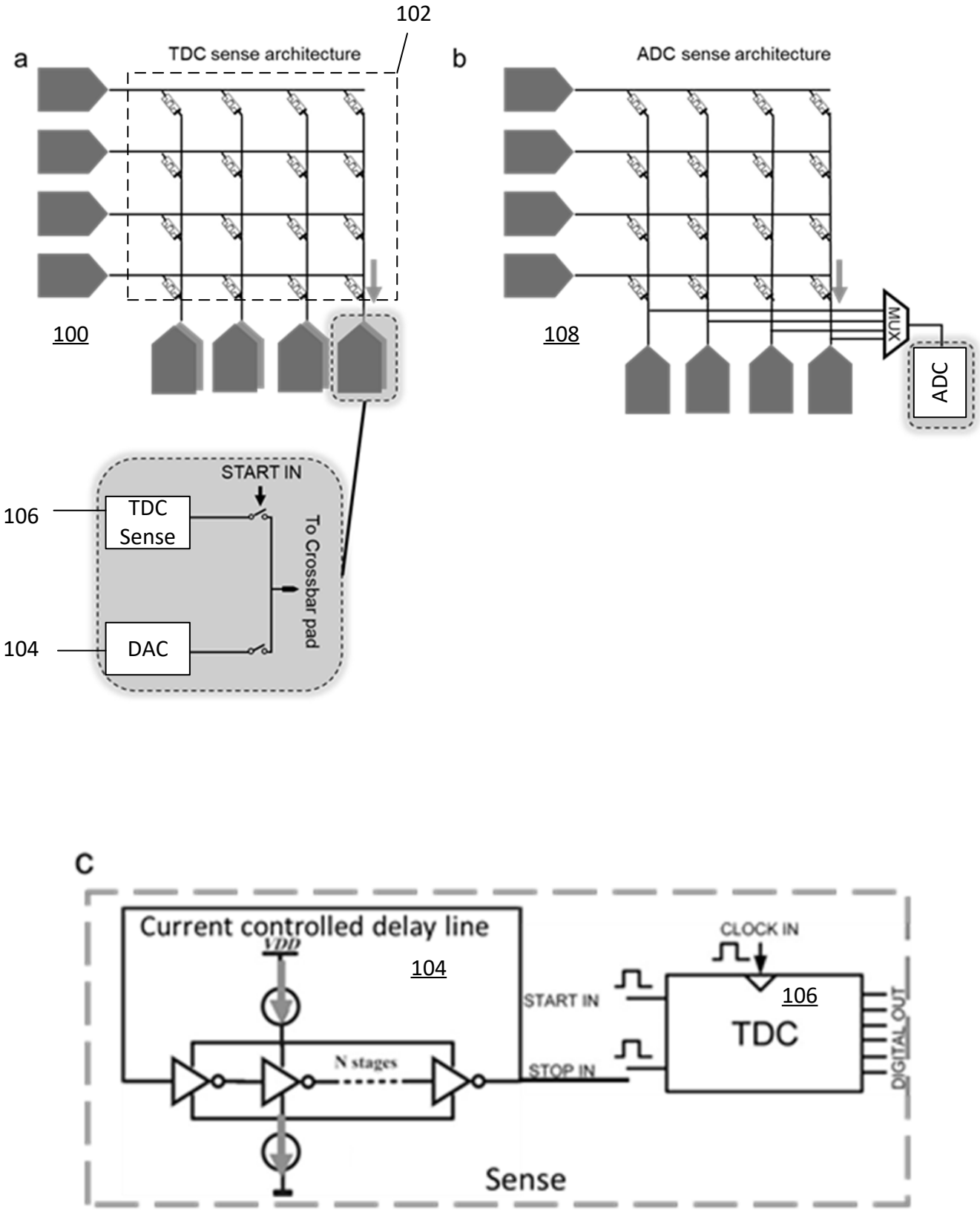

a
TDC sense architecture
102
100
START IN
106
TDC Sense
To Crossbar pad
104
DAC
b
ADC sense architecture
108
MUX
ADC
c
Current controlled delay line
VDD
104
N stages
START IN
STOP IN
CLOCK IN
106
TDC
DIGITAL OUT
Sense

**Figure 1**

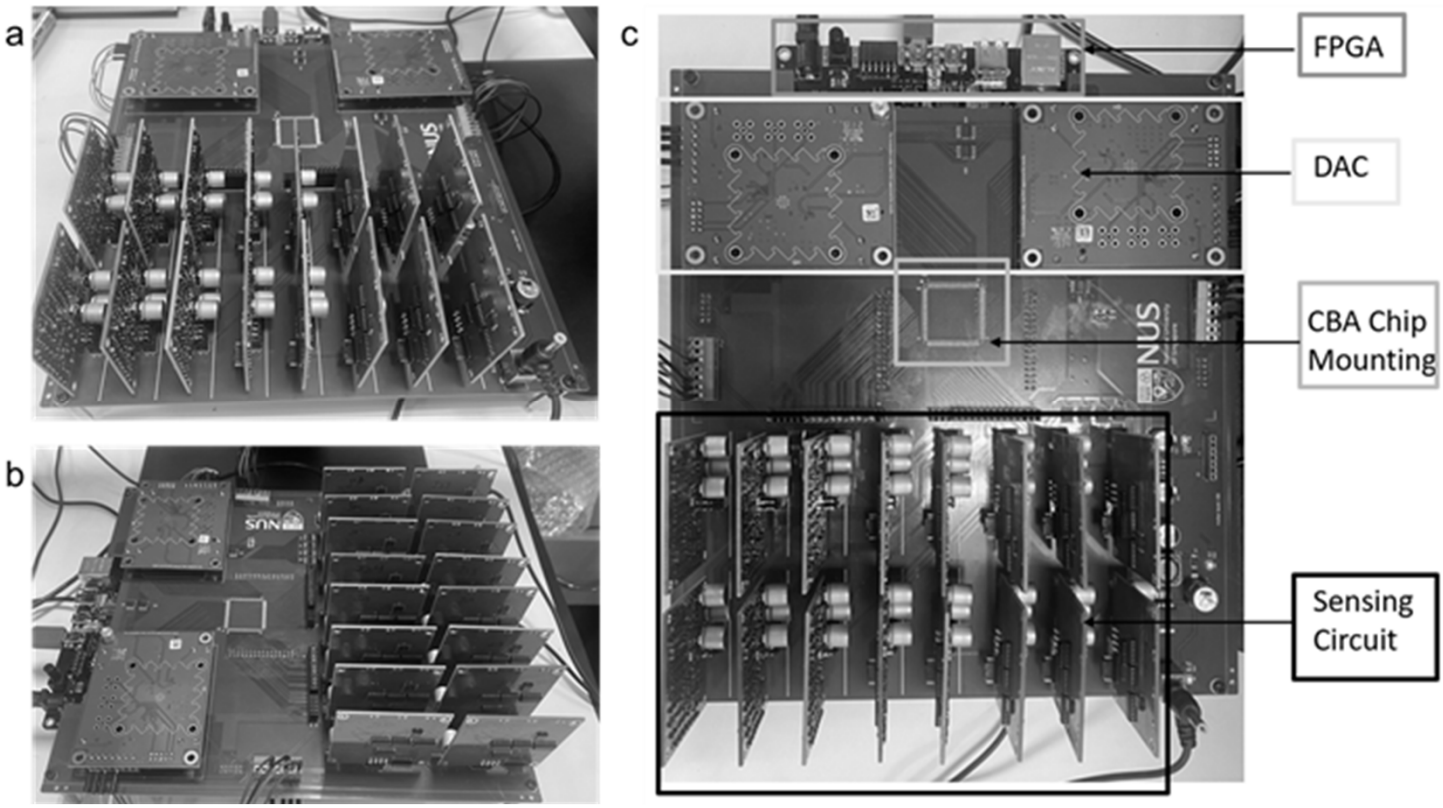
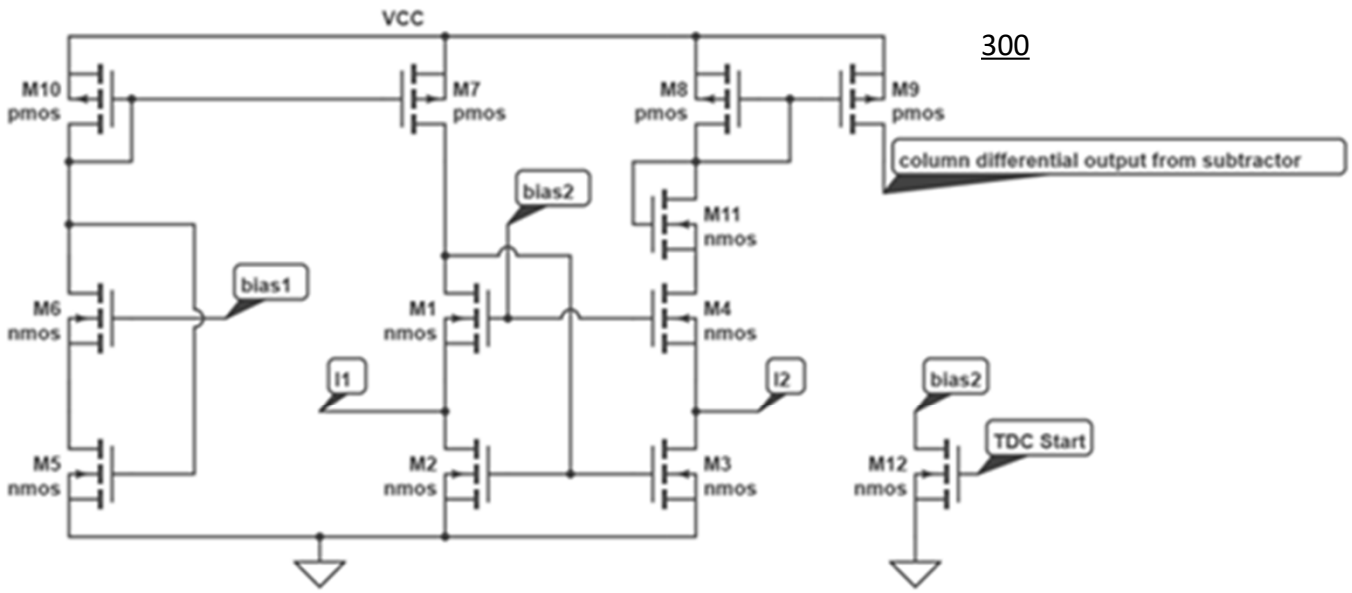
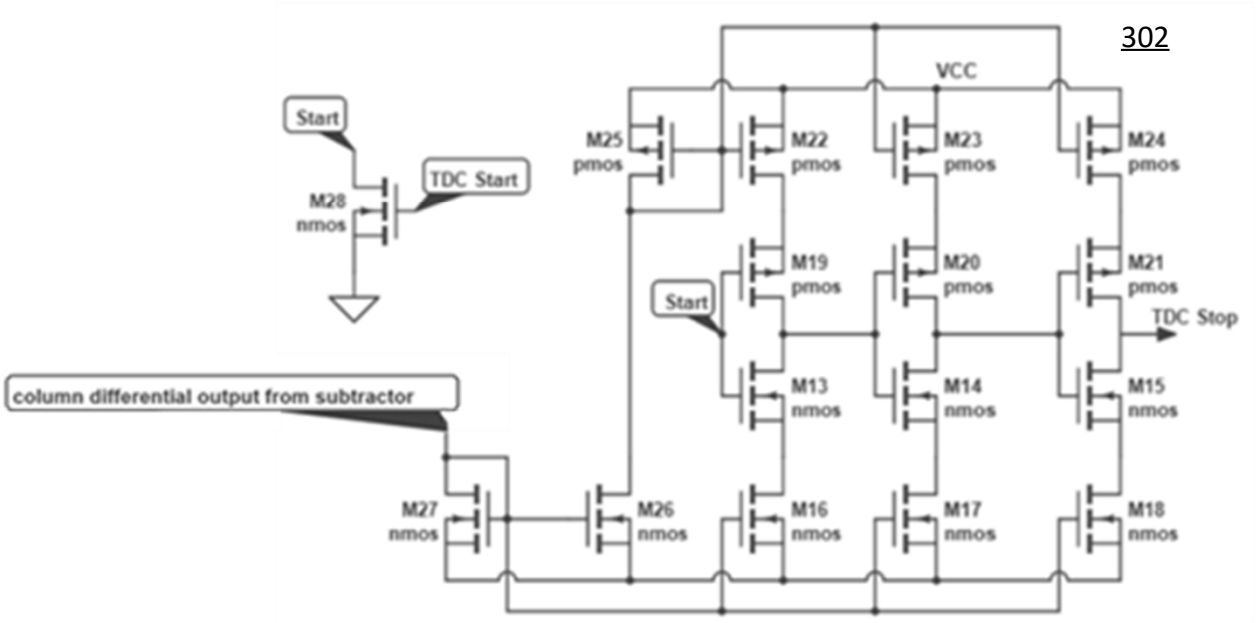



**Figure 2**

a


300
VCC
M10
pmos
M7
pmos
M8
pmos
M9
pmos
column differential output from subtractor
bias2
M11
nmos
bias1
M6
nmos
M1
nmos
M4
nmos
I1
I2
bias2
TDC Start
M5
nmos
M2
nmos
M3
nmos
M12
nmos

b


302
VCC
Start
TDC Start
M28
nmos
M25
pmos
M22
pmos
M23
pmos
M24
pmos
M19
pmos
M20
pmos
M21
pmos
Start
TDC Stop
column differential output from subtractor
M13
nmos
M14
nmos
M15
nmos
M27
nmos
M26
nmos
M16
nmos
M17
nmos
M18
nmos

c

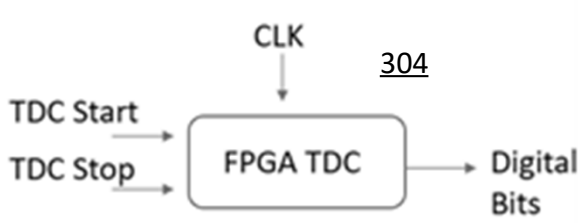

CLK
304
TDC Start
TDC Stop
FPGA TDC
Digital
Bits

**Figure 3**

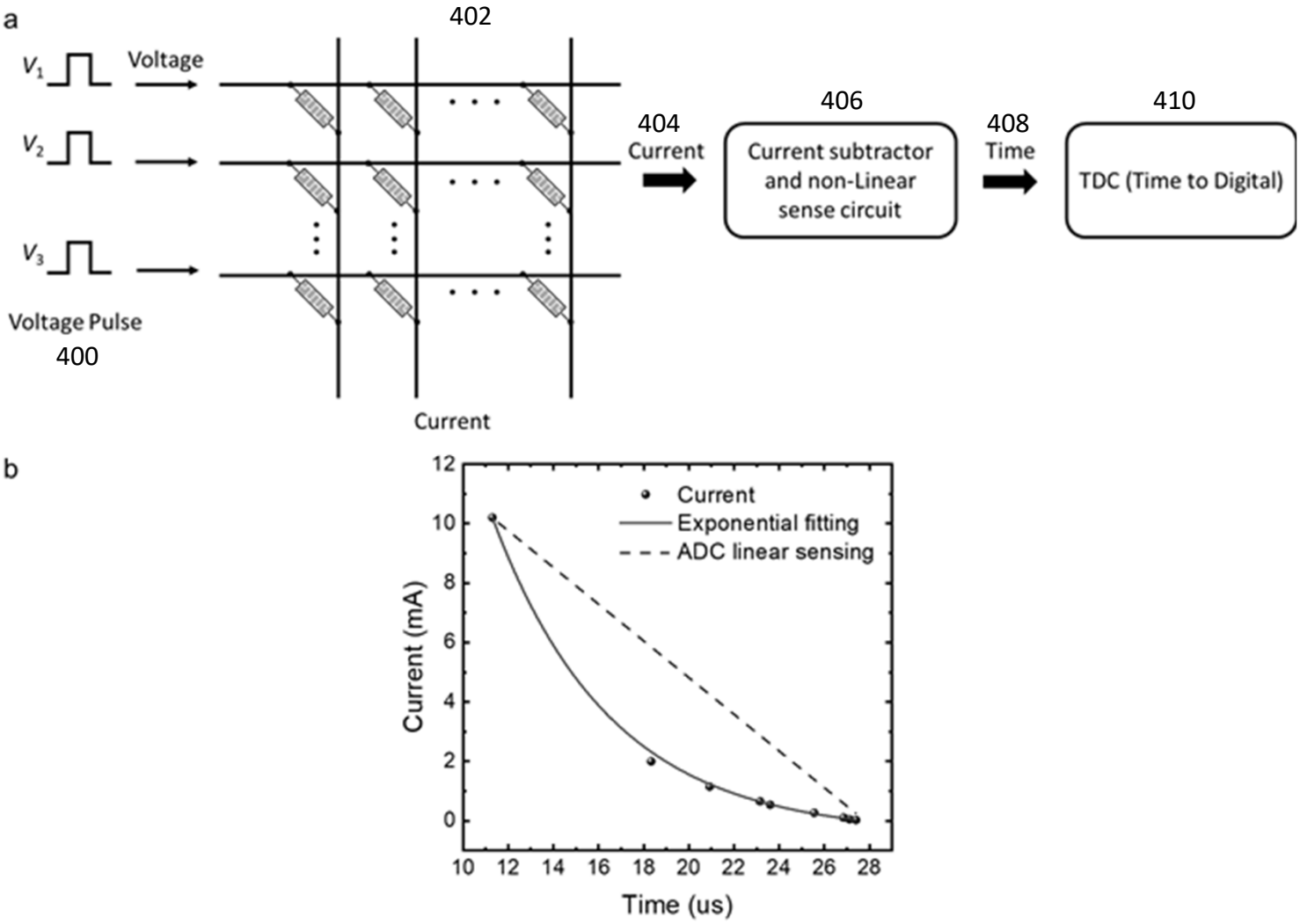
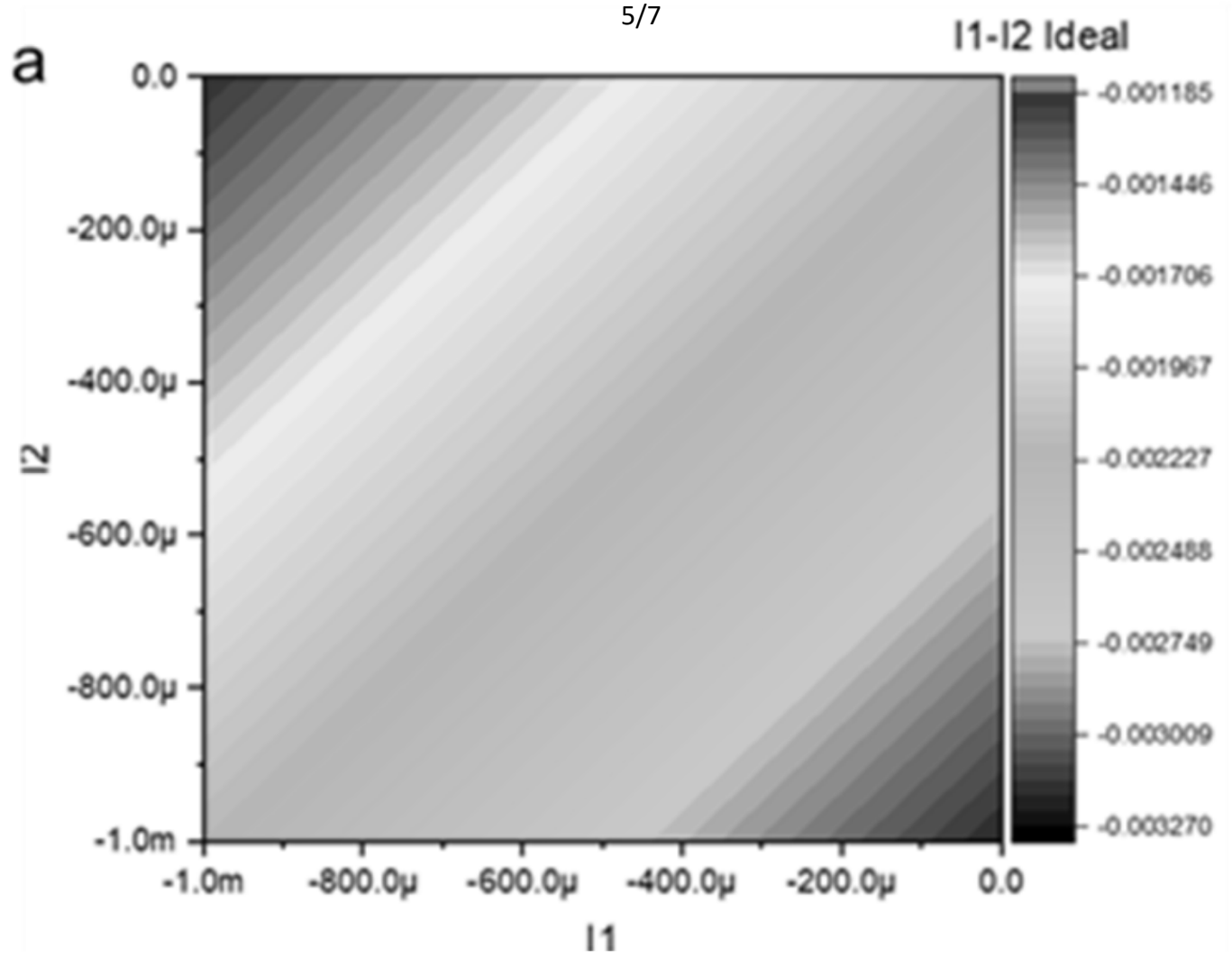
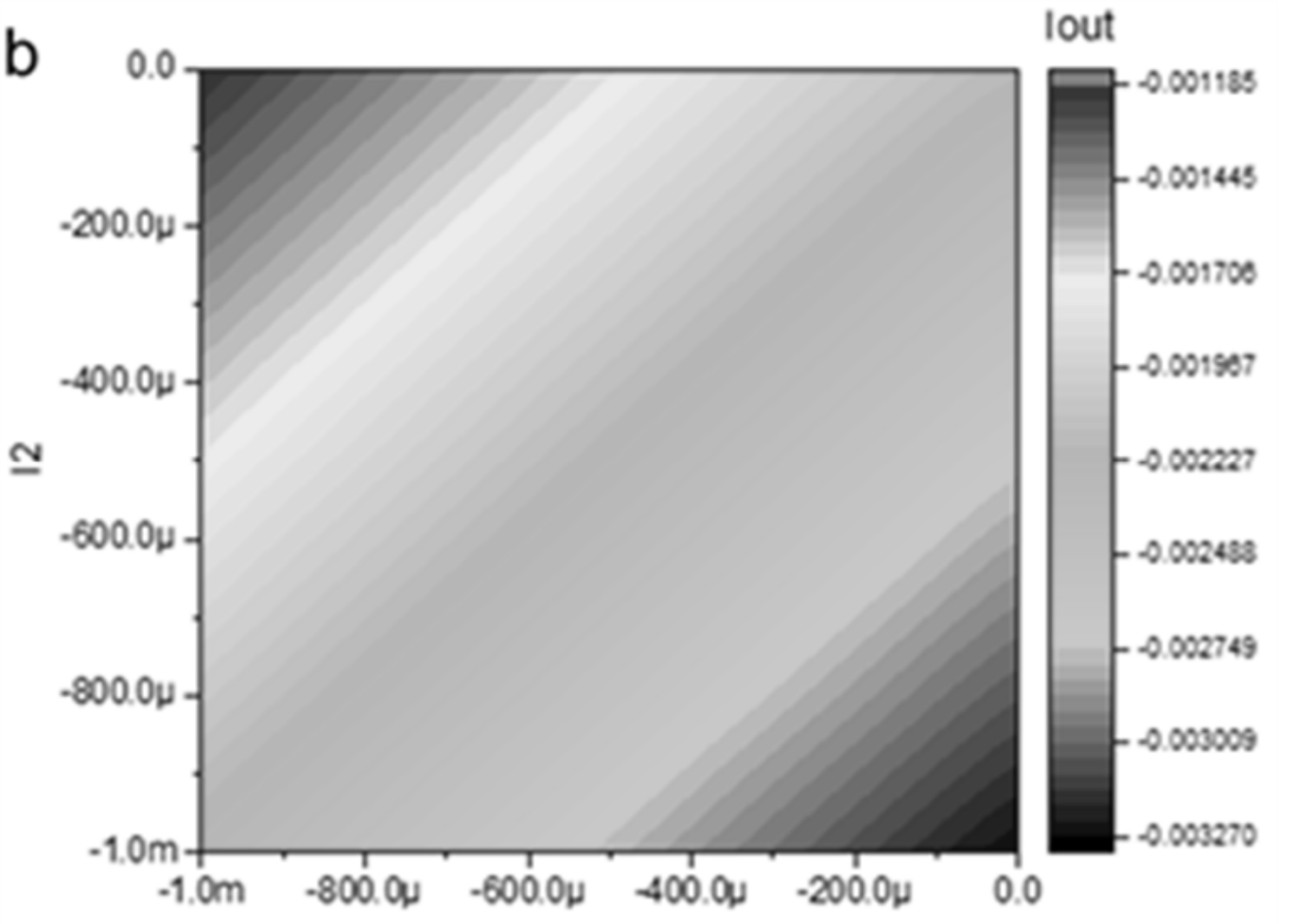
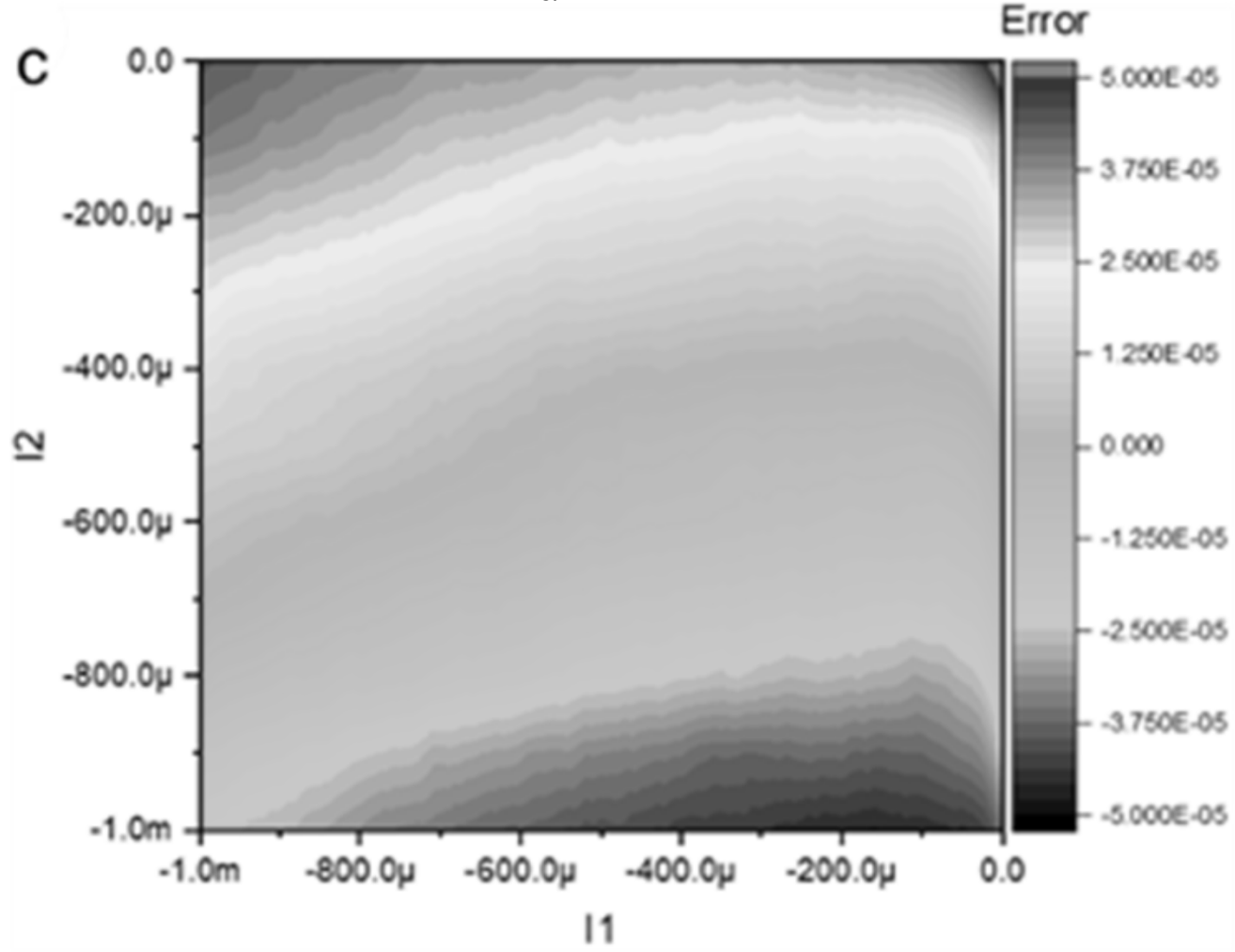

a
402
$V_1$
Voltage
$V_2$
$V_3$
Voltage Pulse
400
Current
404
Current
406
Current subtractor and non-Linear sense circuit
408
Time
410
TDC (Time to Digital)
b
Current
Exponential fitting
ADC linear sensing
Current (mA)
Time (us)
0
2
4
6
8
10
12
10
12
14
16
18
20
22
24
26
28

**Figure 4**


a
I1-I2 Ideal
0.0
-200.0µ
-400.0µ
-600.0µ
-800.0µ
-1.0m
I2
-1.0m
-800.0µ
-600.0µ
-400.0µ
-200.0µ
0.0
I1
-0.001185
-0.001446
-0.001706
-0.001967
-0.002227
-0.002488
-0.002749
-0.003009
-0.003270


b
Iout
0.0
-200.0µ
-400.0µ
-600.0µ
-800.0µ
-1.0m
I2
-1.0m
-800.0µ
-600.0µ
-400.0µ
-200.0µ
0.0
-0.001185
-0.001445
-0.001706
-0.001967
-0.002227
-0.002488
-0.002749
-0.003009
-0.003270


c
Error
5.000E-05
3.750E-05
2.500E-05
1.250E-05
0.000
-1.250E-05
-2.500E-05
-3.750E-05
-5.000E-05
0.0
-200.0μ
-400.0μ
-600.0μ
-800.0μ
-1.0m
I2
-1.0m
-800.0μ
-600.0μ
-400.0μ
-200.0μ
0.0
I1

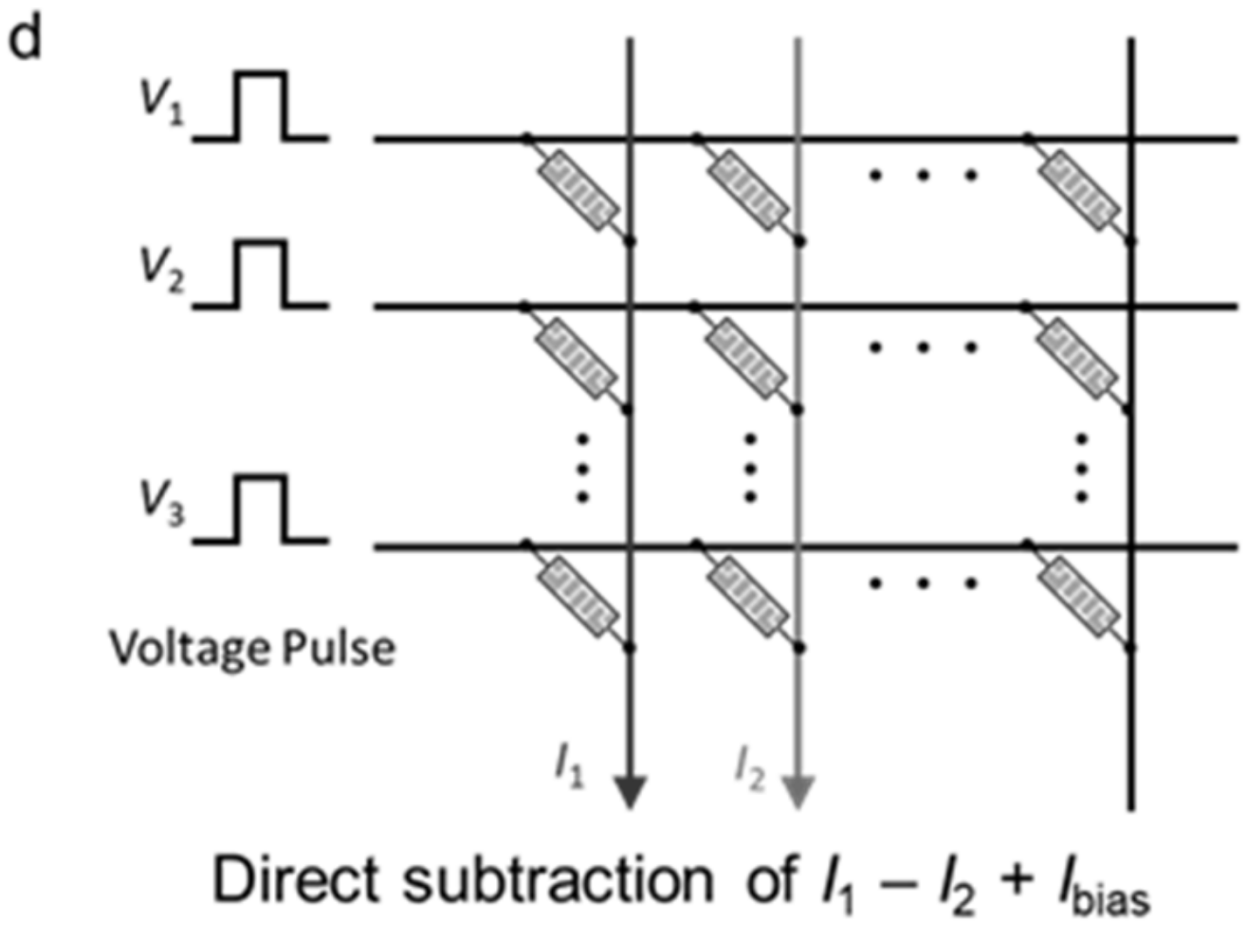

d
$V_1$
$V_2$
$V_3$
Voltage Pulse
$I_1$
$I_2$
Direct subtraction of $I_1 - I_2 + I_{bias}$

**Figure 5**

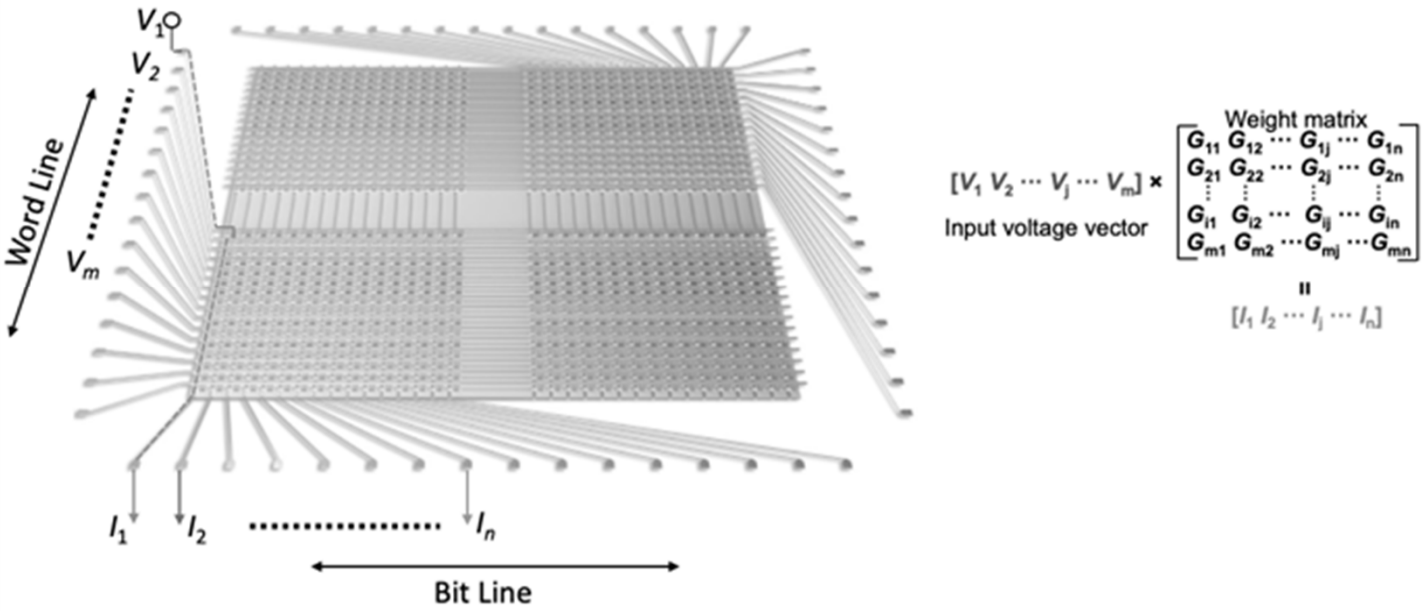

$V_1$
$V_2$
Word Line
$V_m$
$I_1$
$I_2$
$I_n$
Bit Line
$[V_1\ V_2 \cdots V_j \cdots V_m] \times$
Input voltage vector
Weight matrix
$\begin{bmatrix} G_{11} & G_{12} \cdots & G_{1j} \cdots & G_{1n} \\ G_{21} & G_{22} \cdots & G_{2j} \cdots & G_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ G_{i1} & G_{i2} \cdots & G_{ij} \cdots & G_{in} \\ G_{m1} & G_{m2} \cdots & G_{mj} \cdots & G_{mn} \end{bmatrix}$
=
$[I_1\ I_2 \cdots I_j \cdots I_n]$

**Figure 6**