A METHOD OF FABRICATING CMOS DEVICES FEATURING DUAL GATE AND A HIGH DIELECTRIC CONSTANT GATE INSULATOR LAYER

ABSTRACT

A method of forming a metal gate structure, on a high k gate insulator layer, for NMOS devices, and simultaneously forming a metal - polysilicon gate structure, on the same high k gate insulator layer, for PMOS devices, has been developed. The method features forming openings in a composite insulator layer, via removal of silicon nitride dummy gate structures that were embedded in a composite insulator layer, with the openings exposing regions of the semiconductor substrate to be used for subsequent NMOS and PMOS channel regions. Deposition of a high k gate insulator layer is followed by deposition of an in situ doped polysilicon layer. After removal of a portion of the in situ doped polysilicon layer located in the NMOS region, a metal layer is deposited on the underlying high k gate insulator layer in the NMOS region, and on the in situ polysilicon layer in the PMOS region. Removal of unwanted regions of metal, and of in situ polysilicon, result in the definition of a metal gate structure, on the high k gate insulator layer, in the NMOS region, and in the definition of a metal - in situ doped polysilicon gate structure, on the high k gate insulator layer, in the PMOS region, with both gate structures embedded in openings in the composite insulator layer, previously formed via removal of the silicon nitride dummy gate structures.

Figure 1