

FIG. 1

This cross-sectional view shows a central vertical structure (12) with three regions: 12a (dashed), 12b (solid), and 12c (dashed). It is flanked by side structures 25a, 25b, and 25c. A central layer 4 is above the side structures. A base layer 3 is at the bottom. A diagonal line 6 separates the central structure from the right side. Other labels include 7a, 7b, 7c, 8, 9, 13, 14, 16, and 21.

FIG. 4

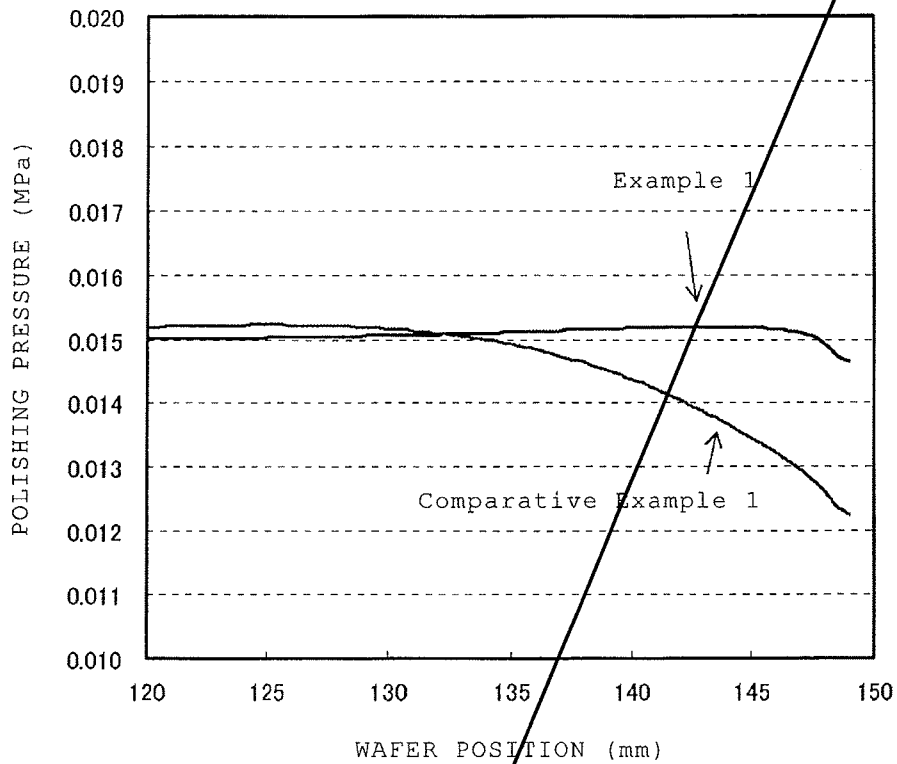


FIG. 5

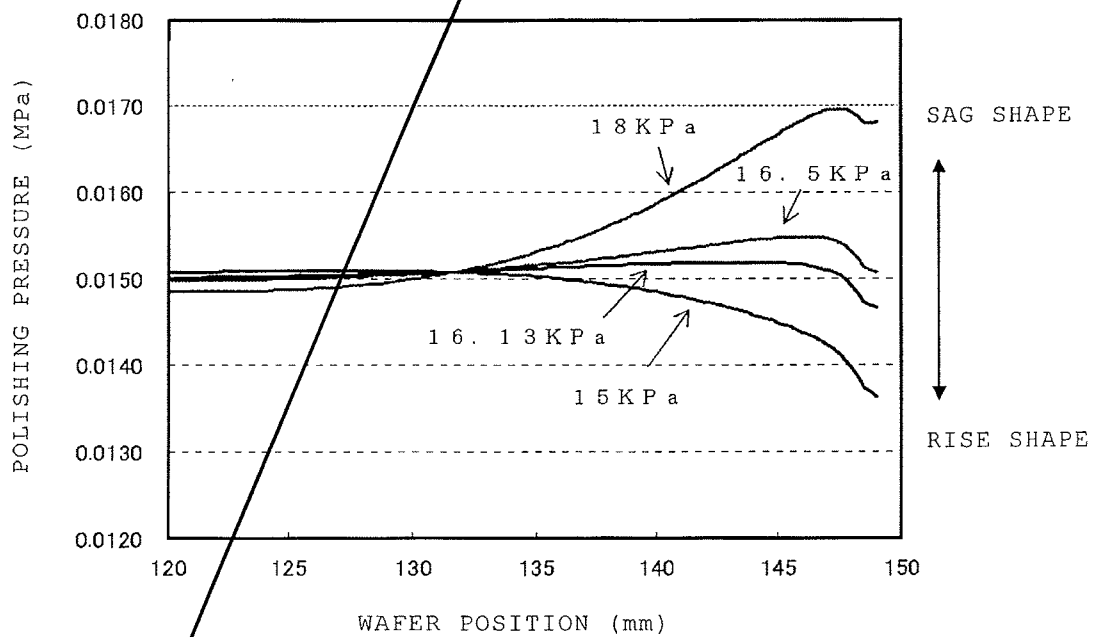


FIG. 6

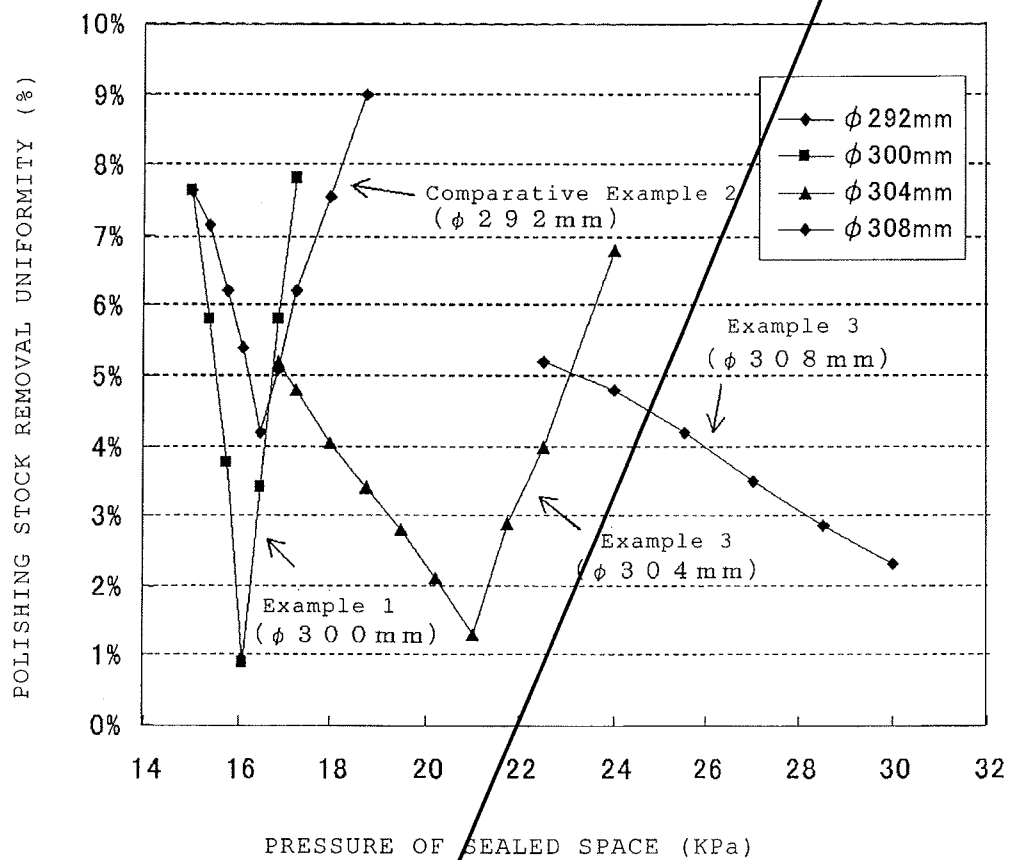


FIG. 7

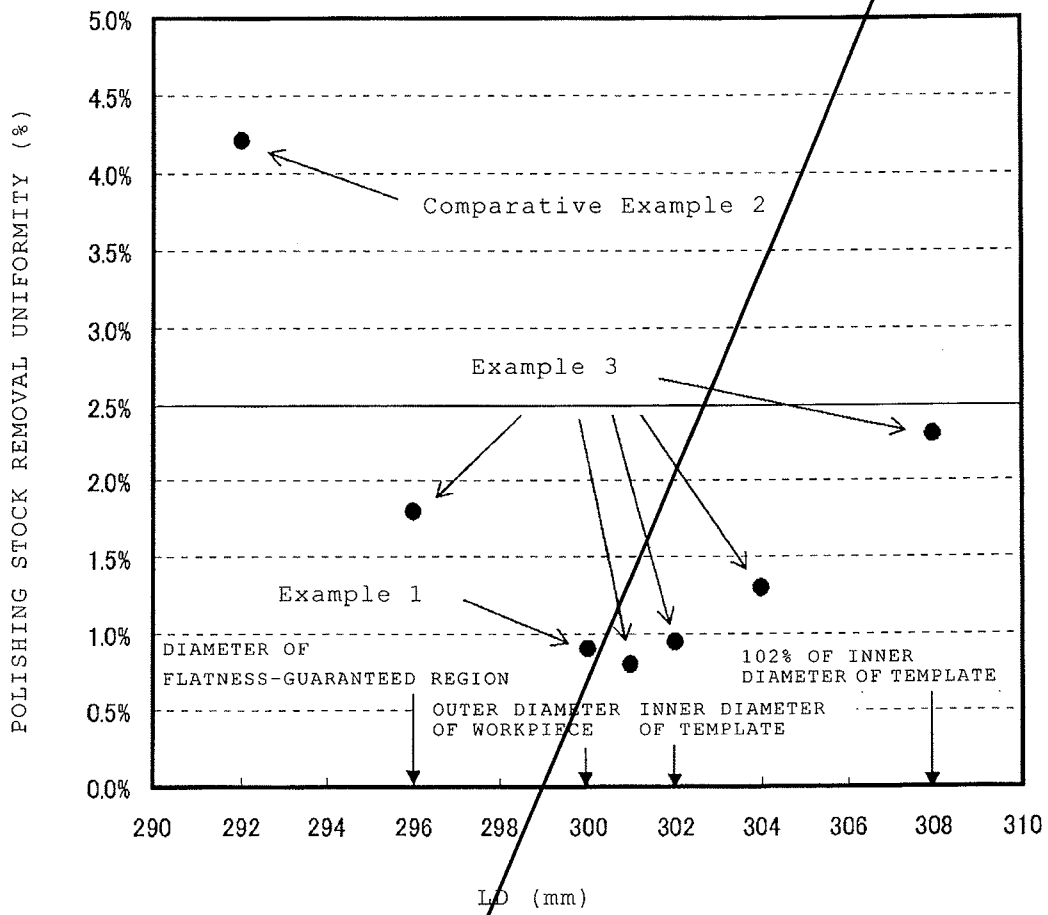


FIG. 8

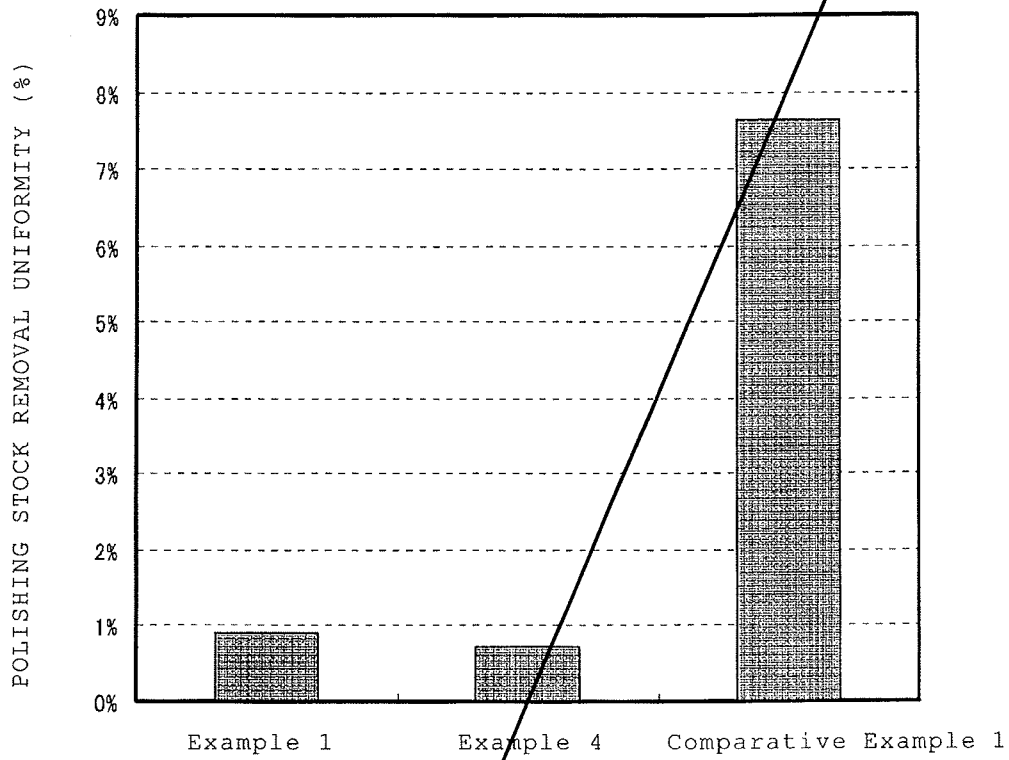


FIG. 9

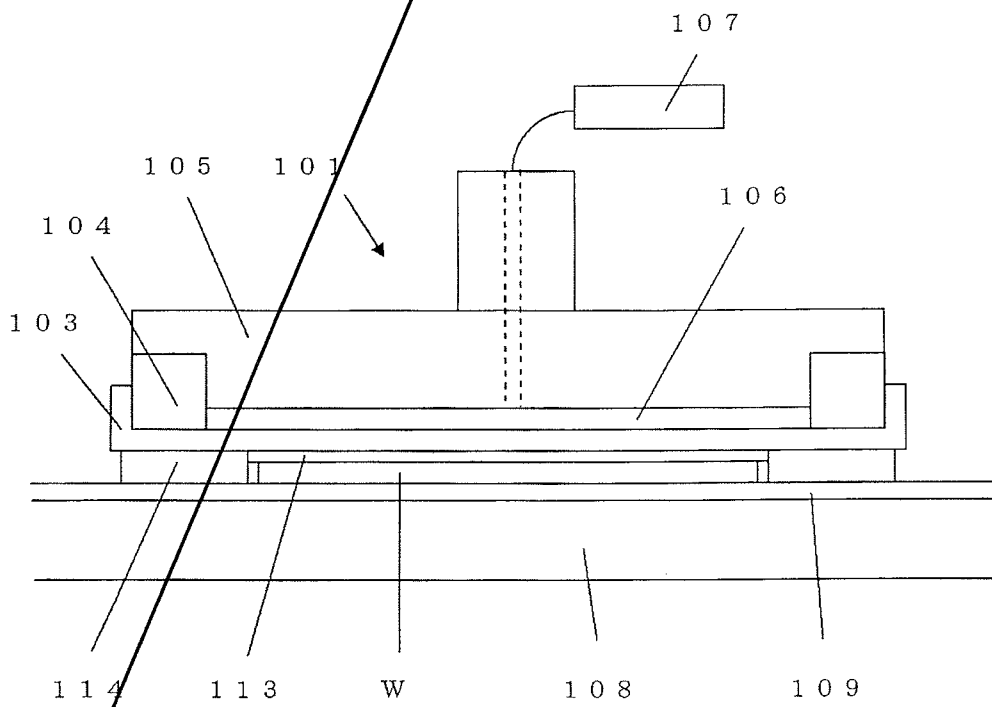
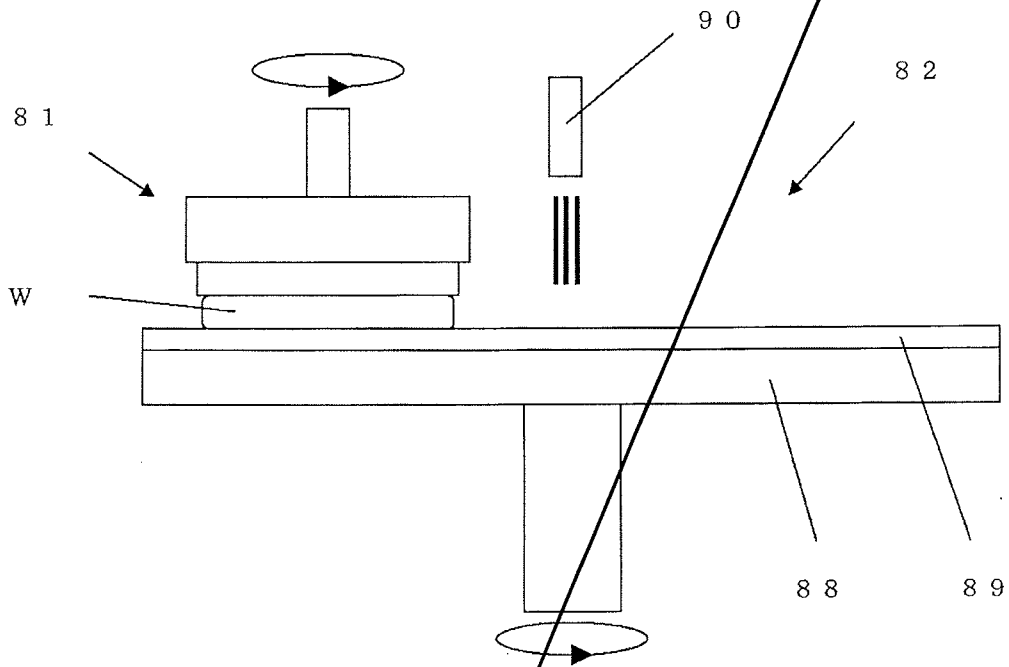


FIG. 10

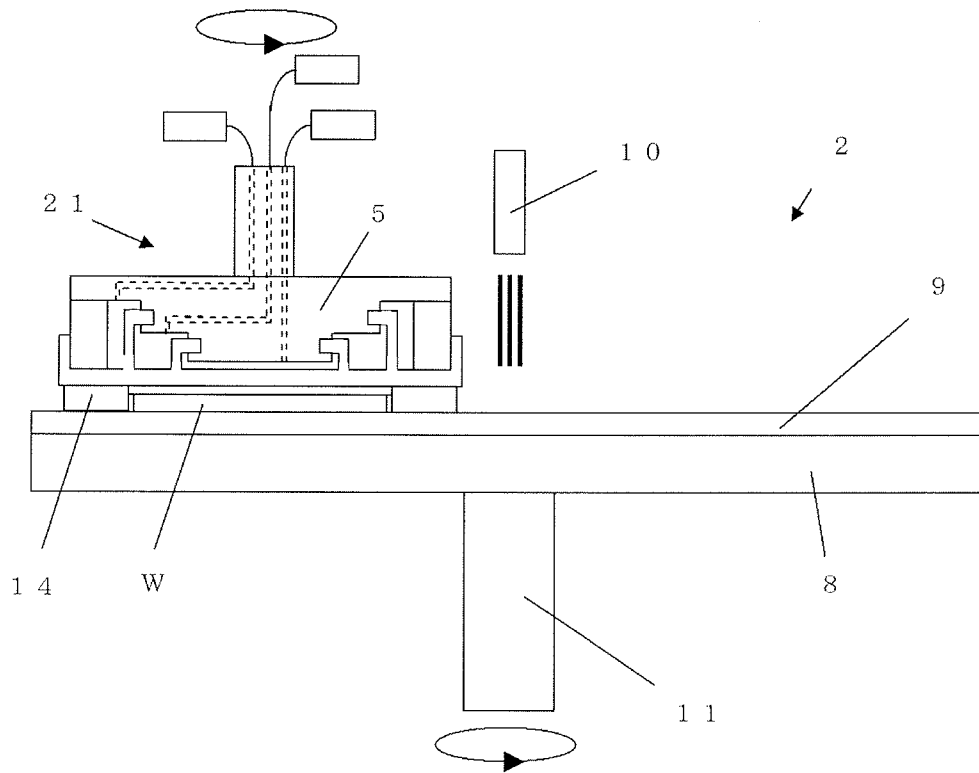


[FIG. 1]

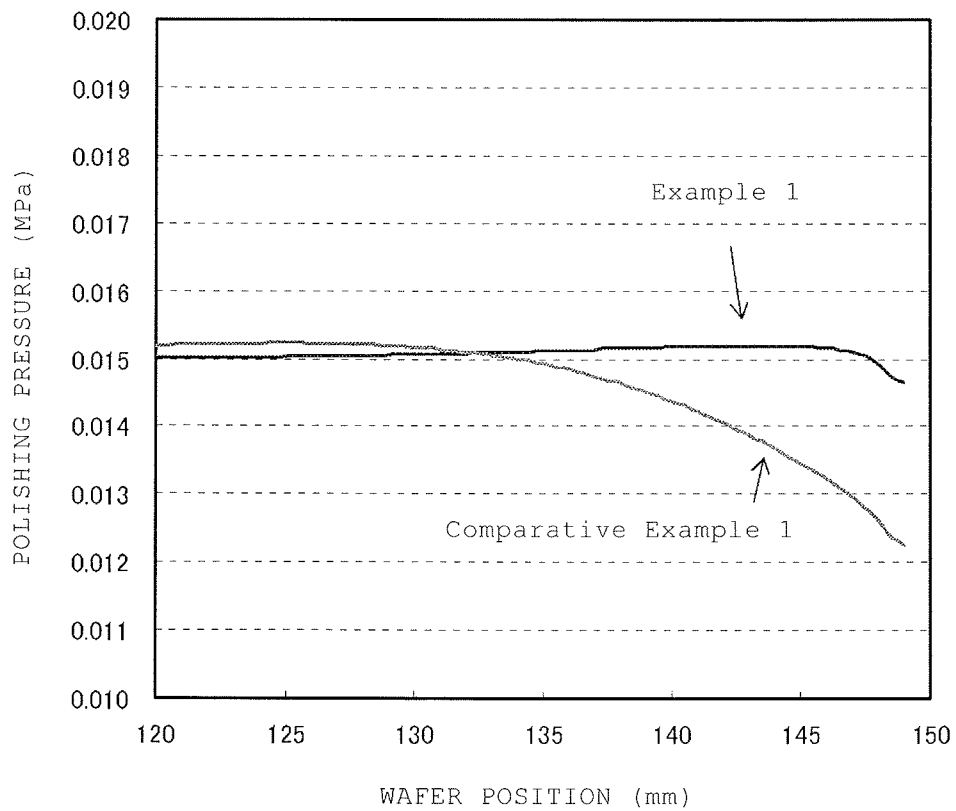
FIG. 1 is a schematic cross-sectional view of a semiconductor device. The device includes a substrate 8 with a thin layer 9 on top. A main body 1 is built on this. At the bottom of the main body is a layer 14. Above it is a layer 3. The central part of the main body contains a layer 5 with a central region 6. On the left and right sides of the central region are structures 15a and 15b. Above the central region are two rectangular blocks 7a and 7b, connected to the central region by vertical lines 12a and 12b. The overall width of the device is labeled W, and the thickness of the main body is labeled TD. The length of the central region is labeled LD. The device is labeled 1.

[illegible]

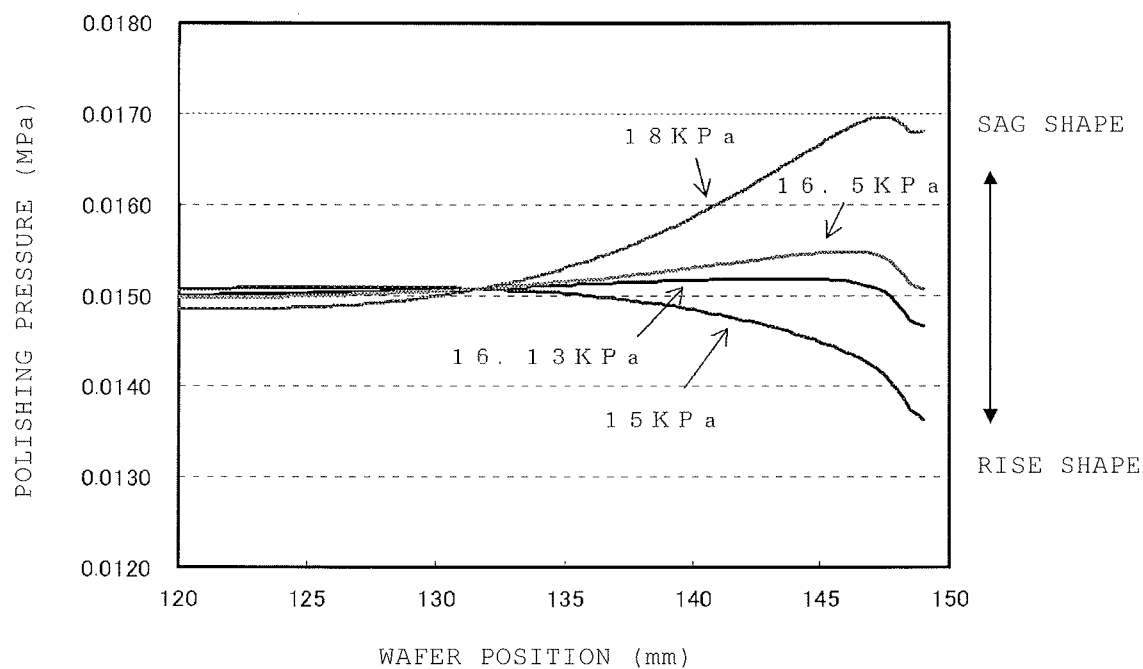
[FIG. 3]



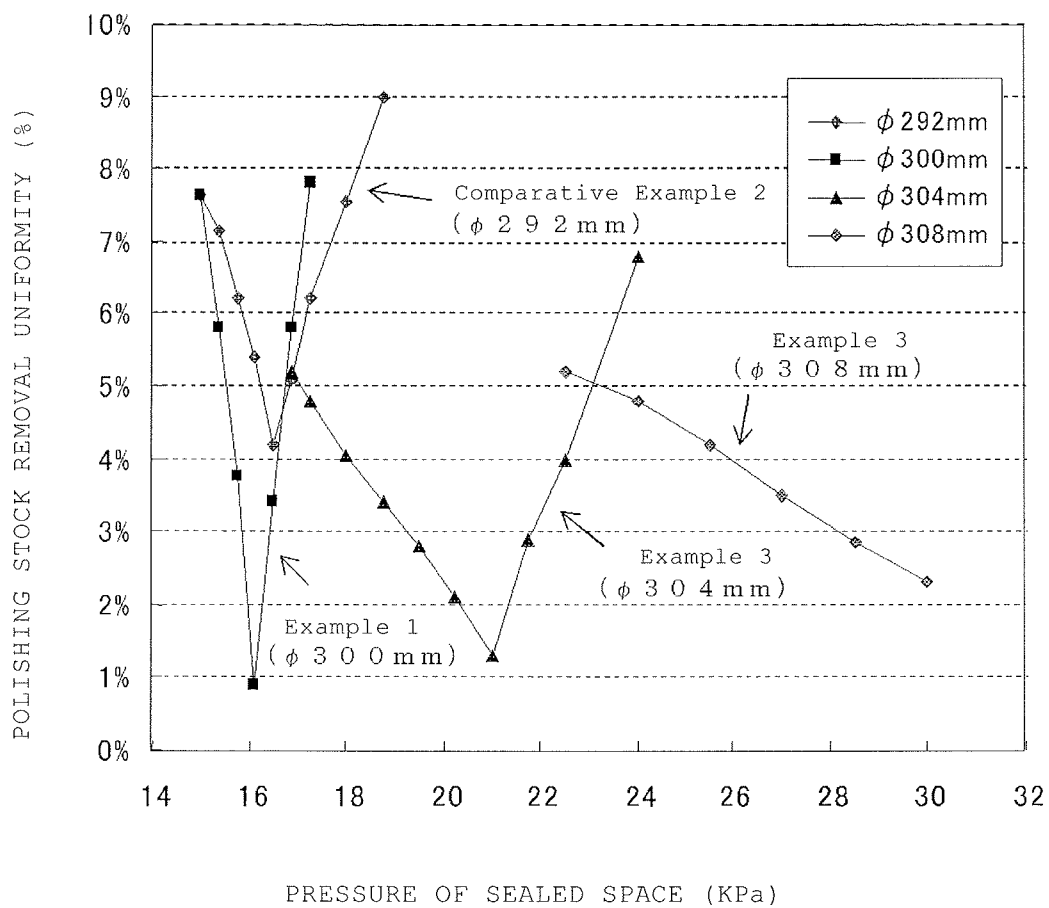
[FIG. 4]



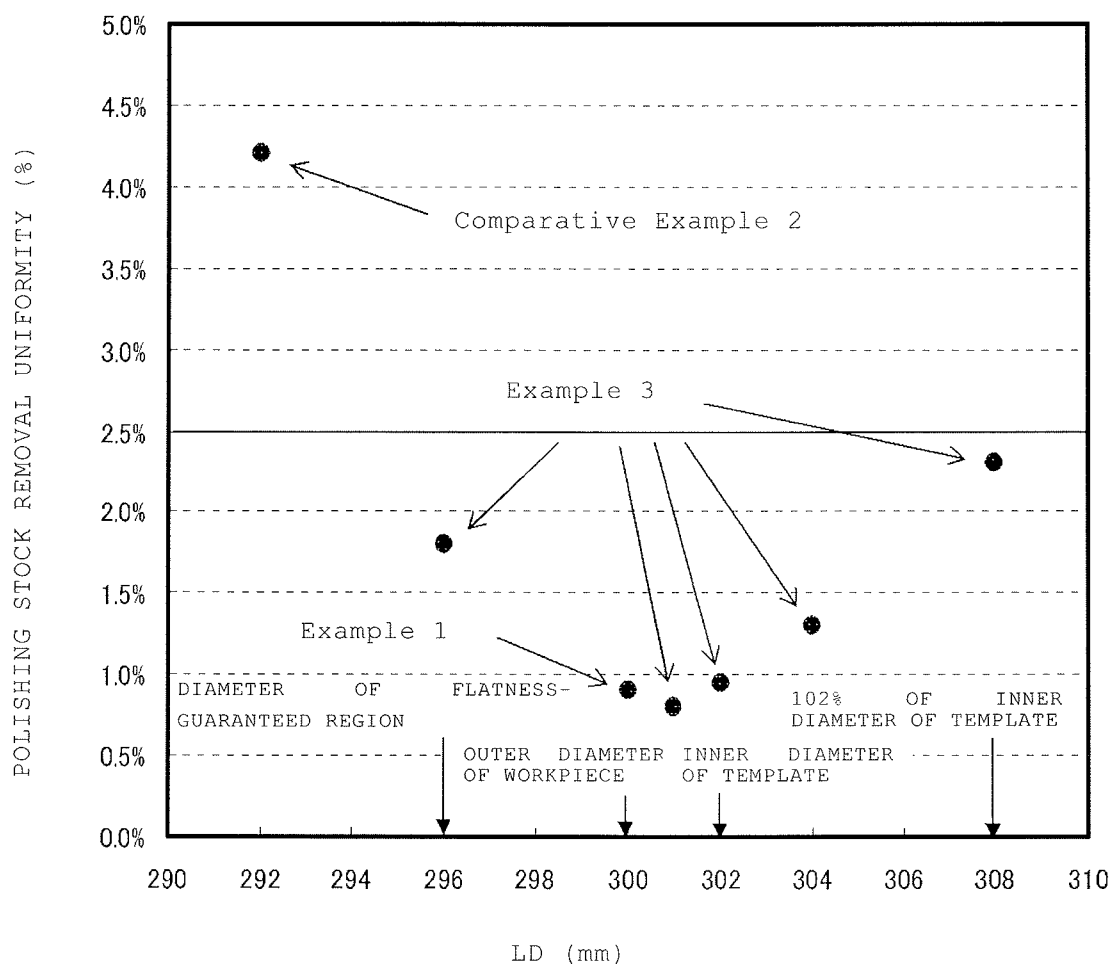
[FIG. 5]



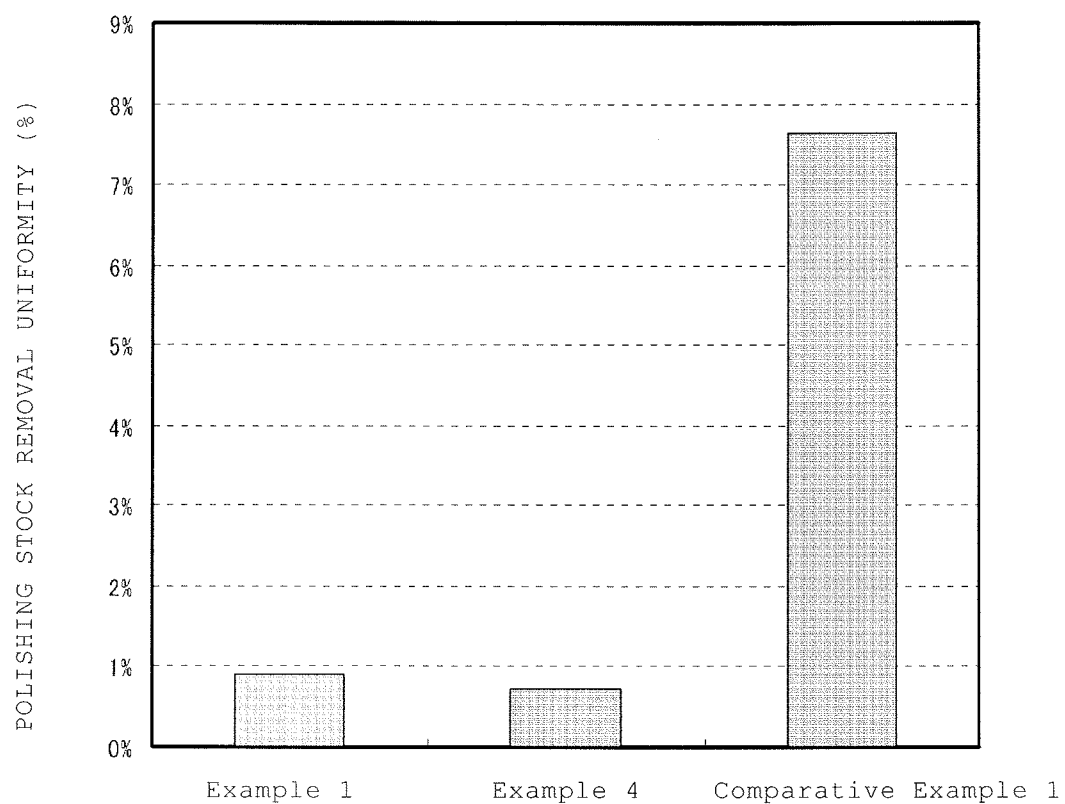
[FIG. 6]



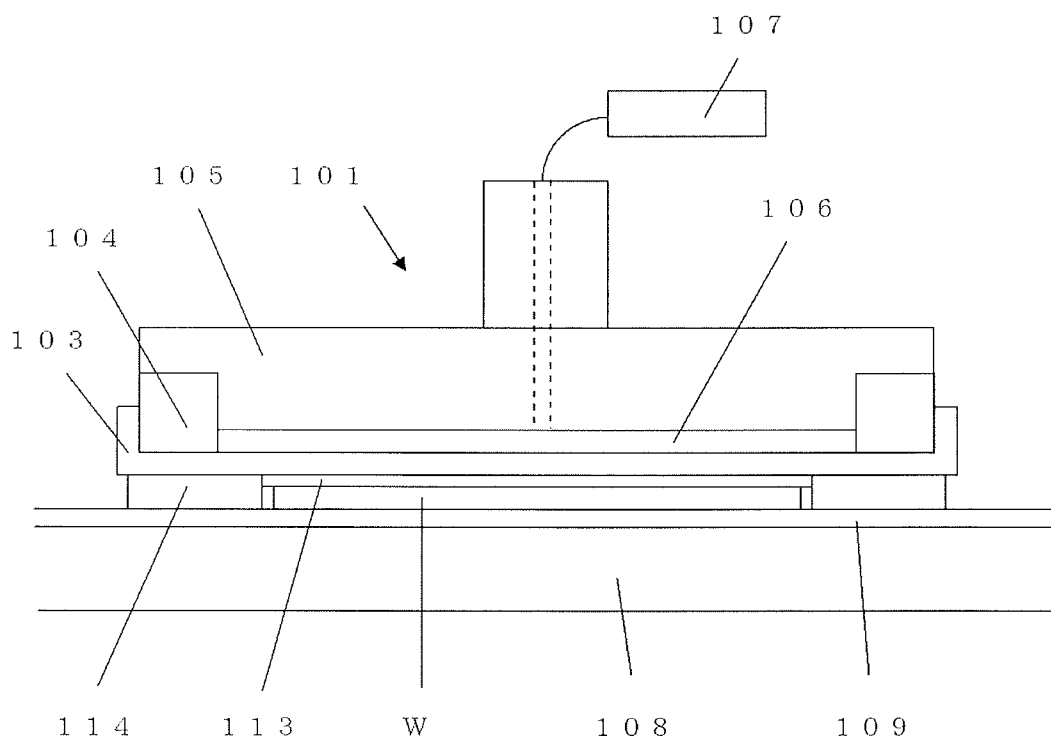
[FIG. 7]



[FIG. 8]



[FIG. 9]



[FIG. 10]

