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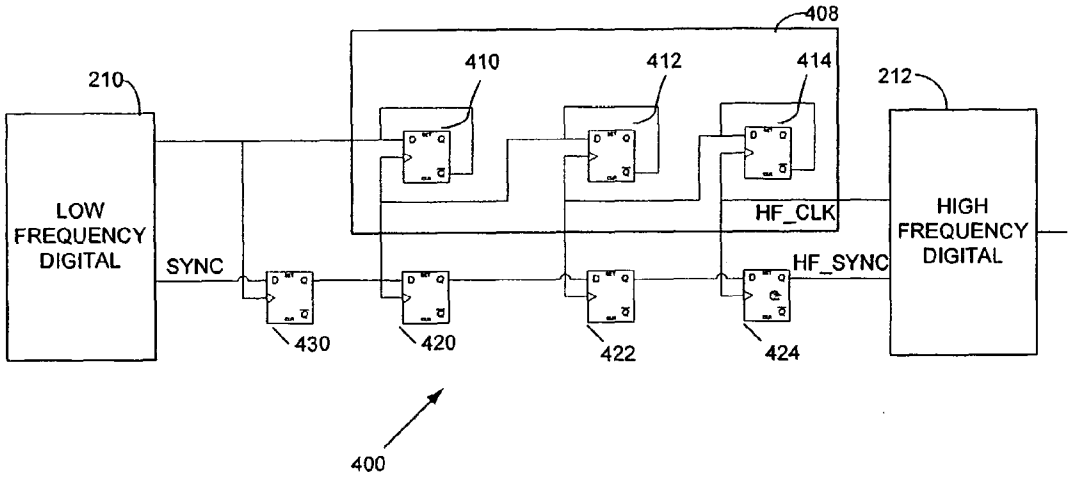
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(54) **Title:** SYNCHRONIZATION BETWEEN LOW FREQUENCY AND HIGH FREQUENCY DIGITAL SIGNALS



(57) **Abstract:** A synchronization circuit for synchronizing low frequency digital circuitry and high frequency digital circuitry. The synchronization circuit produces an ordered series of clocks from the high-frequency digital clock. The clocks have a deterministic time relationship, with at least one clock having a period longer than the timing uncertainty associated with a synchronization signal. The synchronization signal is passed through a chain of latches, each one clocked by one of the divided down clocks with successively higher frequency. These latches align the synchronization signal with the clocks produced by the clock divider, ultimately aligning the synchronization signal with the high frequency clock. This synchronization circuit is described in connection with automatic test equipment used in the manufacture of semiconductor devices.

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