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MEMORY CONTROLLER FOR DIRECT OR INTERLEAVE MEMORY ACCESSING

This invention relates to the field of data processing and, more particularly, to a data processing system having a memory controller which supports both direct and interleave accessing of a dynamic read/write memory.

BACKGROUND OF THE INVENTION

Personal computers commonly use dynamic memory read/write chips that are addressed or selected as physical banks, the chips being arranged in single in-line memory modules (SIMMs). Row address strobe (RAS) signals are used to select the physical banks of memory. In a system with, for example, sixteen banks, sixteen unique RAS lines are required. Lower cost, high performance memory systems are designed to operate in a direct mode wherein only one RAS line is active at any one time. In contrast, higher cost, high performance memory systems are designed with a wider memory data path and operate in an interleaved mode so that two RAS lines are simultaneously active for two bank interleaving.

Typically a memory controller is connected between the memory and a microprocessor, a direct memory access (DMA) controller, and other devices which access the memory. One of the functions of a memory controller is to decode the addresses of the locations to be accessed and generate the appropriate RAS select signal(s) for activating the proper memory bank(s) in accordance with the mode (direct or interleaved) of operation. In the direct mode, a memory controller need only have one decoder per memory bank, whereas in the interleaved mode, the controller needs only one decoder per two banks, the banks being arranged in pairs. A memory controller that supports both modes must provide a decoding mechanism for both modes. Typically, this is done by using two sets of decoders, one set being one decoder per bank for direct mode and the other set being one decoder per pair of banks for interleaved mode. Additional decode logic is needed to select the appropriate set.

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According to the present invention there is provided a data processing system comprising: a microprocessor; a memory including at least two memory banks each having a predetermined number of addressable storage locations, each bank being accessible by control signals including a row address strobe signal RAS; a memory controller for controlling access to said memory; and a bus connected between said microprocessor and said memory controller, said bus comprising address, data and control lines; said microprocessor being operable to initiate a memory access by placing address signals on said address lines, and control signals defining read/write operations on said control lines. characterised in that; said memory controller comprises a plurality of bank address decoders connected to said address lines, and associated with said banks, each decoder being operable in response to decoding an address on said address lines as being in a range of storage locations located in said associated bank to generate a Bank Select signal, a single logical circuit having inputs connected to said two decoders to receive said Bank Select signals therefrom and produce an inactive output signal when said Bank Select signals are both inactive, said logical circuit being further operable to produce an active output signal when at least one of said Bank Select signals is active, and mode control means connected to outputs of said logical circuit and said two decoders, said mode control means being selectively set to operate in either a direct mode or an interleaved mode, said mode control means being operable when set to operate in direct mode to produce a single row address strobe signal in response to a Bank Select signal from one of said decoders, said mode control means being operable when set to operate in interleave mode to produce two row address strobe signals in response to an active output from said logical circuit.

Further according to the present invention there is provided a memory controller for use in a data processing system having a memory and a microprocessor for accessing said memory, said memory having a plurality of banks each comprising a multiplicity of storage locations, said storage locations in each bank have a unique range of addresses, said ranges being contiguous, said memory being accessible in response to said microprocessor outputting control and address signals, said memory controller comprising: a plurality of bank address decoders adapted to

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receive addresses from said microprocessor and produce first Bank Select signals in accordance with which bank contains an addressed storage location; a single logical circuit connected to two of said decoders and operative to produce a second Bank Select signal in response to receiving an active one of said first Bank Select signals, and mode control means connected to said logical circuit and said two decoders, said mode control means being selectively set to operate in either a direct mode or an interleaved mode, said mode control means being operable when set to operate in direct mode to produce a single row address strobe signal in response to a Bank Select signal from one of said decoders, said mode control means being operable when set to operate in interleave mode to produce two row address strobe signals in response to an active output from said logical circuit.

In the drawings:

Fig. 1 is a simplified block diagram of a prior art memory bank decoding system operable in direct mode;

Fig. 2 is a view similar to Fig. 1 showing a prior art system operable in interleaved mode;

Fig. 3 is a view similar to Figs. 1 and 2 showing a prior art system operable in either a direct mode or an interleaved mode;

Fig. 4 is a view similar to Fig. 3 illustrating the present invention;

Fig. 5 is a more detailed block diagram of a data processing system embodying the present invention; and

Fig. 6 is a block diagram of a portion of the memory controller shown in Fig. 5.

DETAILED DESCRIPTION

Prior art memory systems of the type improved upon by the invention are shown in Figs. 1-3, while a comparable diagram illustrating the

invention is shown in Fig. 4. Referring to Fig. 1, the invention is described hereinafter relative to a dynamic memory system 110 having two banks of single in-line memory modules (SIMM) 112 and 114. Each SIMM has one meg of addressable locations, and is 32 bits wide. That is, on each access, 32 bits or one doubleword may be transferred. Two active low, address decoders 116 and 118 are connected to an address bus 120. Decoder 116 produces an active Bank Select output signal when the addressed location is within the first one meg of memory locations and decoder 118 will produce an active output Bank Select signal when the addressed location is within the range from one to two megs. Decoders 116 and 118 have output lines respectively connected to timing circuits 126 and 128. In response to an address appearing on bus 120, the one of decoders 116 and 118 corresponding to the bank being accessed will produce an active Bank Select signal that is transmitted to the timing circuit which then produces the appropriate operating signals, including a RAS signal, to access the desired location in the selected bank. Such mode of operation is known as the direct mode.

Fig. 2 shows the same memory banks arranged for interleave operation wherein the banks are combined to provide a 64 bit wide memory data path. In this case, a decoder 130 is connected to bus 120 and in response thereto will produce an active Bank Select signal when the accessed address is in the range 0-2 megs. Decoder 130 is connected to timing logic circuits 126 and 128 which in response to receiving an active Bank Select signal and a RAS timing signal on line 129 transmits RAS0 and RAS1 signals to banks 112 and 114 respectively. The RAS timing signal signal controls the high/low timing of the individual RAS0 and RAS1 pulses.

Fig. 3 illustrates a system for supporting both direct and interleave modes. A register 132 stores a control signal (D/I) defining the mode of operation and the memory is accessed in either a direct mode or an interleave mode dependent upon the control signal. To accomplish this, the system further includes two multiplexers or MUXes 134 and 136 which are connected to register 132 and are operable in accordance with the control signal D/I to transmit a Bank Select signal to each bank from

decoder 130 when in the interleaved mode, or a Bank Select signal to each bank from decoders 116 and 118 when in the direct mode.

During the course of designing a memory controller for use in a high performance personal computer, in which an objective of such design was to provide a memory controller that supports both interleave and direct modes of operation, we analysed the above prior art designs and noted a relationship that allows the two decoders designed for the direct mode to be additionally used for the interleave mode by replacing decoder 130 with a simple AND circuit to thereby achieve the same results while reducing the number of circuits. Referring to Fig. 4, an AND circuit 140 has two inputs connected to the outputs of decoders 116 and 118 and an output connected to inputs of MUXes 134 and 136. When operating in the direct mode, MUXes 134 and 136 will transmit only the active output signal from decoders 116 or 118 dependent on which Bank Select signal is active. When operating in the interleave mode, the MUXes 134 and 136 will both transmit an active signal from AND circuit 140 to simultaneously access both banks 12 and 14. Circuit 140 effectively creates a single logical memory bank from two physical banks, in which the logical bank has an address range 0-2 megs.

The simplicity of the invention and why an AND circuit can be used should be understandable from the following logical reasoning. The output of decoder 116 is active or low only when the addressed location is in the range 0-1 meg. The output of decoder 118 is active or low only when the addressed location is in the range 1-2 megs. If the addressed location is above such range, the outputs of both decoders will be inactive or high. The logic of AND circuit 140 is such that when either or both inputs are active, its output will be active. If both are high or inactive, the output will likewise be high or inactive.

Referring now to Fig. 5, the data processing system there shown includes a microprocessor 10, a memory controller 12, a memory 14 having a plurality of SIMMs 16-1 through 16-n, a bus interface 18, a read only memory (ROM) 20 for storing a basic input/output operating system (BIOS), a non-volatile RAM (NVRAM) 22 for storing setup and configuration information, a direct memory access (DMA) controller 24, an expansion bus

26 connected to a plurality of expansion sockets 27-1 through 27-n, and a busmaster 28 connected to expansion socket 27-1. Controller 12 is a dual port controller connected to a CPU bus 30 and a system bus 32. A data bus 30D is connected between microprocessor 10 and a buffer 34, and a data bus 32D is connected between bus interface 18 and a buffer 35. Buffers 34 and 35 are connected to memory 14 by the data bus 36D of a memory bus 36. It should be noted that the address, control, and data busses of busses 26, 30, 32 and 36 are referenced using the respective suffixes A, C, and D.

Except for certain details of controller 12 and the operation as described below, the system is constructed in accordance with known principles and uses well documented, commercially available devices so that further details thereof not necessary to an understanding of the invention are omitted herefrom. It is to be understood that the many support and other devices commonly included in a data processing system have been omitted for simplicity of illustration.

Within the system as described thus far, memory 14 can be accessed by microprocessor 10, DMA controller 24, or bus master 28. Since such memory accessing is similar for each such device, the following description will be limited to illustrating how microprocessor 10 accesses memory 14. It is apparent to those skilled in the art how other devices can similarly access the memory. Furthermore, it is recognised there are many different memory configurations but for the purpose of illustrating the invention, memory 14 is assumed to have a maximum capacity of eight, 32-bit wide SIMMs, each SIMM having one or two banks, each bank having a capacity of 1 or 4 Mbytes, and operable at RAS speeds of 30-100ns. Additional memory can be added through use of the expansion bus.

Fig. 6 shows generally how the invention is incorporated into memory controller 12. Address bus 120 receives a bank address from bus 30 (Fig. 5) and inputs such address into decoders 116 and 118. The outputs of the decoders are connected to inputs of a logic circuit 42 which includes MUXes 134 and 136, and AND circuit 140. An I/O port 40 contains register 132. When the system is initially configured, and the user decides

whether to have the system operate in a direct mode or an interleaved mode, the control signal in register 132 is then set by addressing such port and writing the appropriate D/L signal in the register. Normally, once a system is thus set to operate in a given mode, it remains that way. Register 132 is connected to transmit the mode control signal D/L to logic 42. Controller 12 also includes a state machine 44 that in response to address and control signals from the microprocessor on bus 30, provides timing signals to logic 42 causing appropriate memory operating signals, including the RAS signals, to be transmitted to memory 14 to access the bank containing the addressed memory location.

While the invention is described above relative to a one Meg SIMM, for which there is an advantage of replacing one eight-to-one decoder by a single AND circuit, the advantage becomes even greater when the complexity of a decoder is increased to handle various size SIMMs and various starting addresses.

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CLAIMS

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1. A data processing system comprising:

a microprocessor (10);

a memory (14) including at least two memory banks each having a predetermined number of addressable storage locations, each bank being accessible by control signals including a row address strobe signal RAS;

a memory controller for controlling (12) access to said memory;

and a bus (30) connected between said microprocessor and said memory controller, said bus comprising address, data and control lines;

said microprocessor being operable to initiate a memory access by placing address signals on said address lines, and control signals defining read/write operations on said control lines characterised in that;

said memory controller comprises

a plurality of bank address decoders (116, 118) connected to said address lines, and associated with said banks, each decoder being operable in response to decoding an address on said address lines as being in a range of storage locations located in said associated bank to generate a Bank Select signal,

a single logical circuit (140) having inputs connected to said two decoders to receive said Bank Select signals therefrom and produce an inactive output signal when said Bank Select signals are both inactive, said logical circuit being further operable to produce an active output signal when at least one of said Bank Select signals is active,

and mode control means (132) connected to outputs of said logical circuit and said two decoders, said mode control means being selectively set to operate in either a direct mode or an interleaved mode, said mode

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control means being operable when set to operate in direct mode to produce a single row address strobe signal in response to a Bank Select signal from one of said decoders, said mode control means being operable when set to operate in interleave mode to produce two row address strobe signals in response to an active output from said logical circuit.

2. A data processing system in accordance with claim 1 wherein: said logical circuit (140) is an AND circuit.

3. A data processing system in accordance with claim 1 or 2 wherein said mode control means comprises:

a register (132) for storing a control signal defining whether said memory controller will operate in a direct mode or an interleaved mode,

multiplexer means (134, 136) connected to the outputs of said decoders, said logical circuit and said register and being operable to produce on an output thereof a first signal when said control signal is set for direct mode and a second signal when said control signal is set for interleave mode,

and timing means (44) connected to said multiplexer means and said banks for producing memory cycling signals including row address strobe signals to access said banks, said timing means being operable in response to receiving said first signal to produce a single row address strobe signal for only one of said banks when operating in the direct mode, said timing means being operable in response to receiving said second signal to produce two row address strobe signals for both banks when operating in the interleave mode.

4. A data processing system in accordance with claim 3 comprising:

an I/O port (40), said register being part of said port and being settable upon writing said control signal to said port.

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5. A memory controller for use in a data processing system having a memory (14) and a microprocessor (10) for accessing said memory, said memory having a plurality of banks each comprising a multiplicity of storage locations, said storage locations in each bank have a unique range of addresses, said ranges being contiguous, said memory being accessible in response to said microprocessor outputting control and address signals, said memory controller comprising:

a plurality of bank address decoders (116, 118) adapted to receive addresses from said microprocessor (10) and produce first Bank Select signals in accordance with which bank contains an addressed storage location;

a single logical circuit (140) connected to two of said decoders and operative to produce a second Bank Select signal in response to receiving an active one of said first Bank Select signals,

and mode control means (132) connected to said logical circuit and said two decoders, said mode control means being selectively set to operate in either a direct mode or an interleaved mode, said mode control means being operable when set to operate in direct mode to produce a single row address strobe signal in response to a Bank Select signal from one of said decoders, said mode control means being operable when set to operate in interleave mode to produce two row address strobe signals in response to an active output from said logical circuit.

6. A memory controller in accordance with claim 5 wherein:

said logical circuit (140) is an AND circuit.

7. A memory controller in accordance with claim 6 wherein said mode control means comprises:

a register (132) for storing a control signal defining whether said memory controller will operate in a direct mode or an interleaved mode,

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multiplexer means (134, 136) connected to the outputs of said decoders, said logical circuit and said register and being operable to produce on an output thereof a first signal when said control signal is set for direct mode and a second signal when said control signal is set for interleave mode,

and timing means (44) connected to said multiplexer means and said banks for producing memory cycling signals including row address strobe signals to access said banks, said timing means being operable in response to receiving said first signal to produce a single row address strobe signal for only one of said banks when operating in the direct mode, said timing means being operable in response to receiving said second signal to produce two row address strobe signals for both banks when operating in the interleave mode.

8. A memory controller in accordance with claim 7 comprising:

an I/O port (40), said register (132) being part of said port and being settable upon writing said control signal to said port.

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