

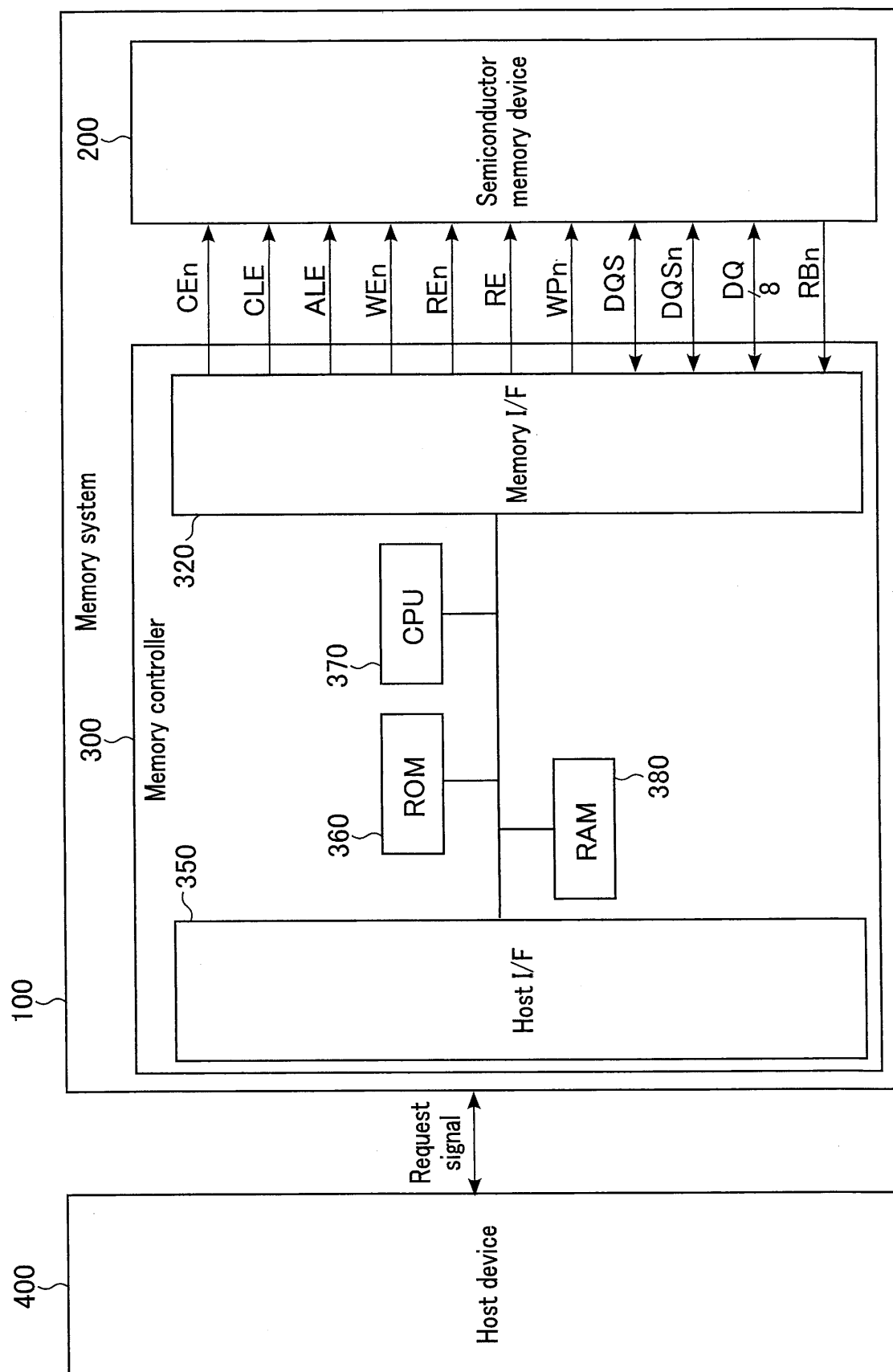


FIG. 1

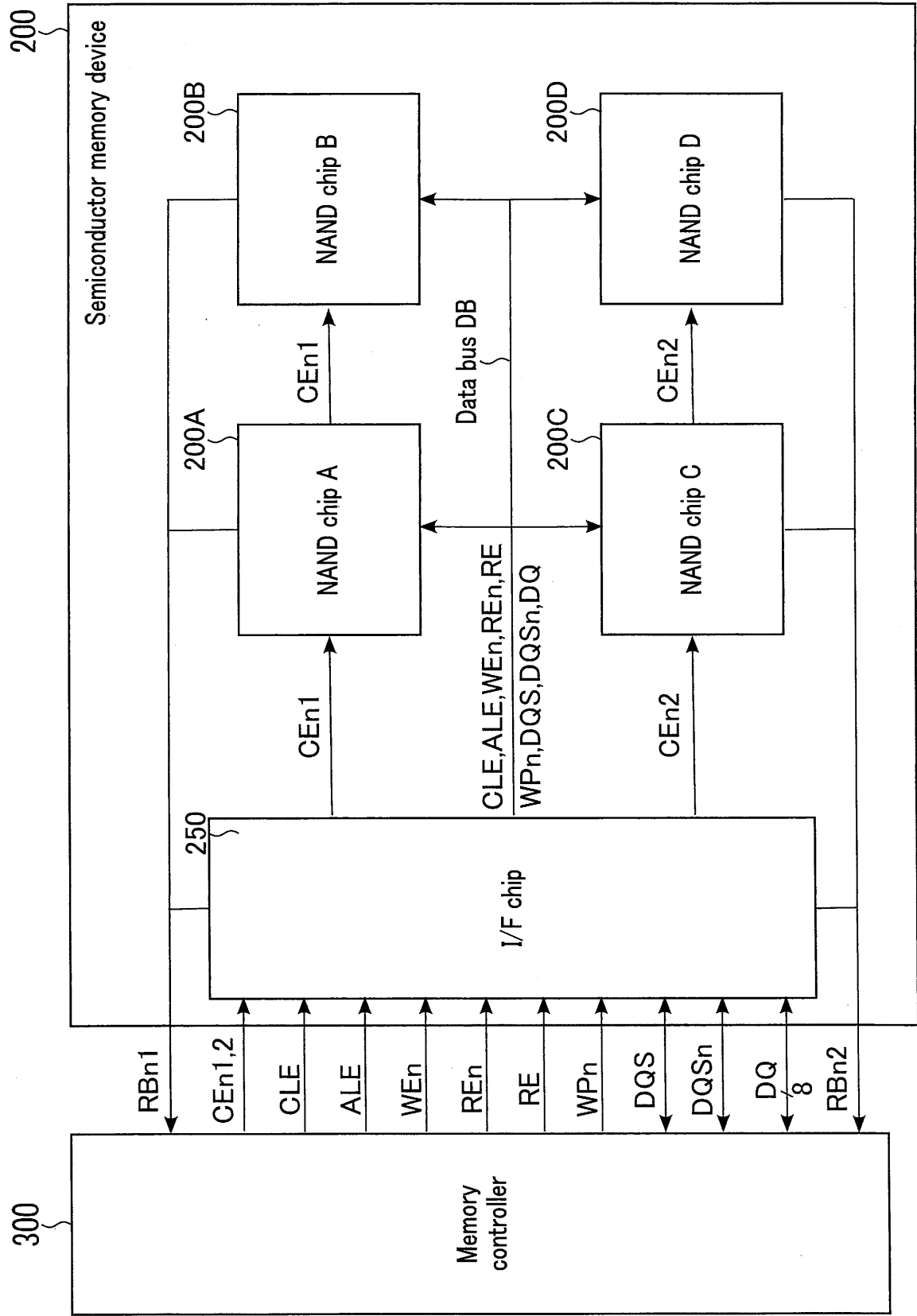


FIG. 2

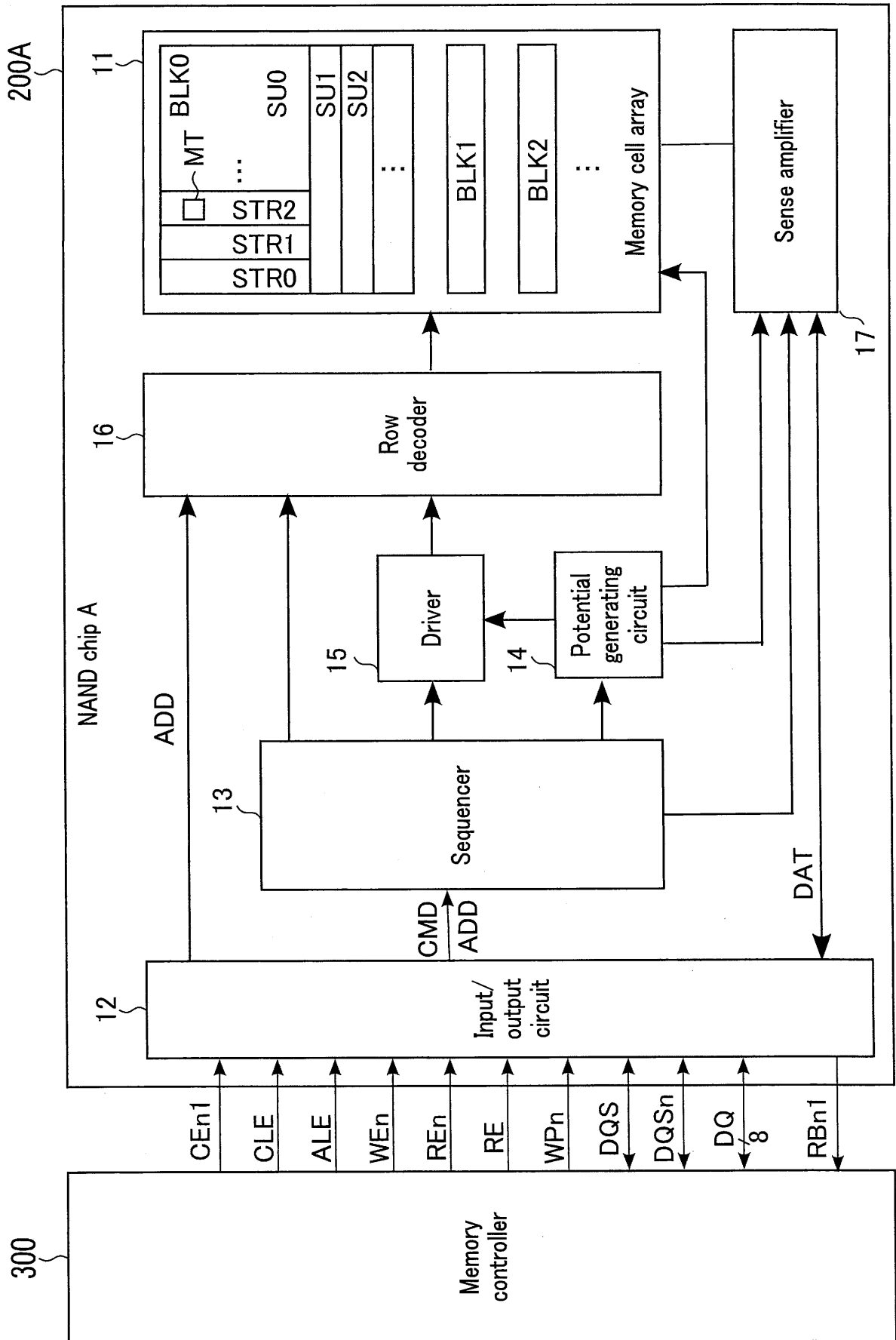


FIG. 3

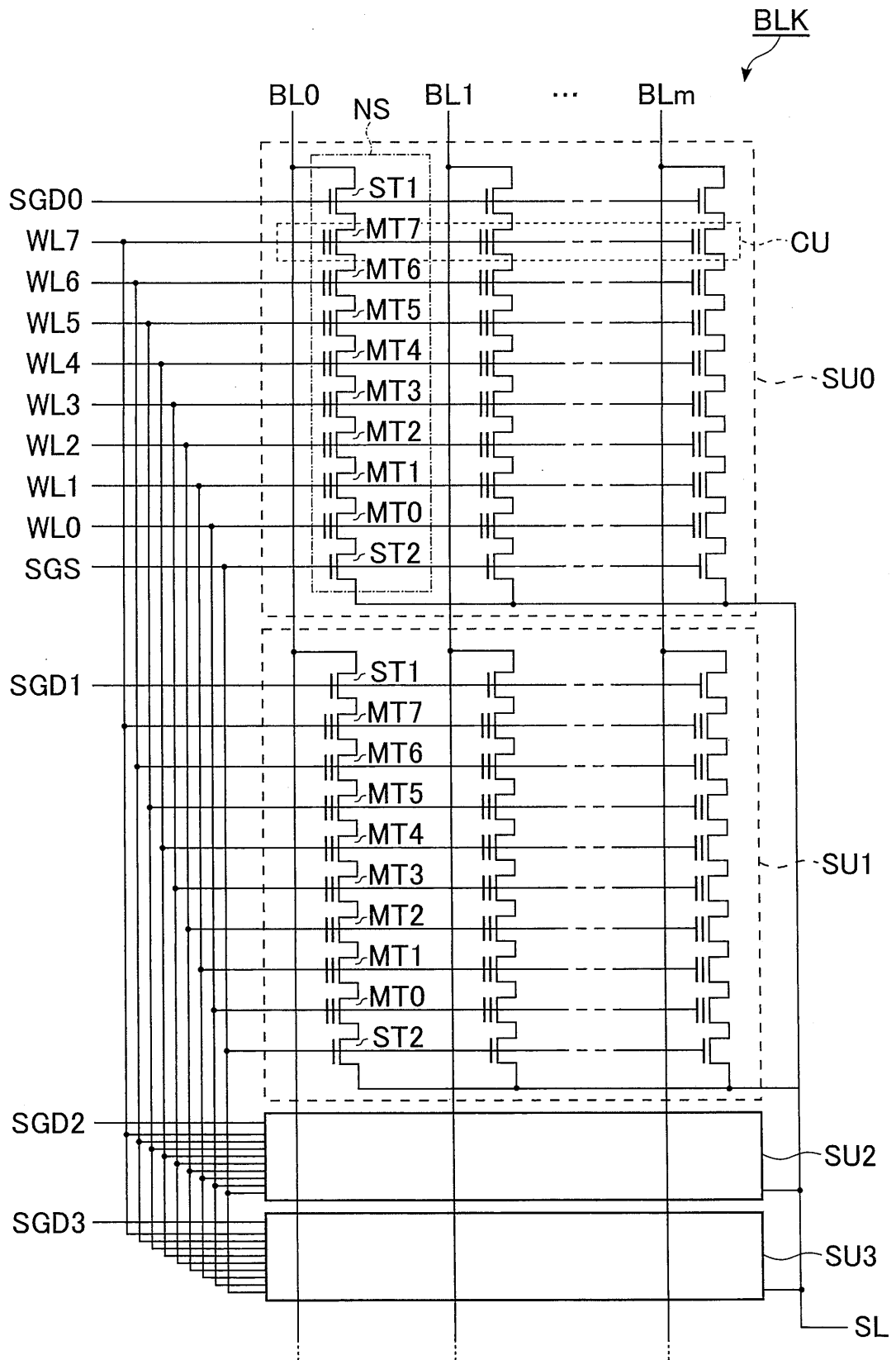


FIG. 4

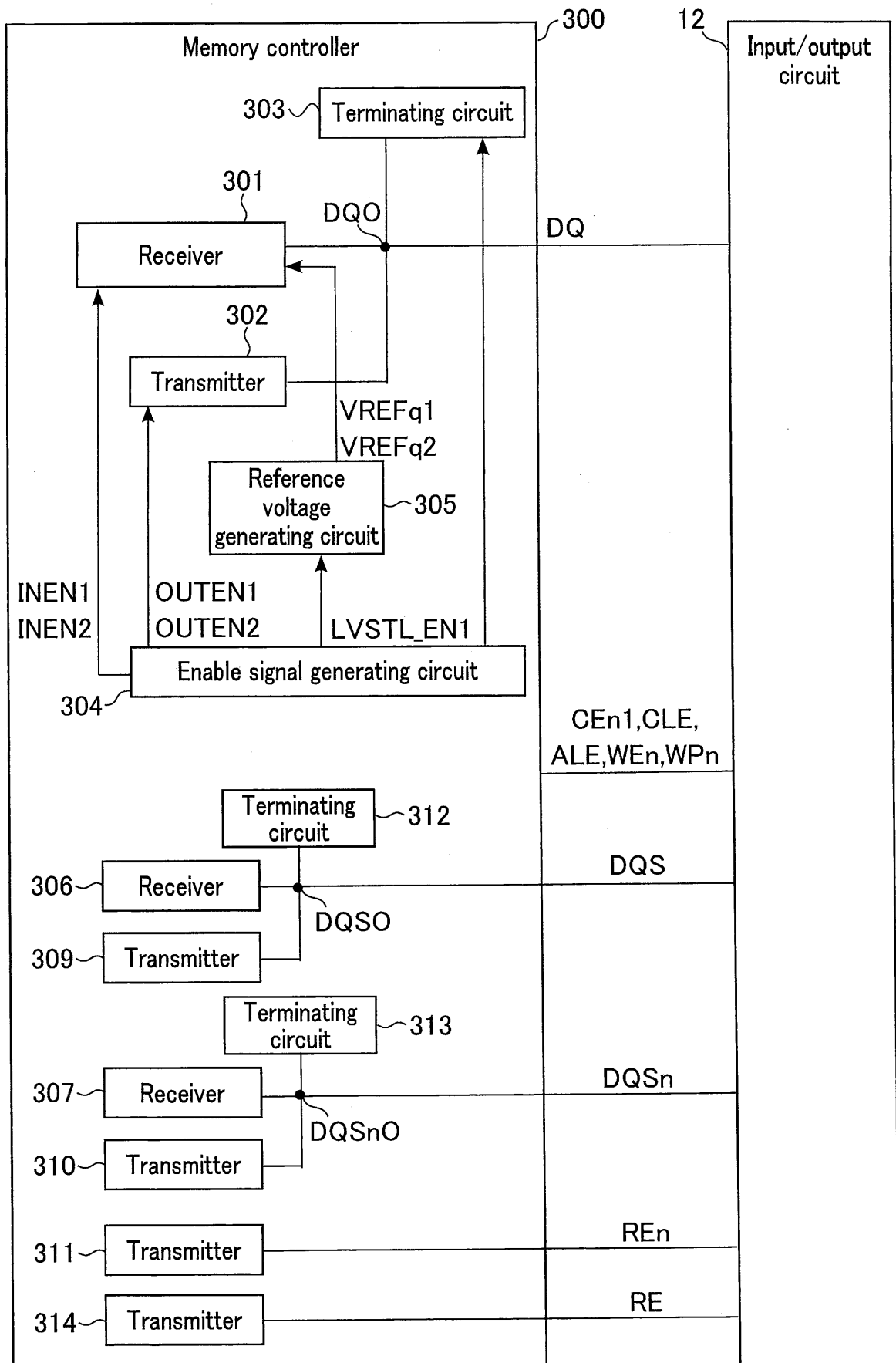


FIG. 5

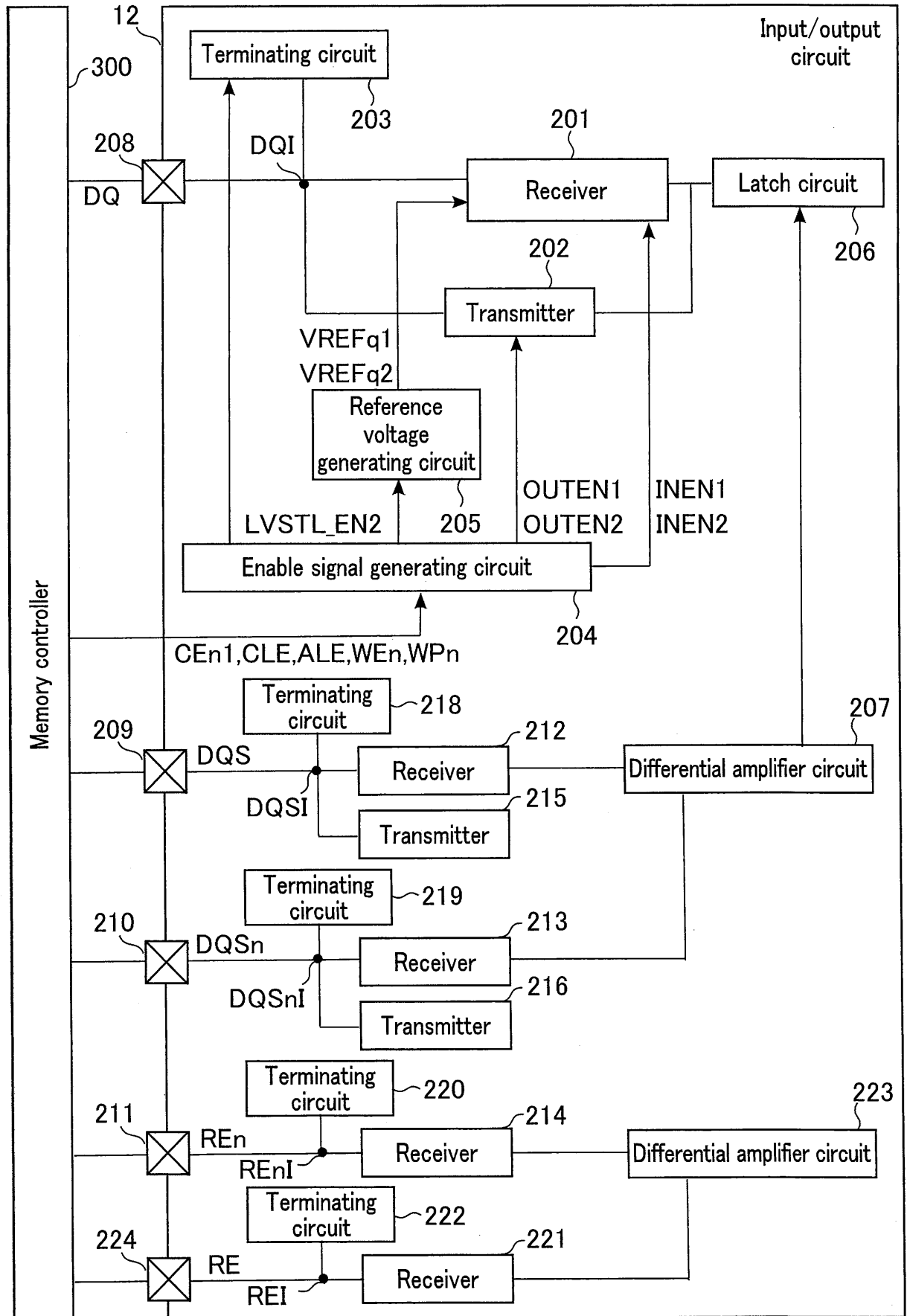


FIG. 6

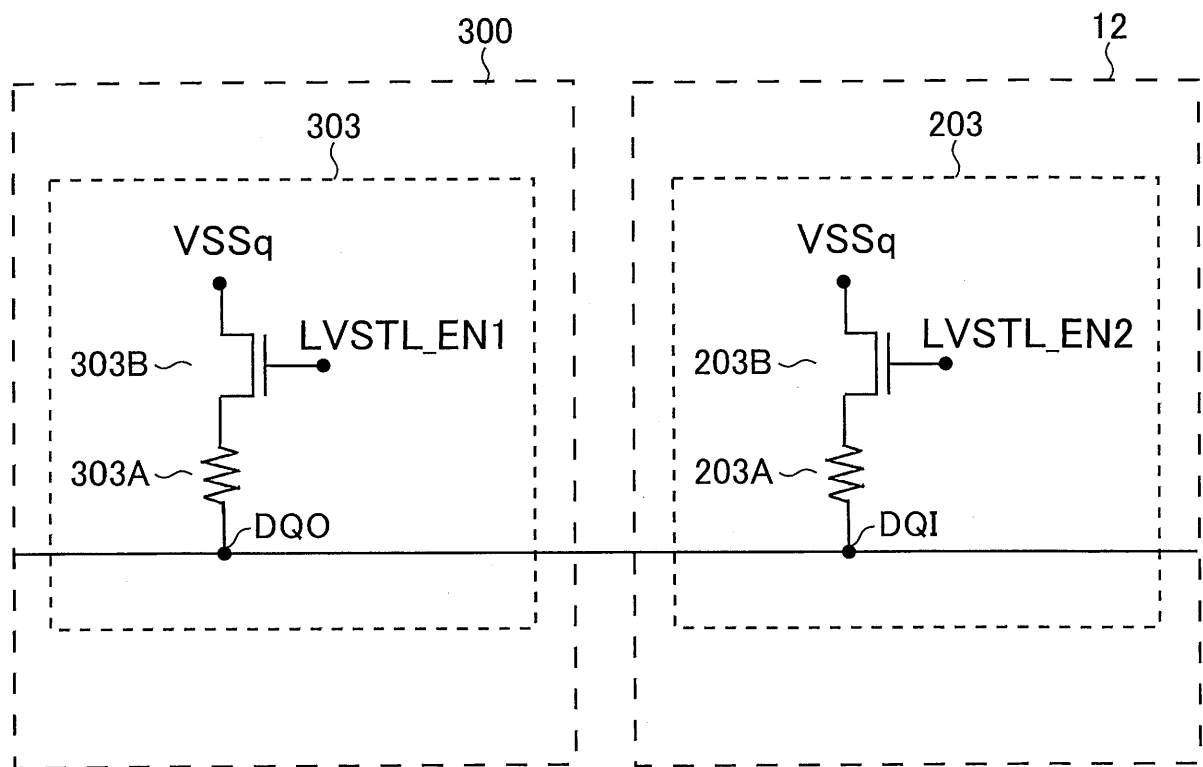


FIG. 7

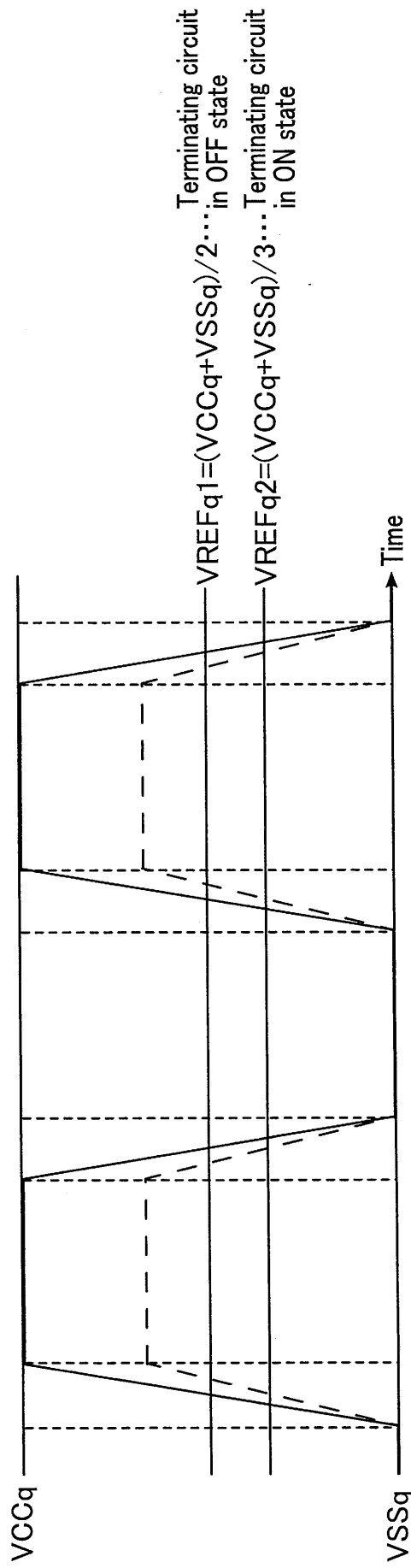


FIG. 8

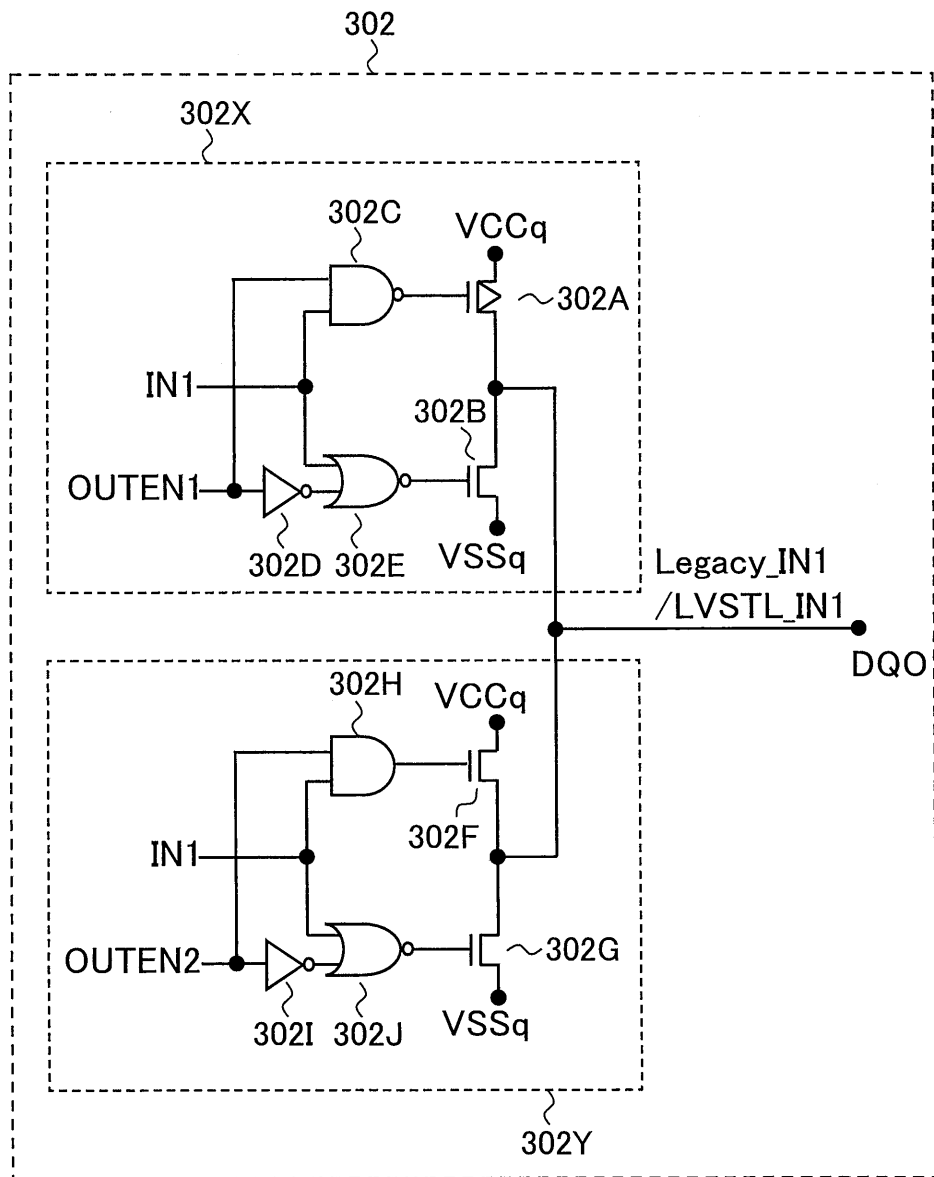


FIG. 9

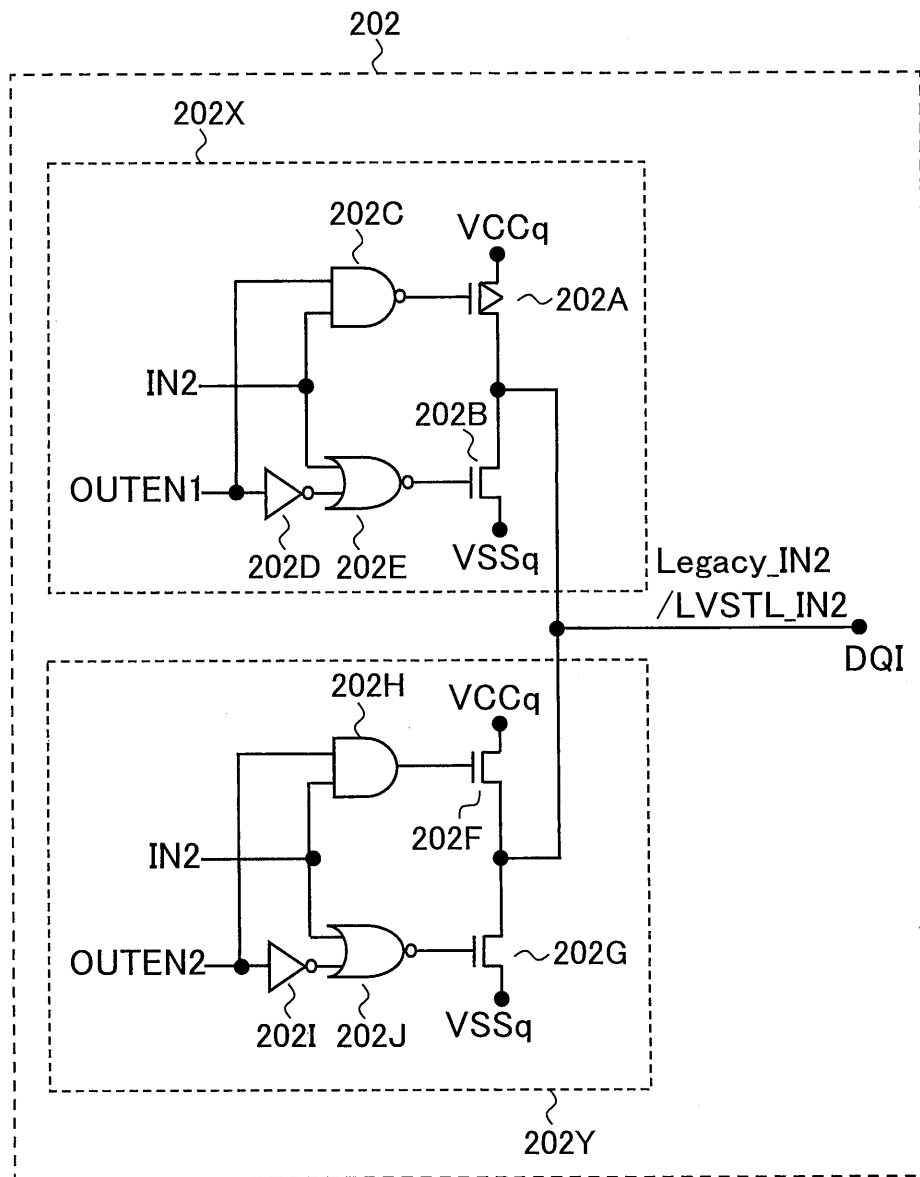


FIG. 10

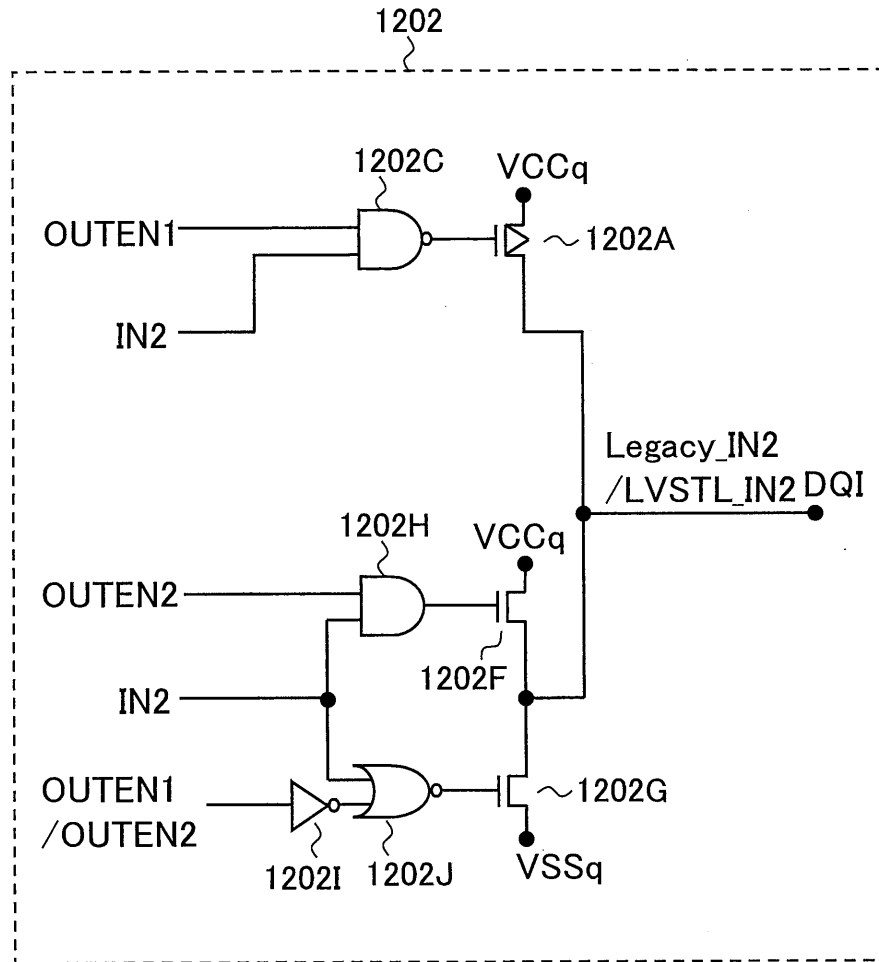


FIG. 11

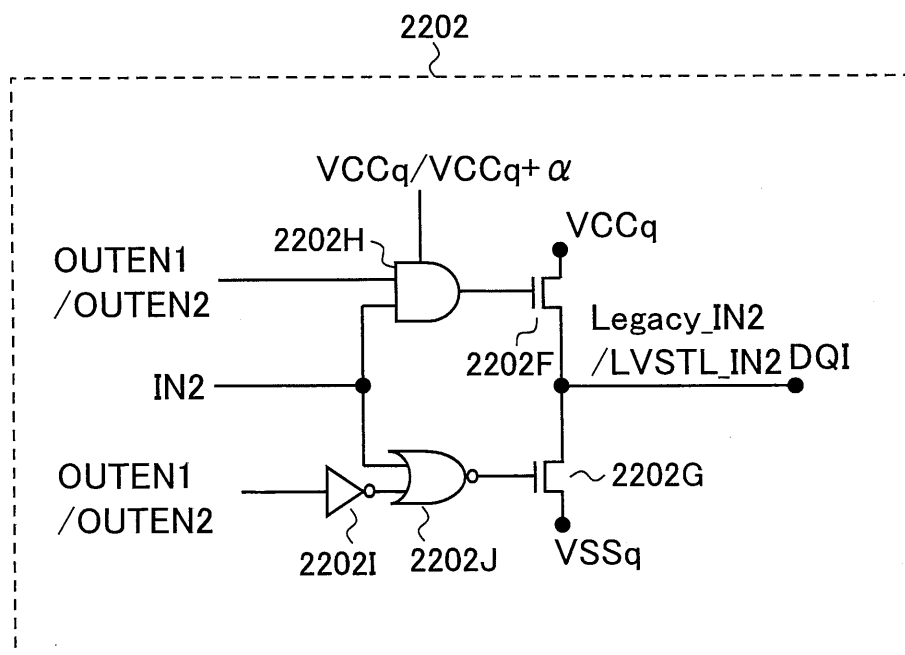


FIG. 12

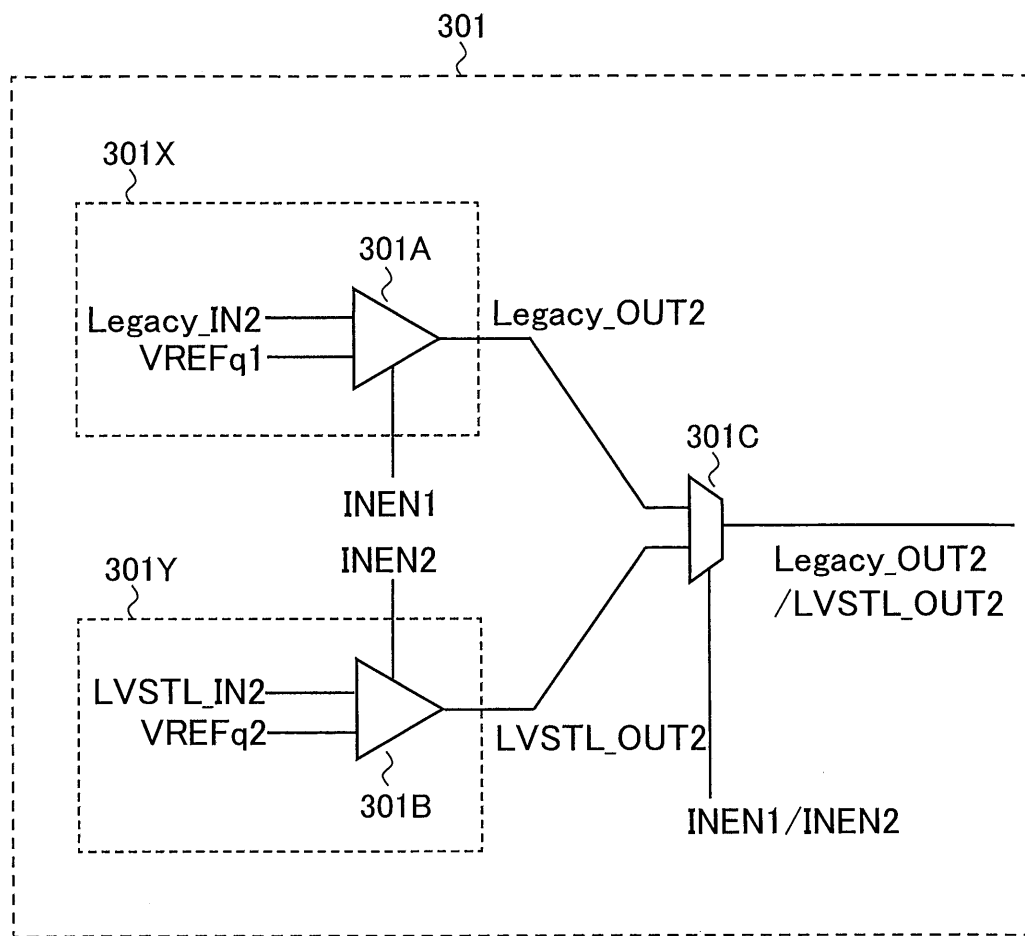


FIG. 13

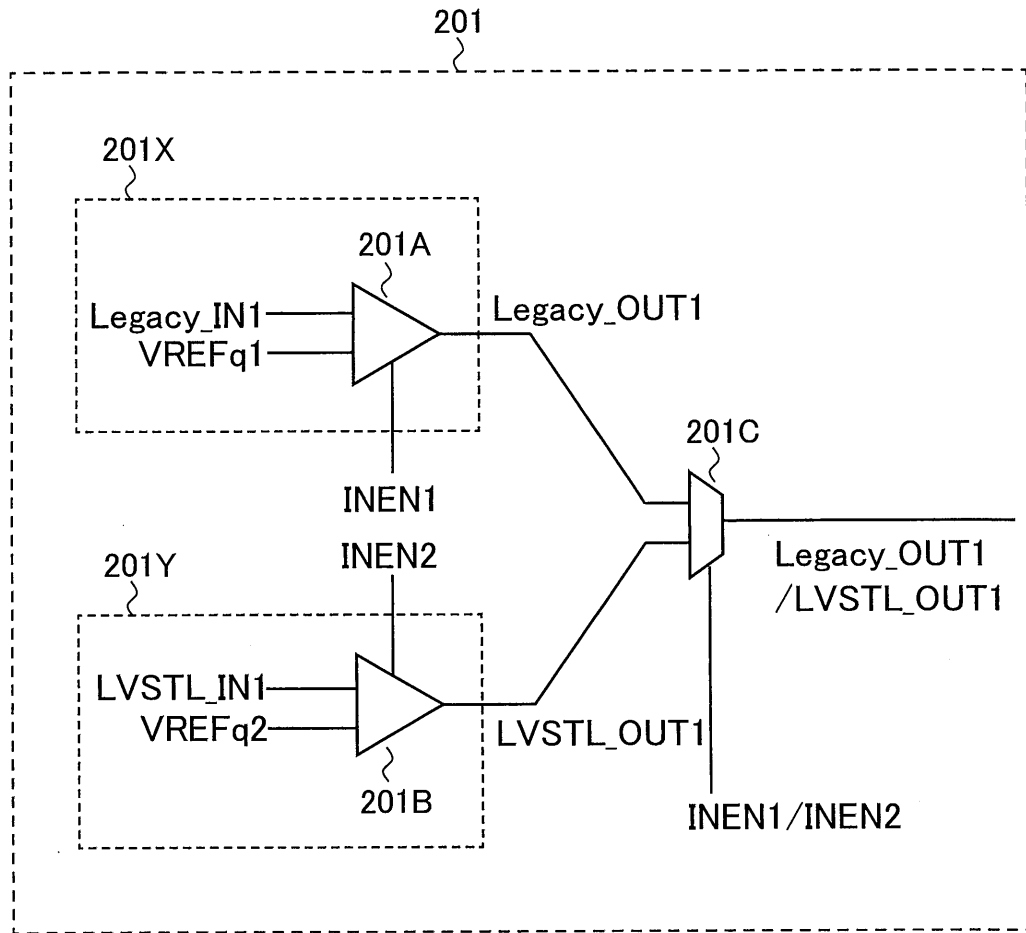


FIG. 14

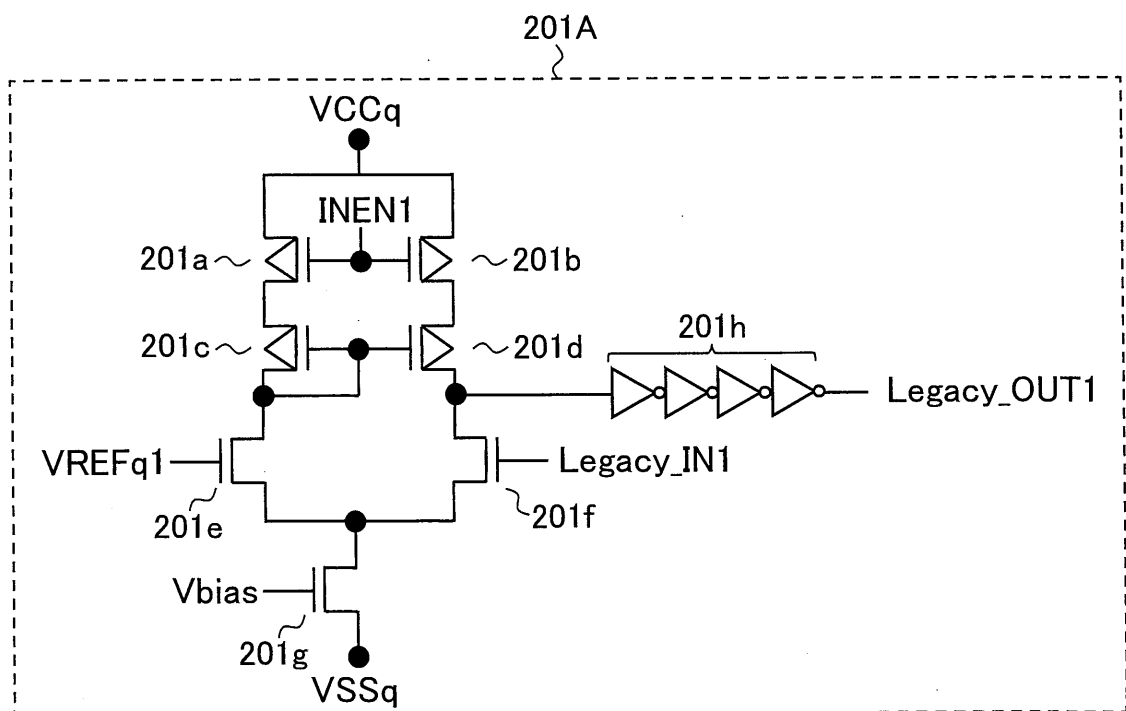


FIG. 15

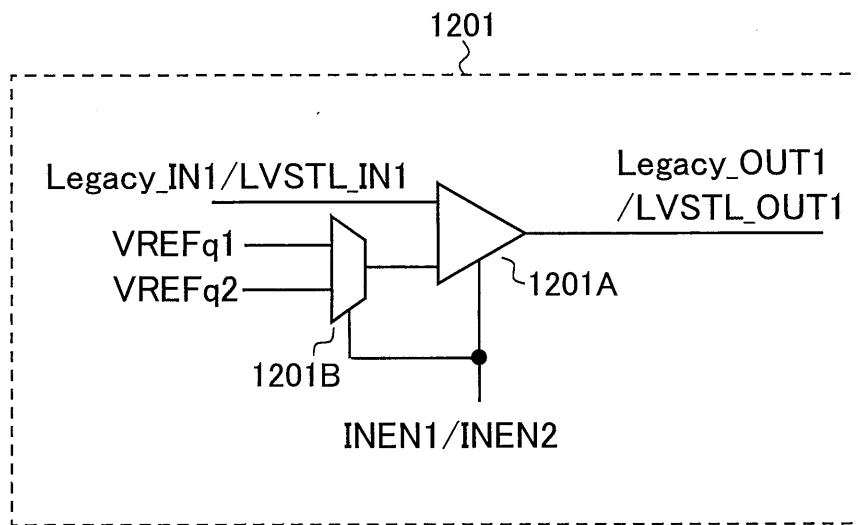


FIG. 16

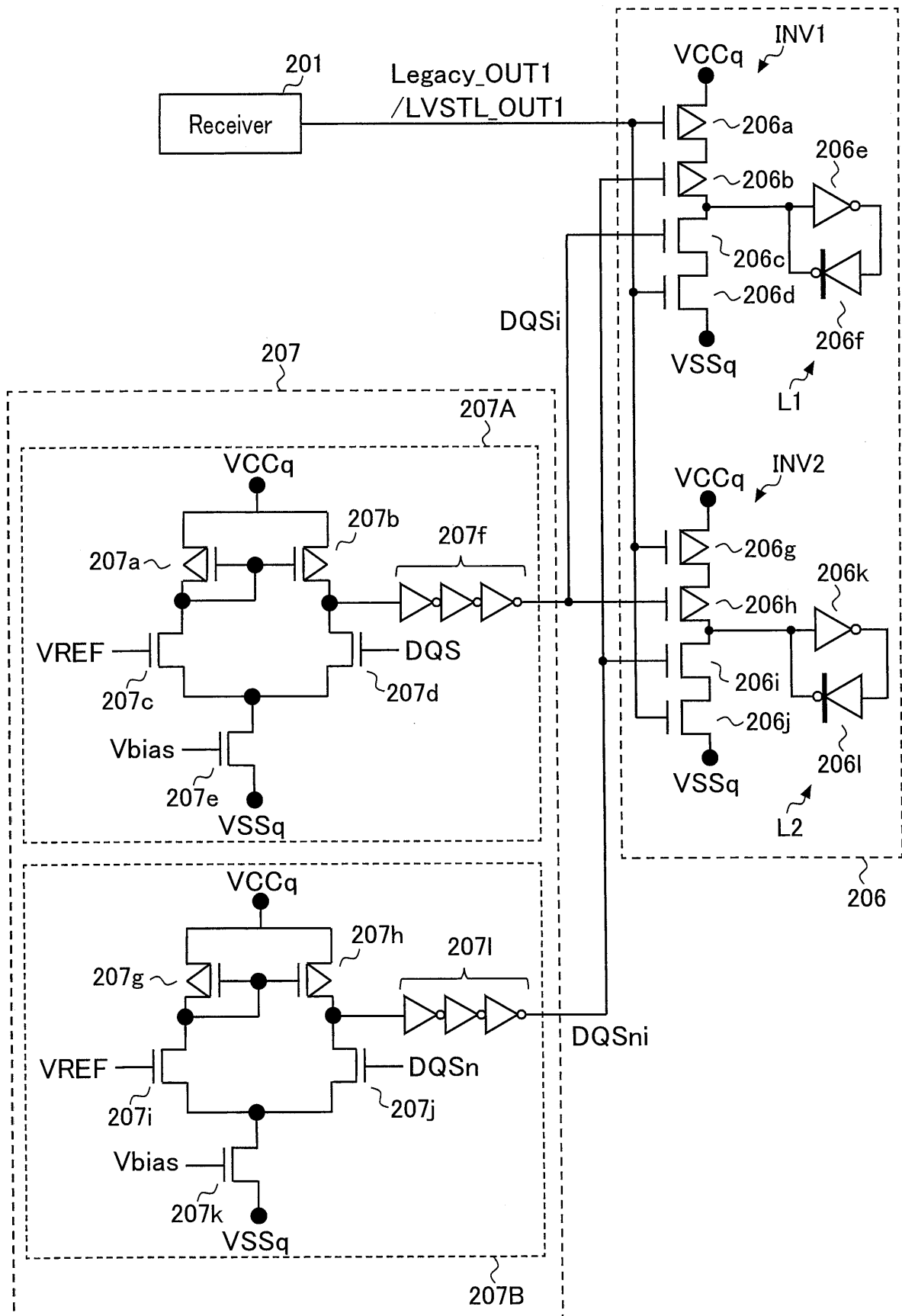


FIG. 17

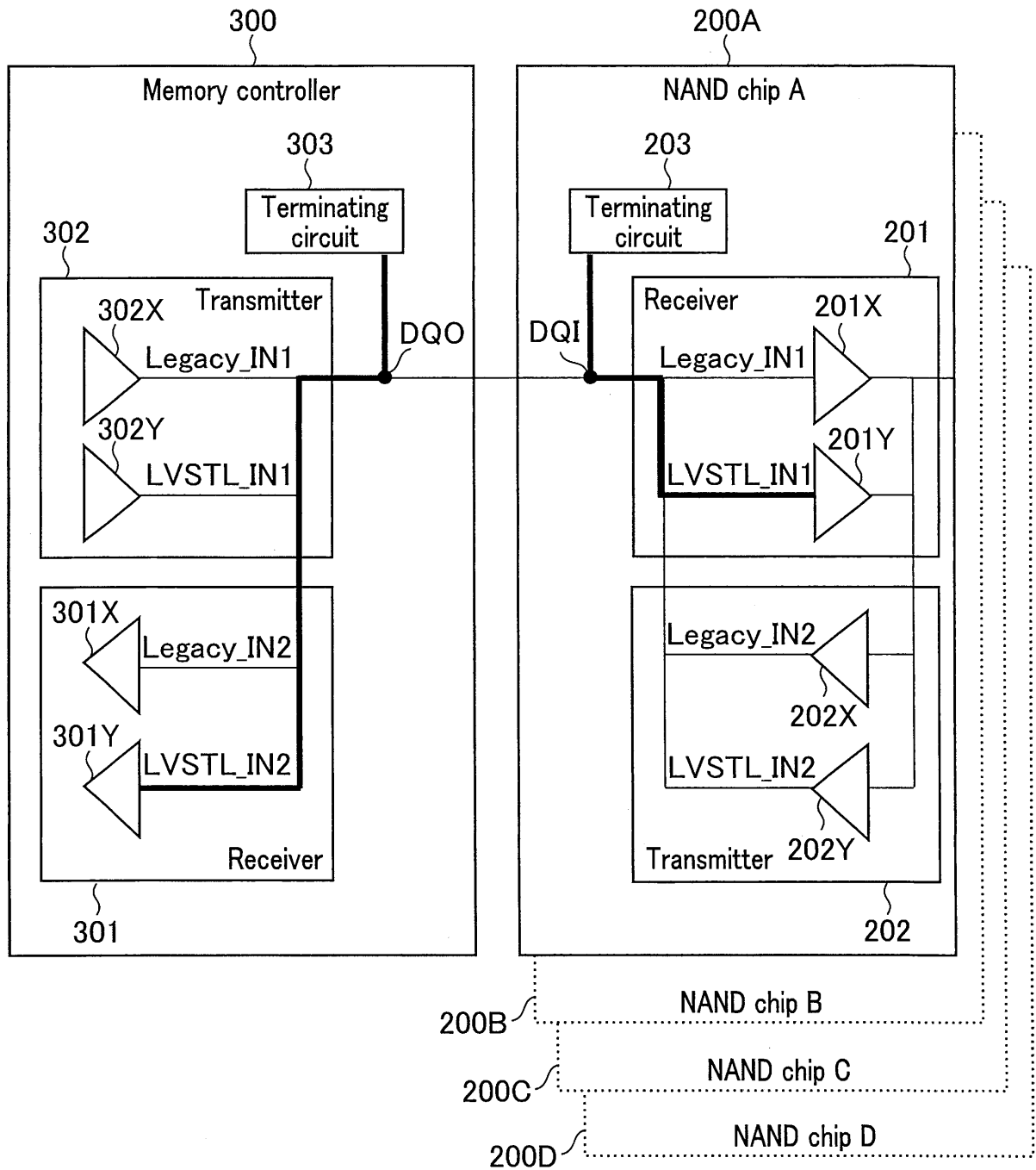


FIG. 18

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN1	Legacy_IN1	Legacy_IN1		
DQS	Fixed at L				
RE	Fixed at L				

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN2	Legacy_IN2			
DQS	Legacy_DQS2	Legacy_DQS2			
RE	Legacy_RE1	Legacy_RE1			

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN2	Legacy_IN2	Legacy_IN2		
DQS	Legacy_DQS2	Legacy_DQS2	Legacy_DQS2		
RE	Legacy_RE1	Legacy_RE1	Legacy_RE1		

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2			
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2			
RE	LVSTL_RE1	LVSTL_RE1, Terminate			

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

FIG. 19

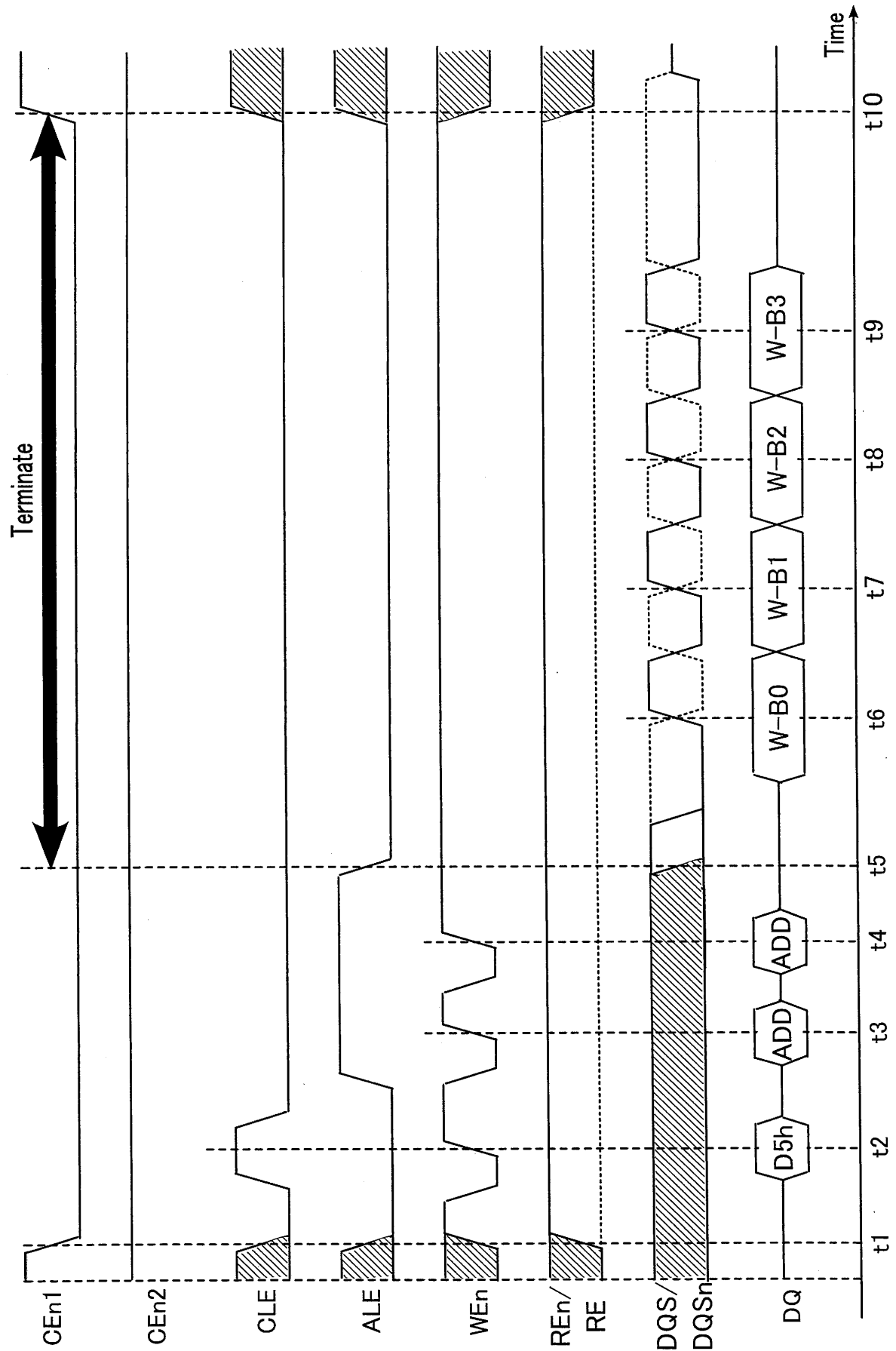


FIG. 20

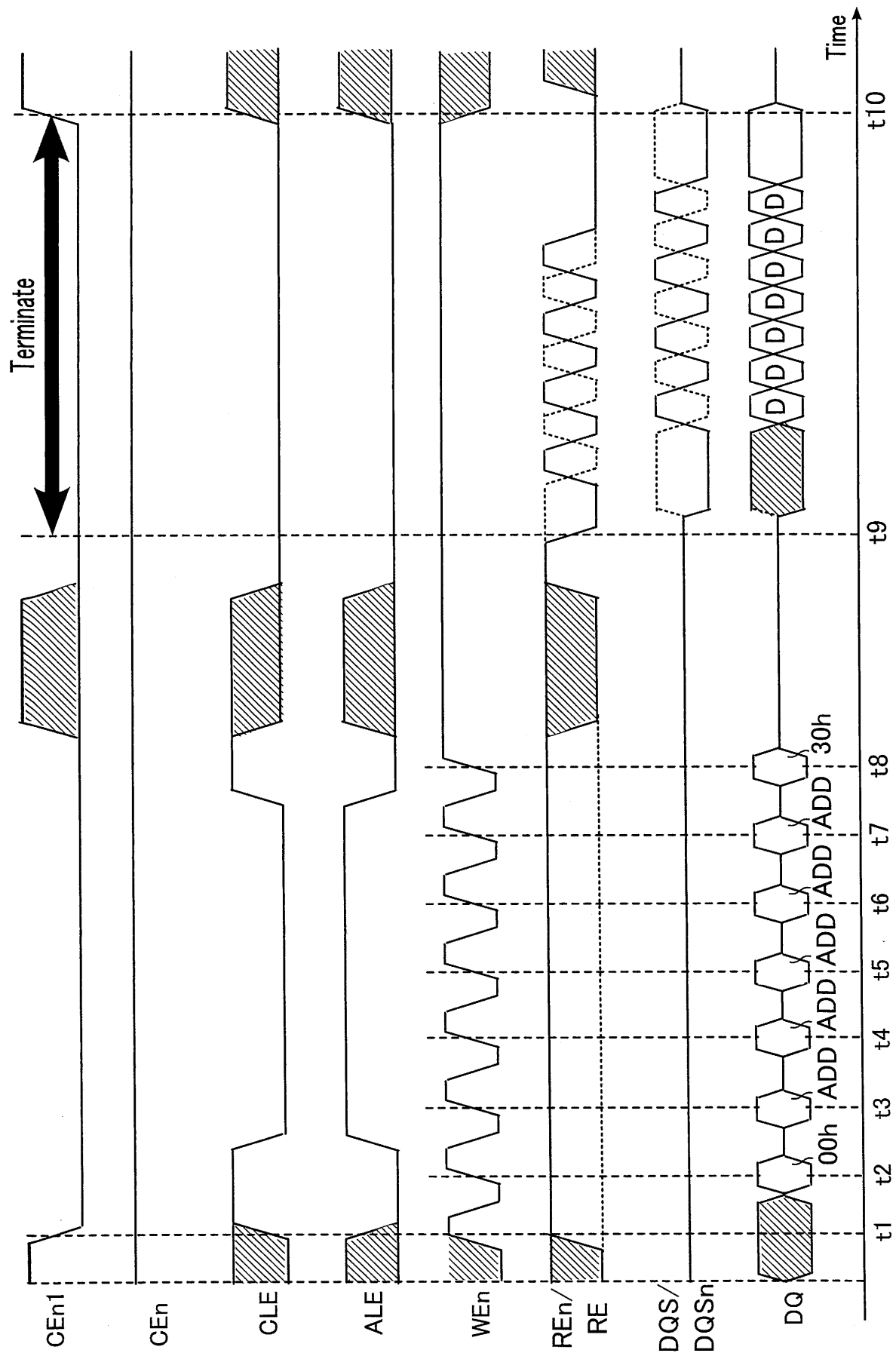


FIG. 21

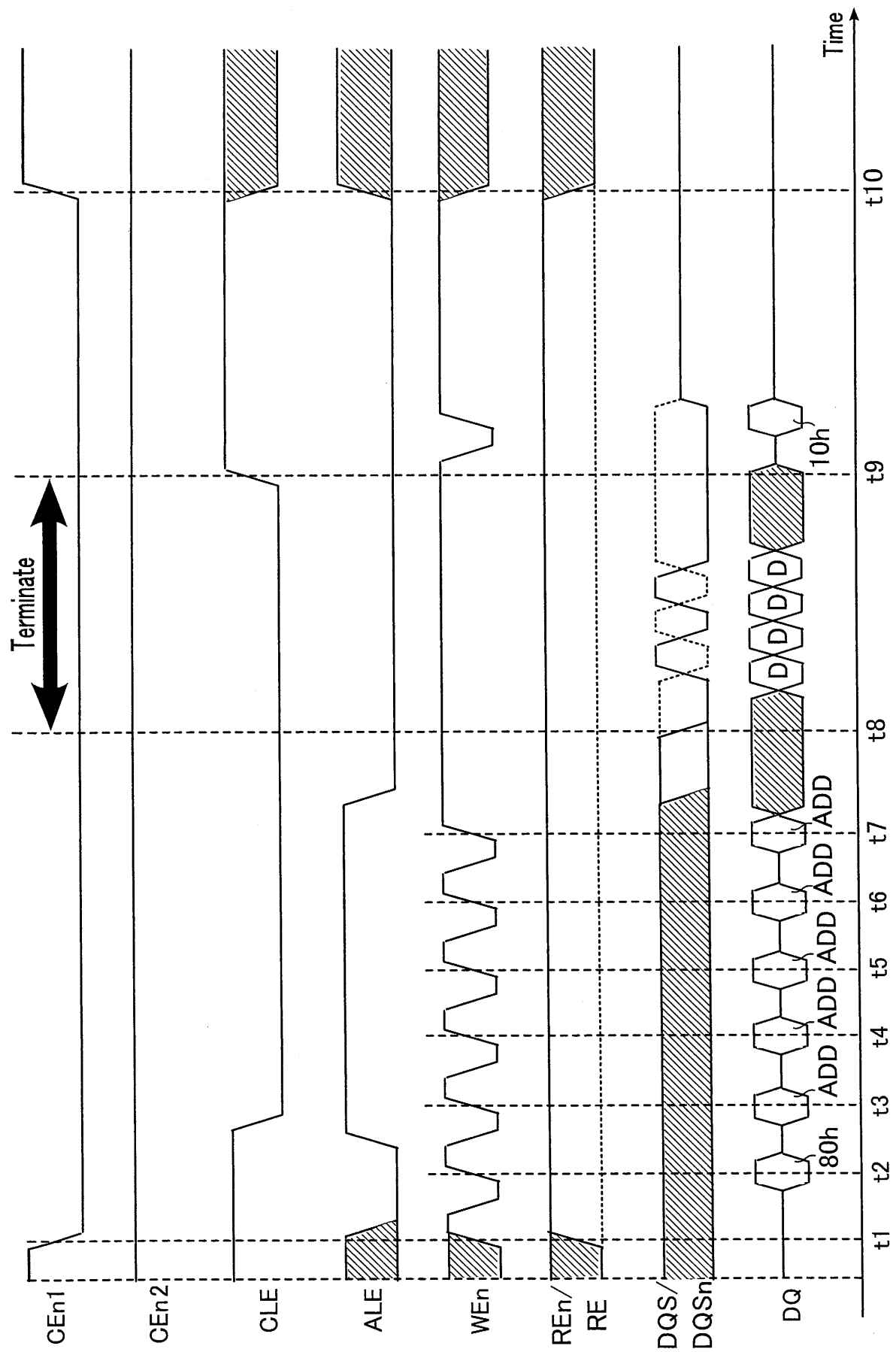


FIG. 22

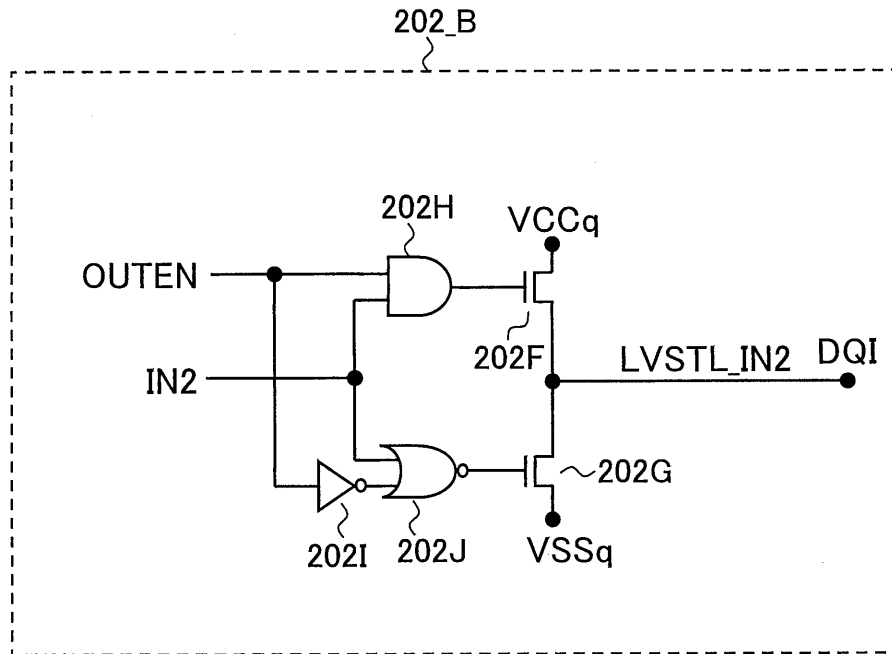


FIG. 23

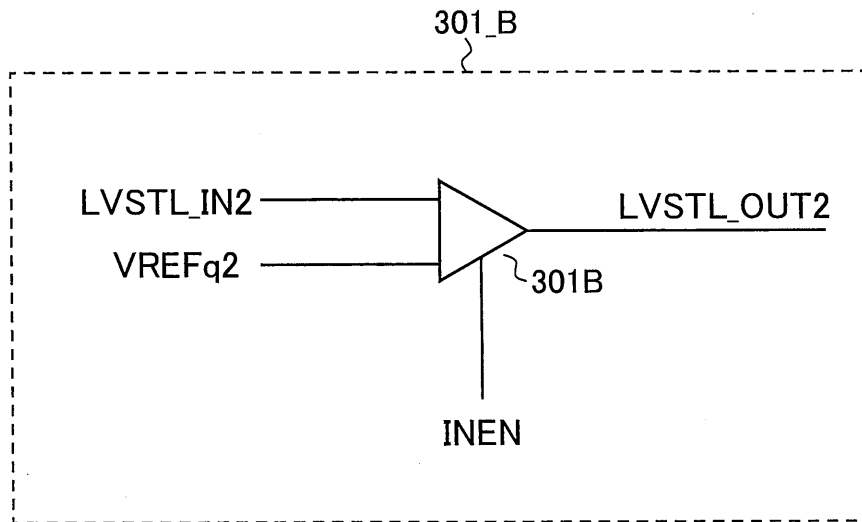


FIG. 24

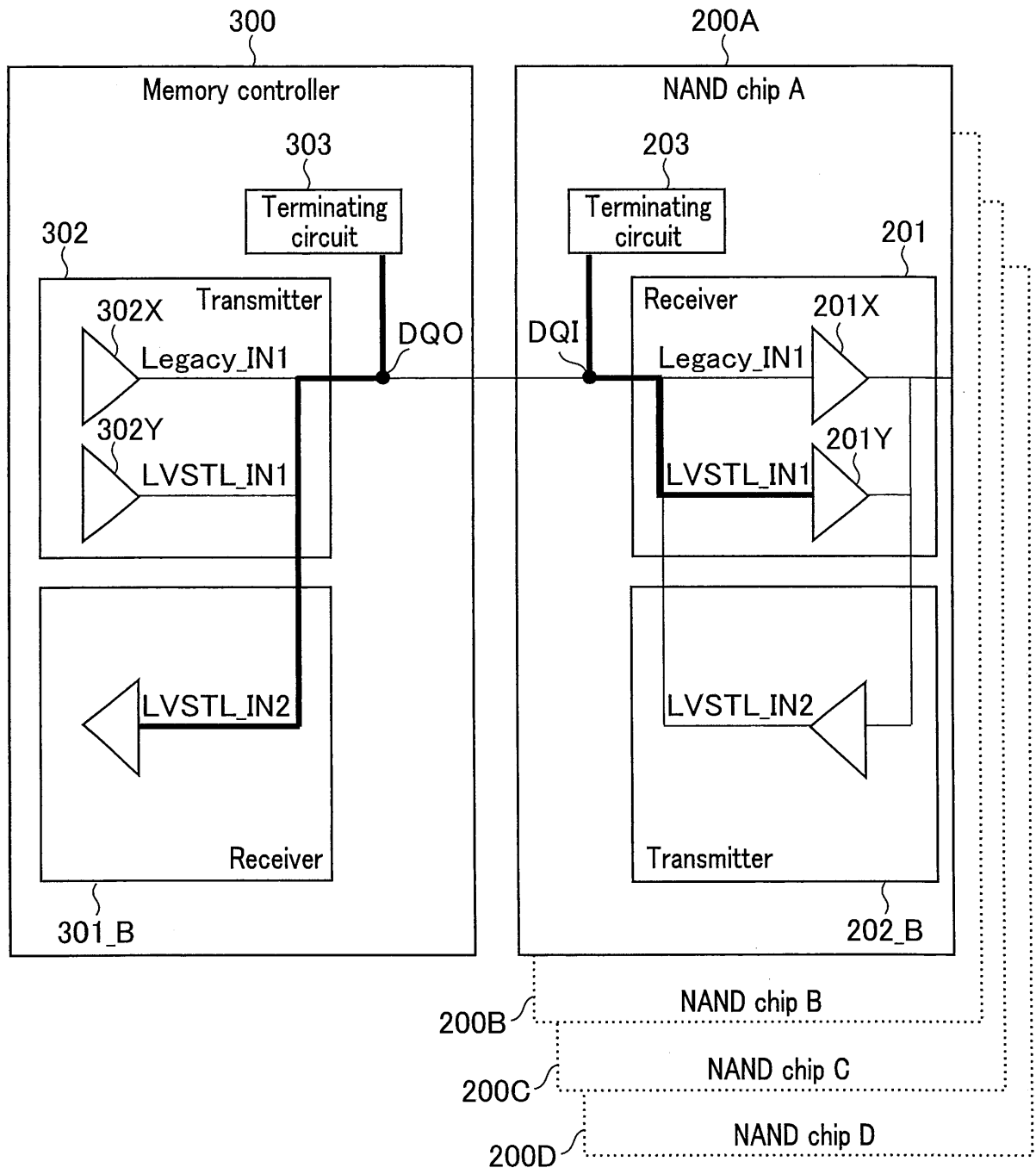


FIG. 25

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN1	Legacy_IN1	Legacy_IN1		
DQS	Fixed at L				
RE	Fixed at L				

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2			
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2			
RE	LVSTL_RE1	LVSTL_RE1, Terminate			

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2	LVSTL_IN2		
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2	LVSTL_DQS2		
RE	Legacy_RE1	Legacy_RE1	Legacy_RE1		

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2			
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2			
RE	LVSTL_RE1	LVSTL_RE1, Terminate			

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

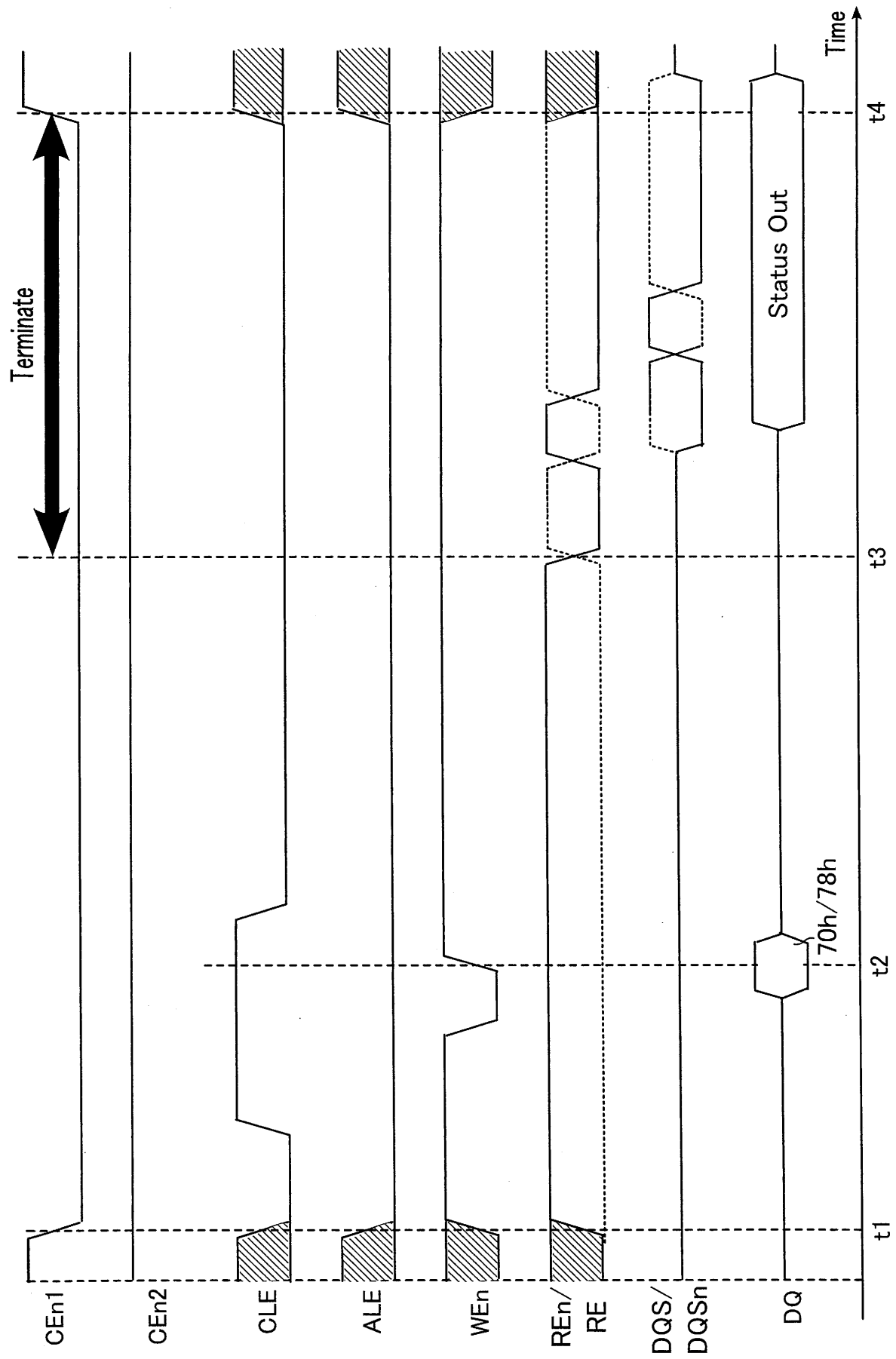


FIG. 27

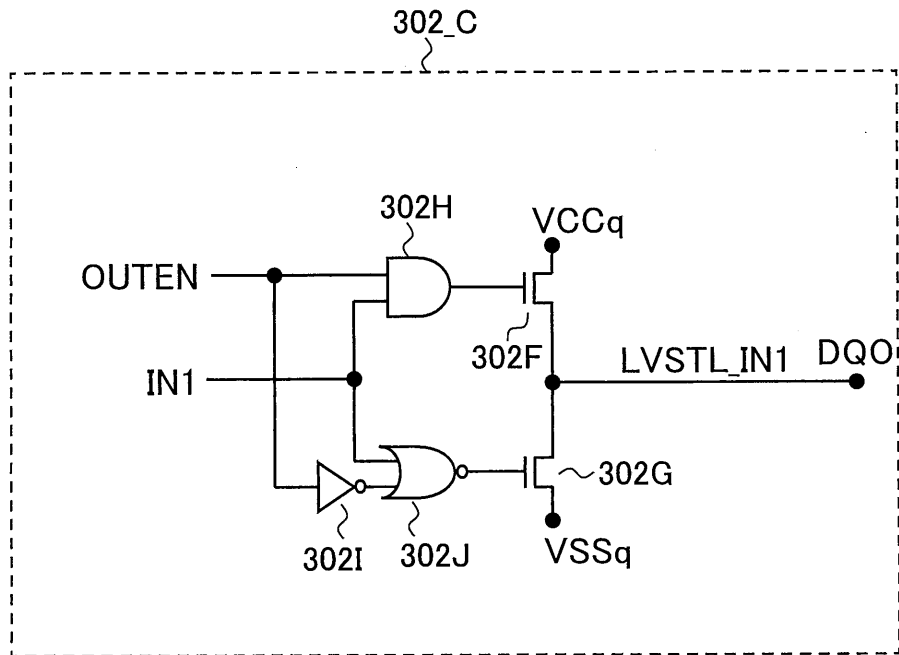


FIG. 28

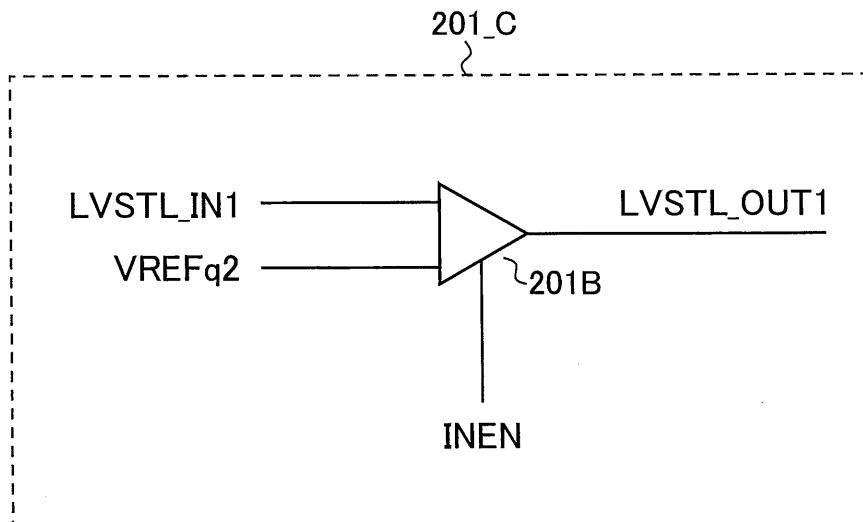


FIG. 29

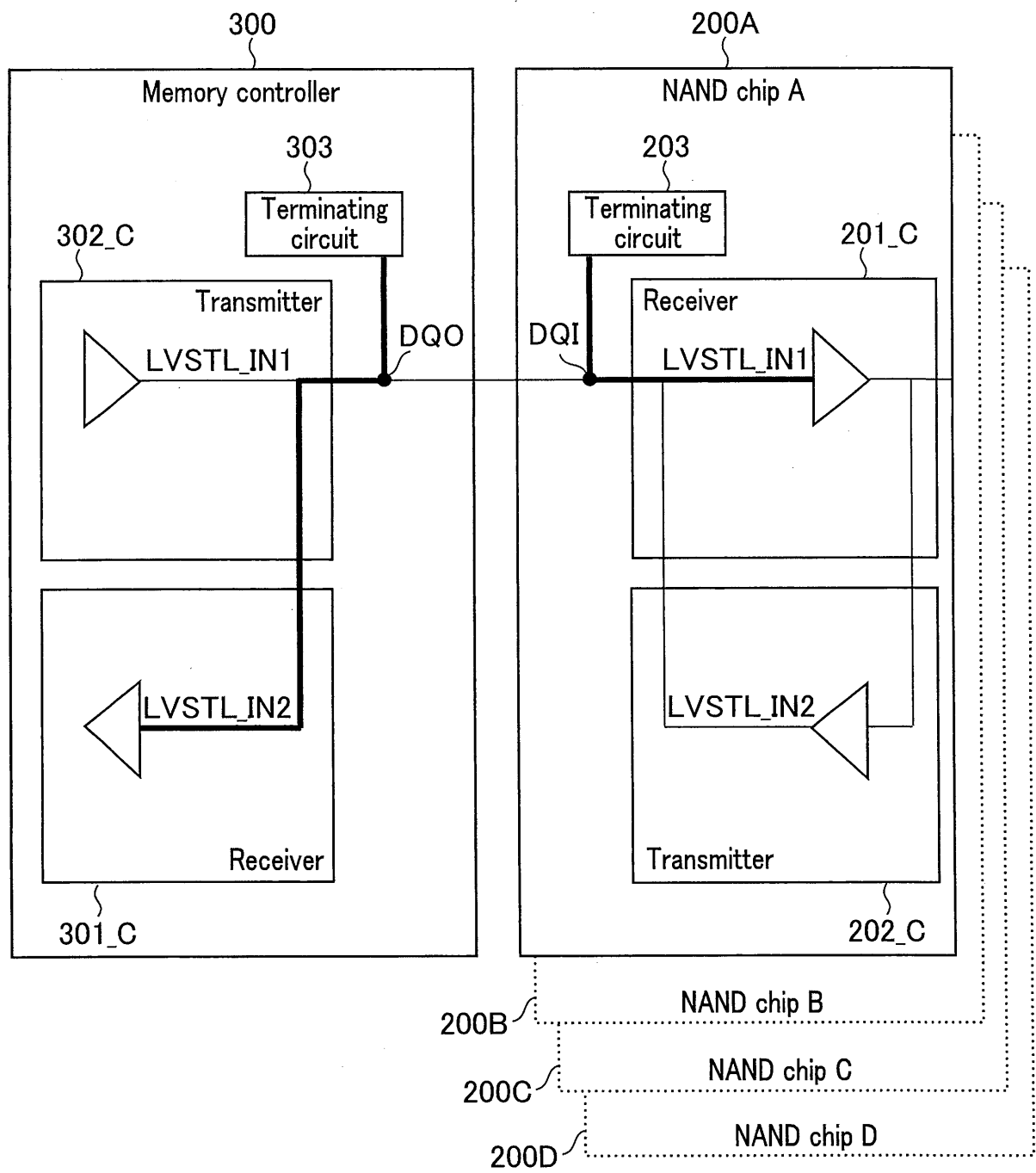


FIG. 30

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate	LVSTL_IN1		
DQS	Fixed at L				
RE	Fixed at L				

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2			
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2			
RE	LVSTL_RE1	LVSTL_RE1, Terminate			

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2	LVSTL_IN2		
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2	LVSTL_DQS2		
RE	LVSTL_RE1	LVSTL_RE1, Terminate	LVSTL_RE1		

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2, Terminate	LVSTL_IN2			
DQS	LVSTL_DQS2, Terminate	LVSTL_DQS2			
RE	LVSTL_RE1	LVSTL_RE1, Terminate			

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1, Terminate			
DQS	LVSTL_DQS1	LVSTL_DQS1, Terminate			
RE	Fixed at L				

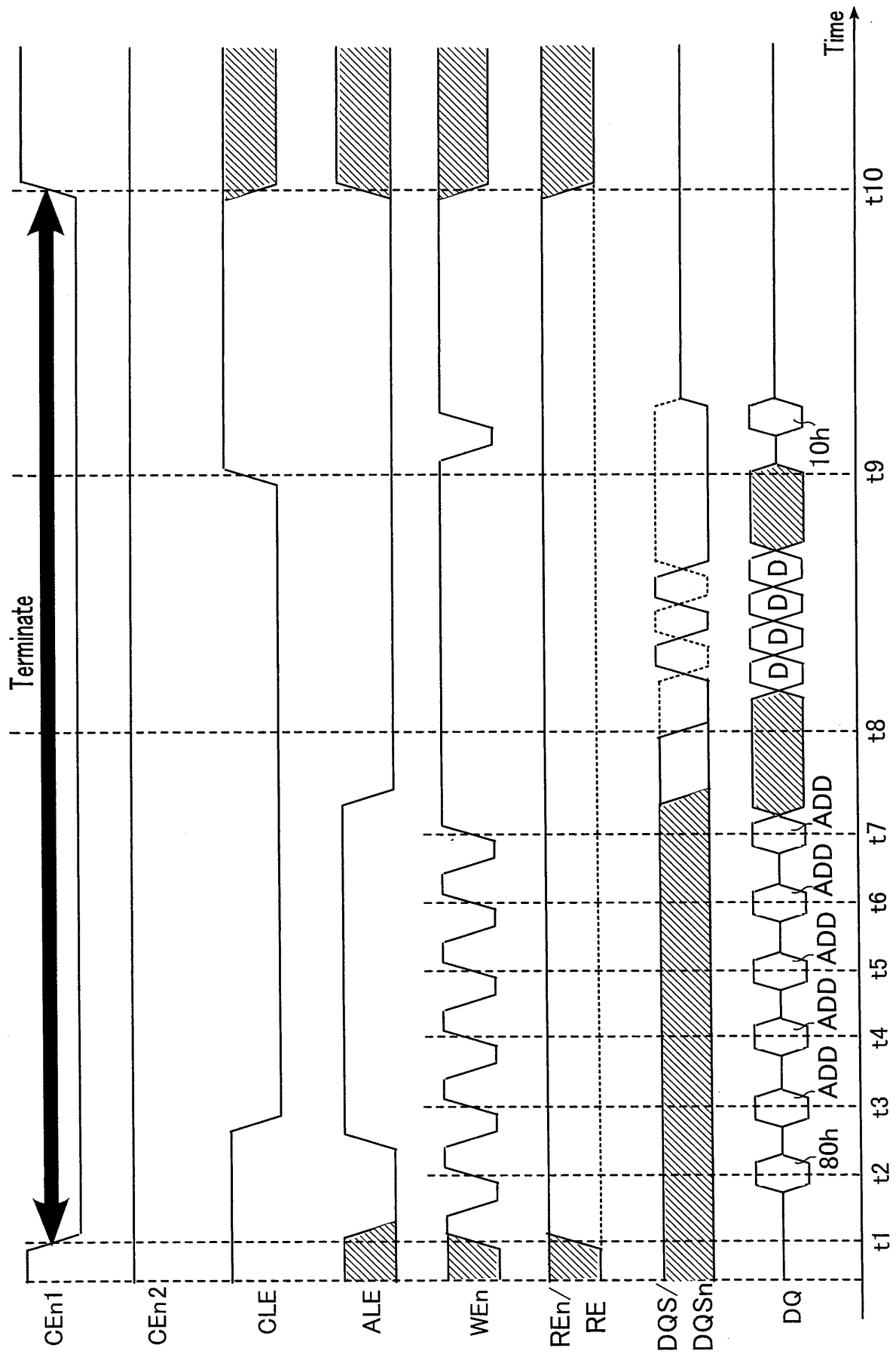


FIG. 32

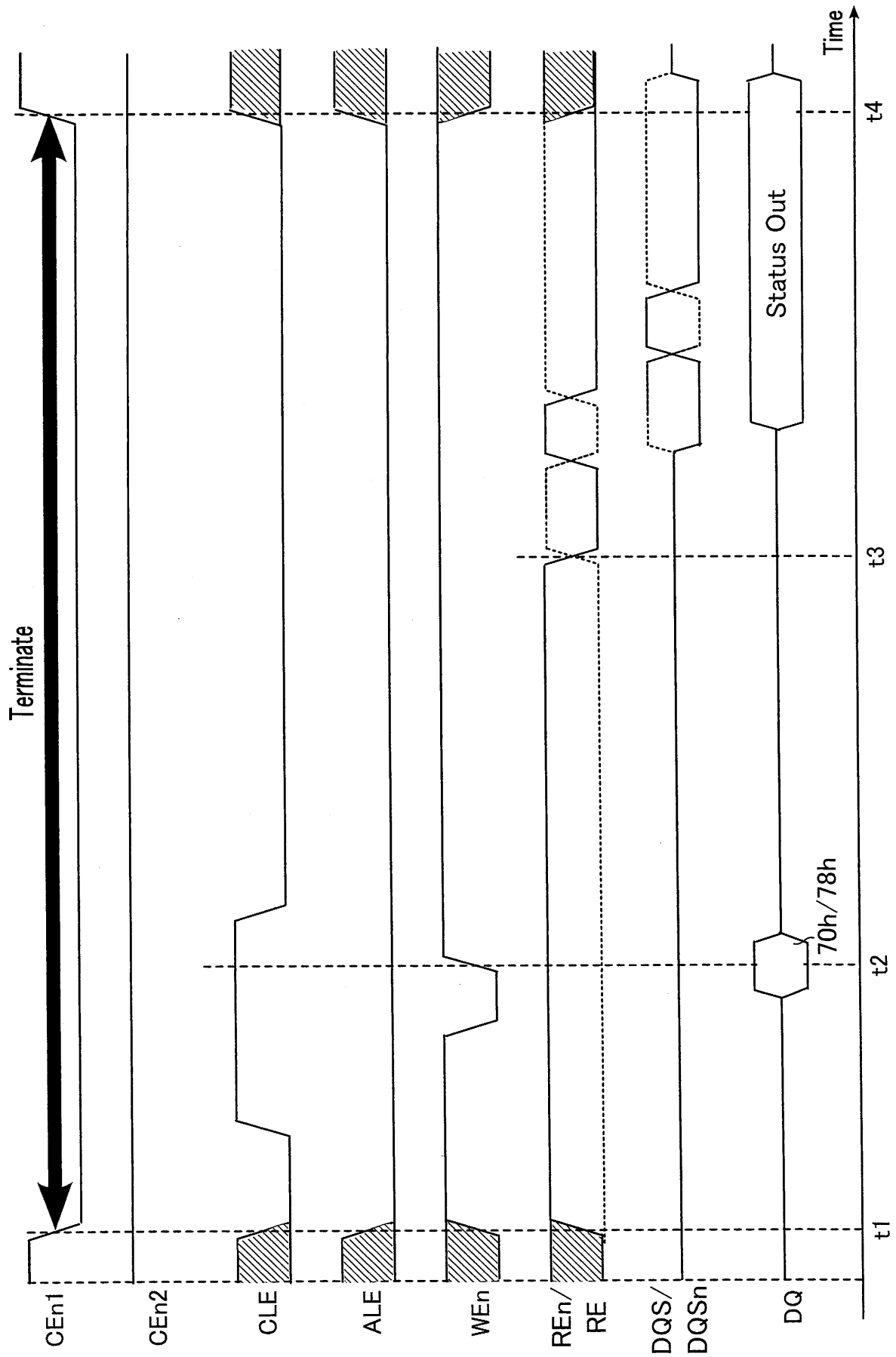


FIG. 33

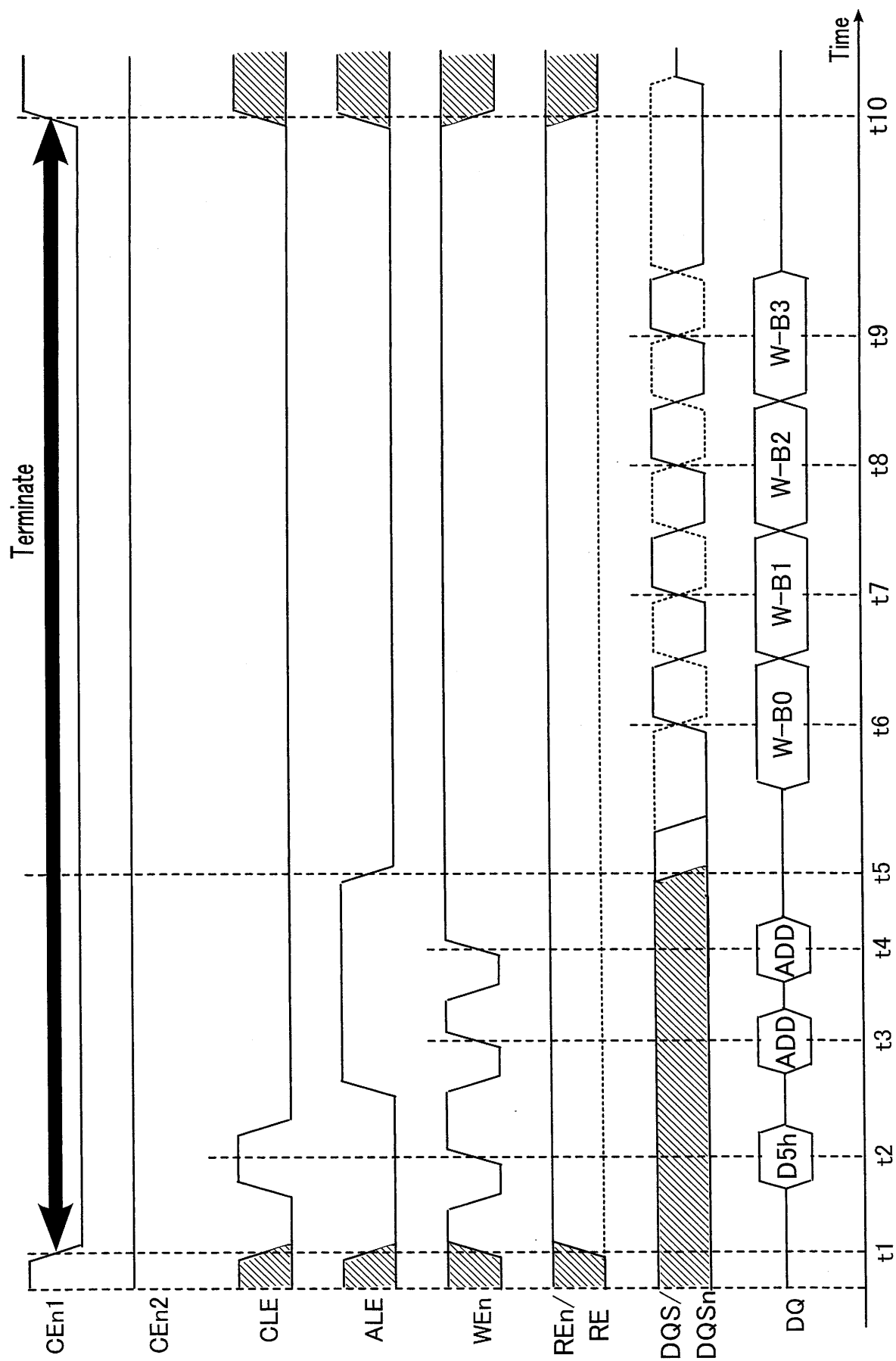


FIG. 34

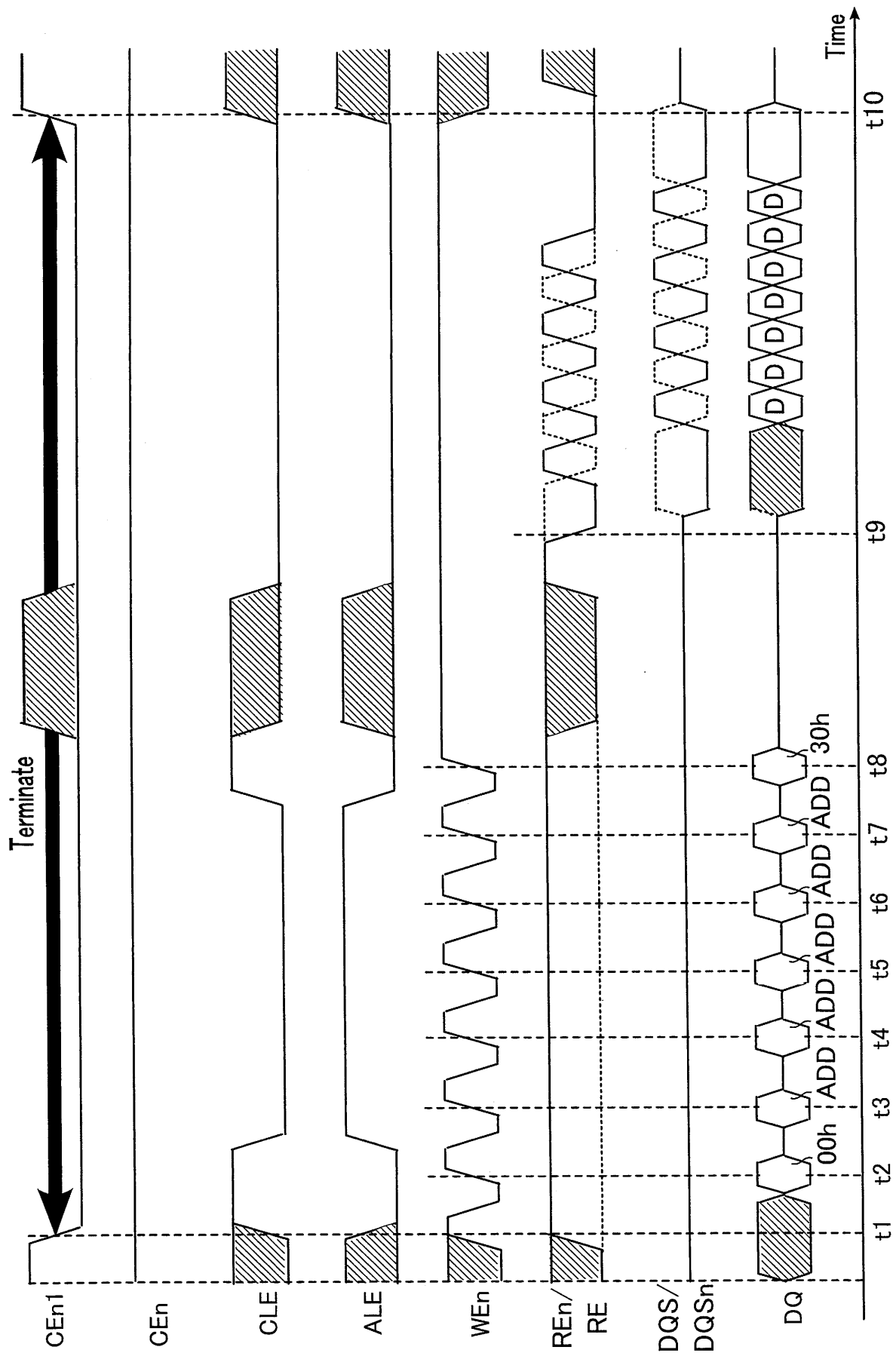


FIG. 35

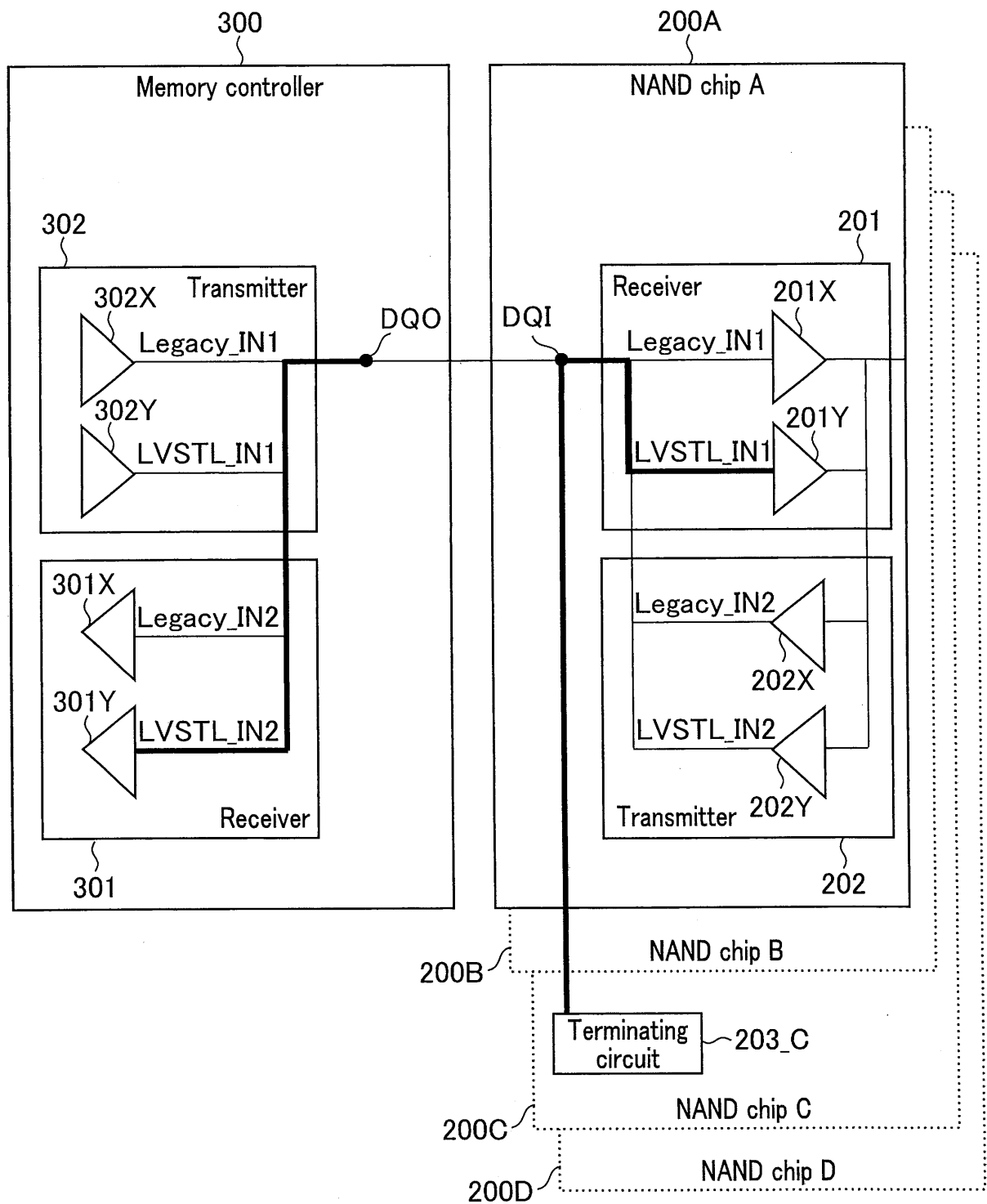


FIG. 36

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN1	Legacy_IN1	Legacy_IN1		
DQS	Fixed at L				
RE	Fixed at L				

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN2	Legacy_IN2			
DQS	Legacy_DQS2	Legacy_DQS2			
RE	Legacy_RE1	Legacy_RE1			

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN2	Legacy_IN2	Legacy_IN2		
DQS	Legacy_DQS2	Legacy_DQS2	Legacy_DQS2		
RE	Legacy_RE1	Legacy_RE1	Legacy_RE1		

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	Fixed at L				

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2		Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2		Terminate	
RE	LVSTL_RE1	LVSTL_RE1		Terminate	

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	Fixed at L				

FIG. 37

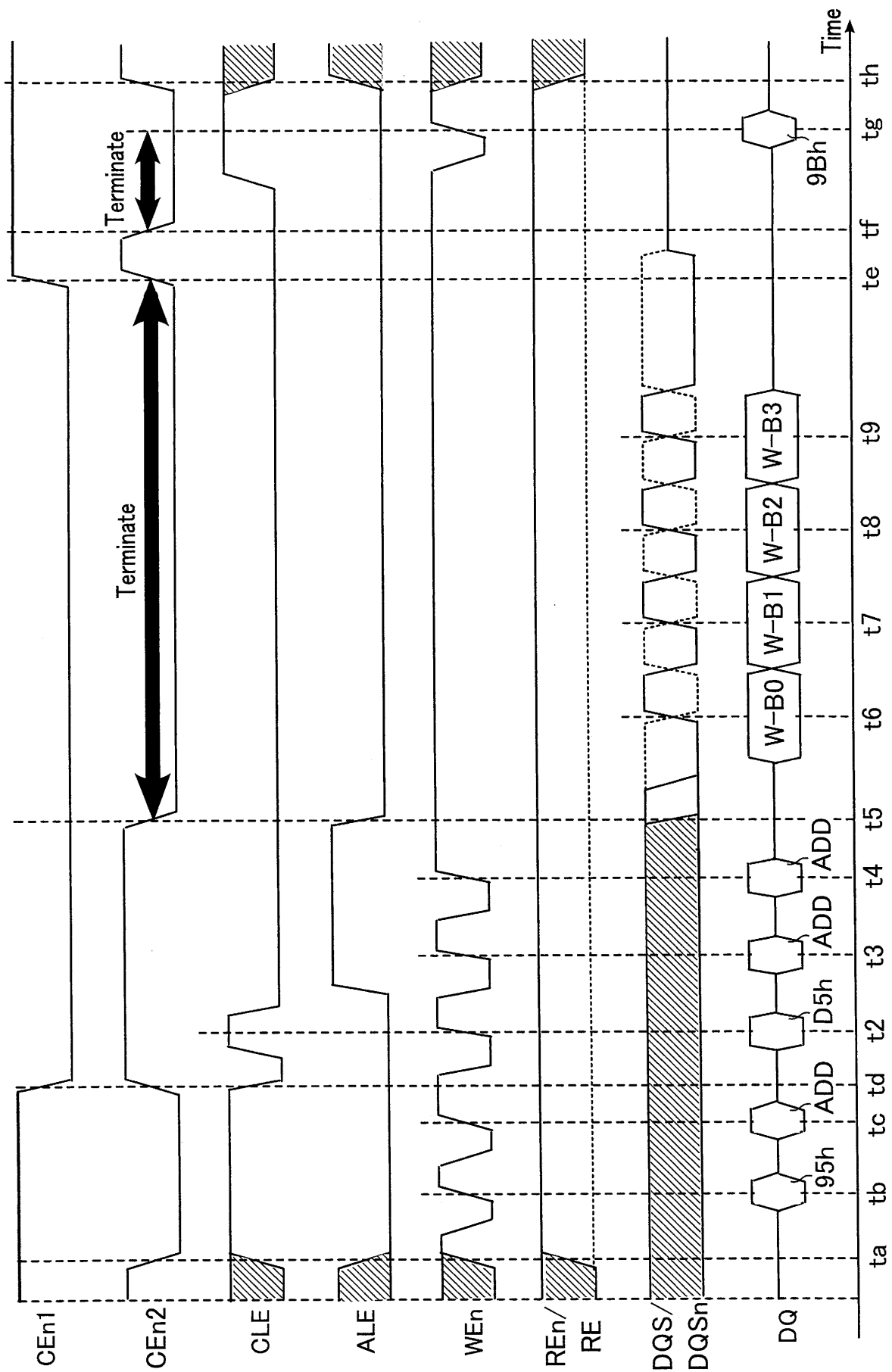


FIG. 38

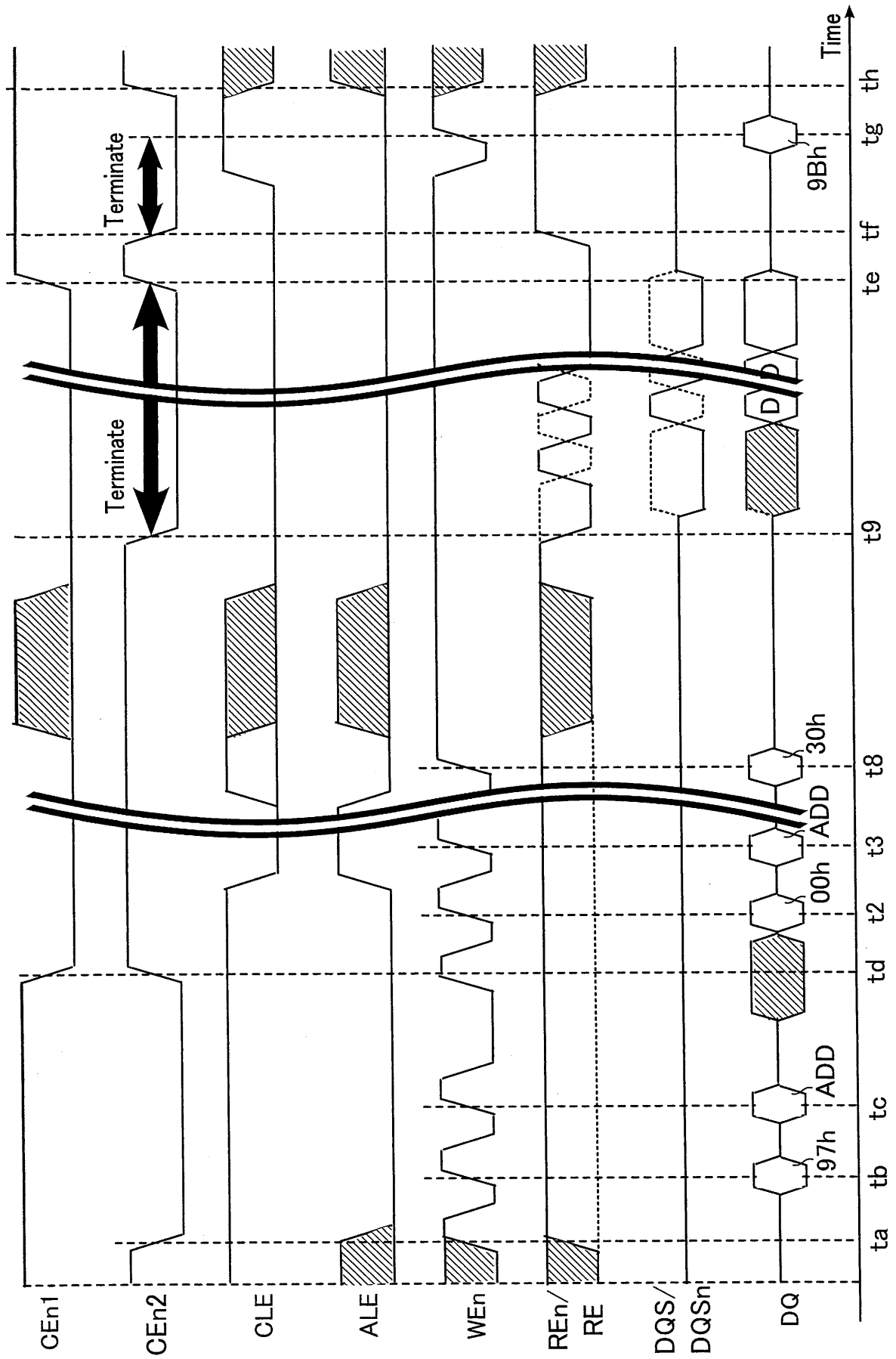


FIG. 39

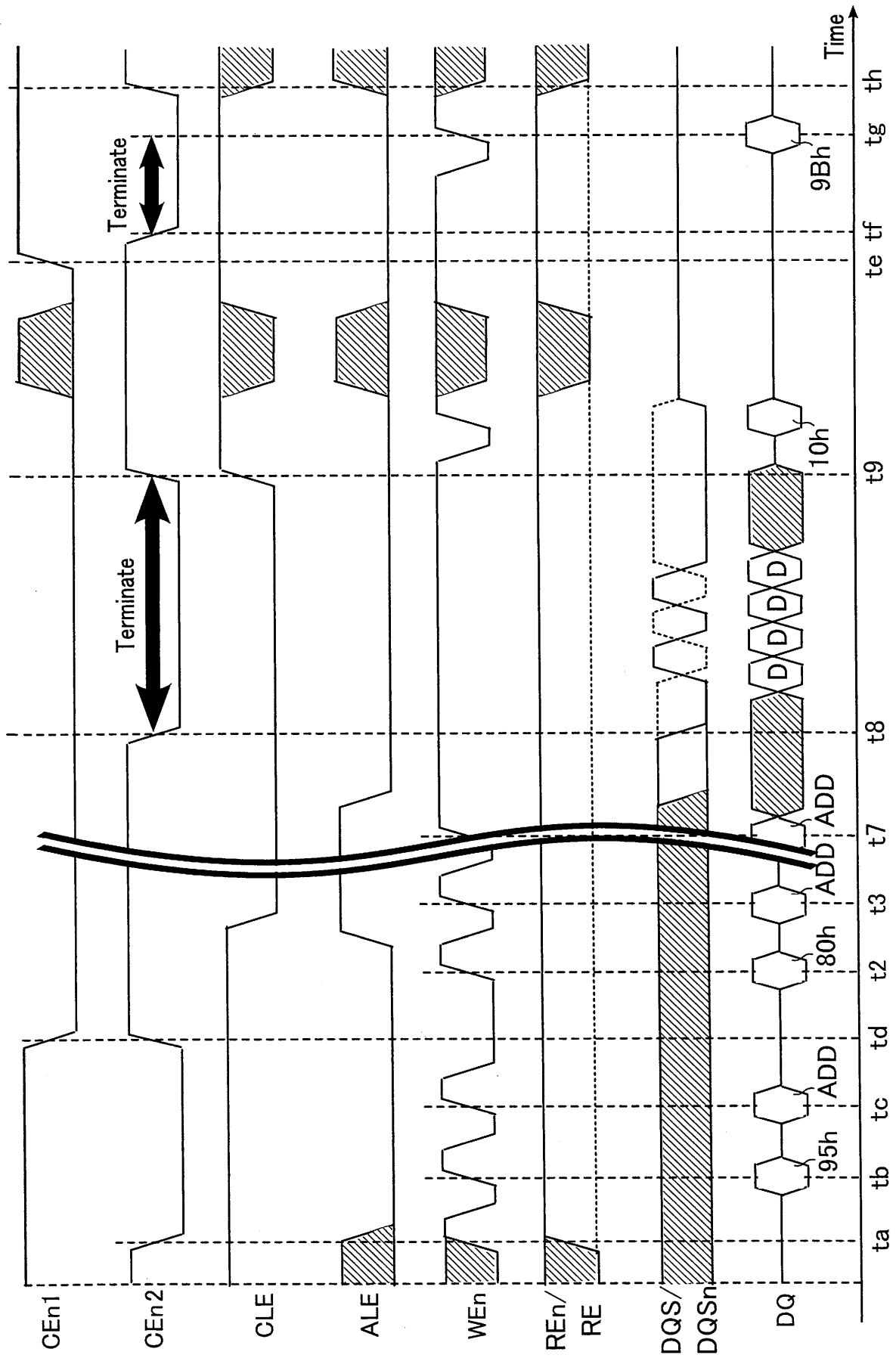


FIG. 40

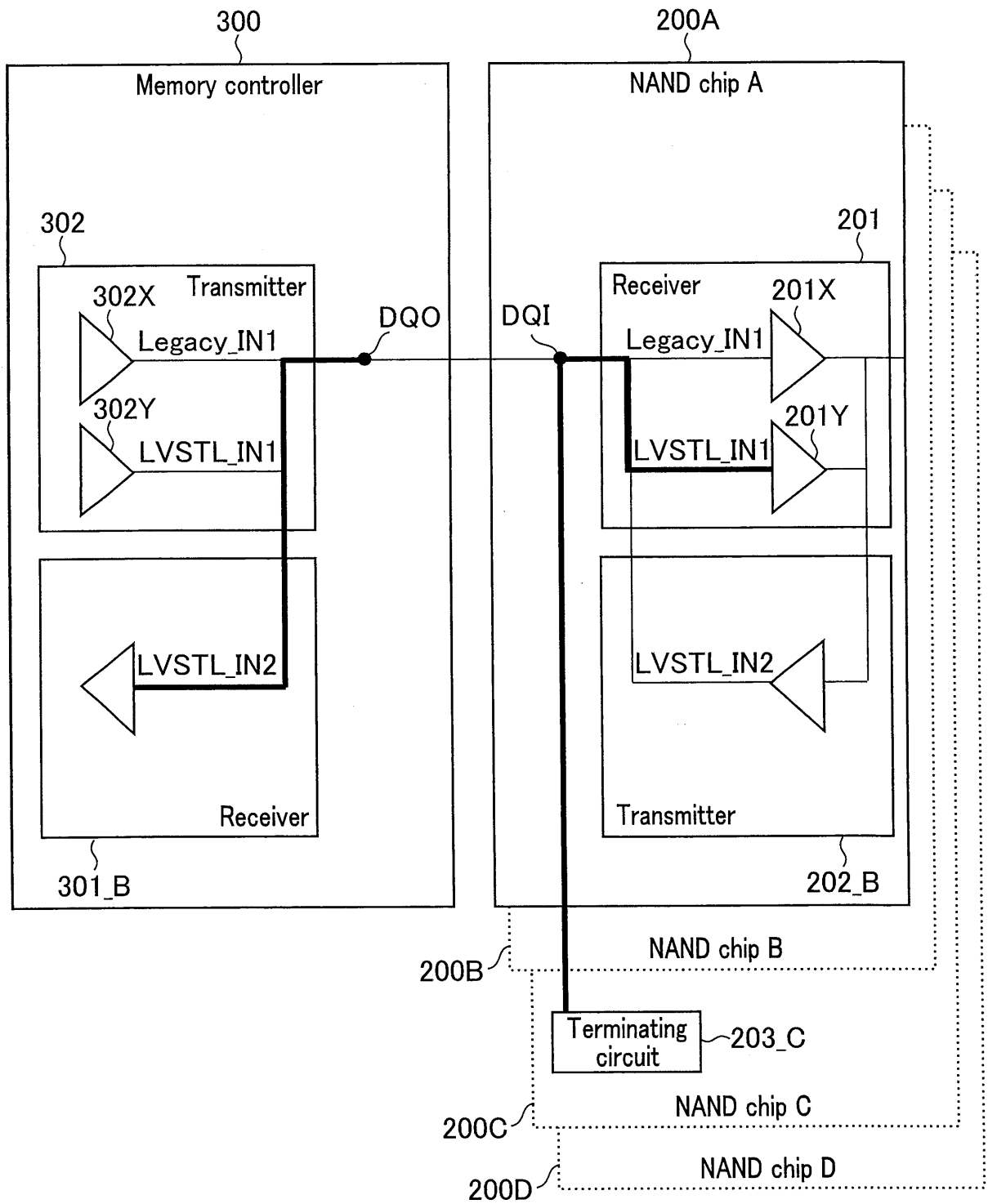


FIG. 41

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	Legacy_IN1	Legacy_IN1	Legacy_IN1		
DQS	Fixed at L				
RE	Fixed at L				

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2		Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2		Terminate	
RE	LVSTL_RE1	LVSTL_RE1		Terminate	

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2	LVSTL_IN2	Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2	LVSTL_DQS2	Terminate	
RE	LVSTL_RE1	LVSTL_RE1	LVSTL_RE1	Terminate	

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	Fixed at L				

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2		Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2		Terminate	
RE	LVSTL_RE1	LVSTL_RE1		Terminate	

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	Fixed at L				

FIG. 42

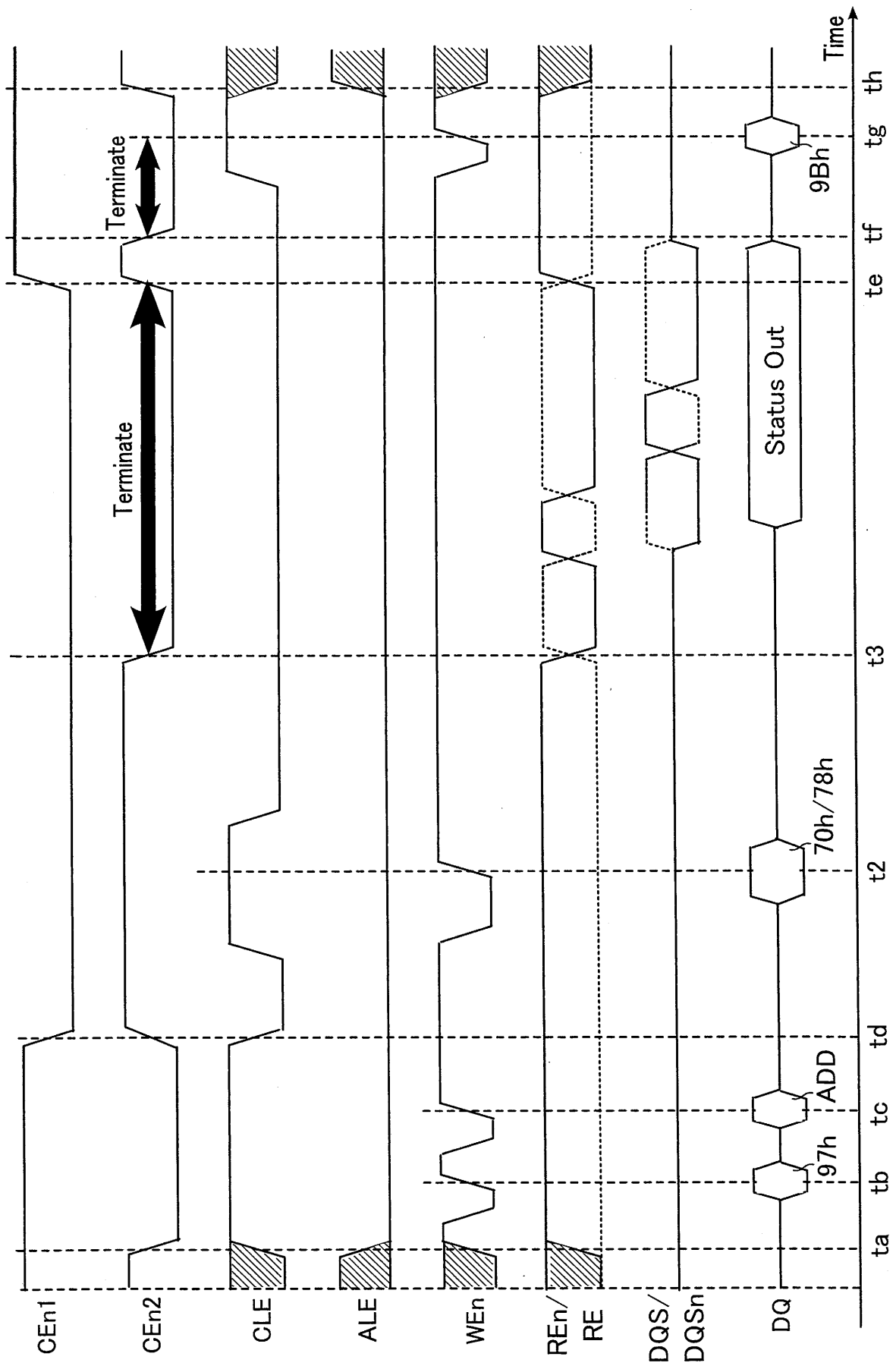


FIG. 43

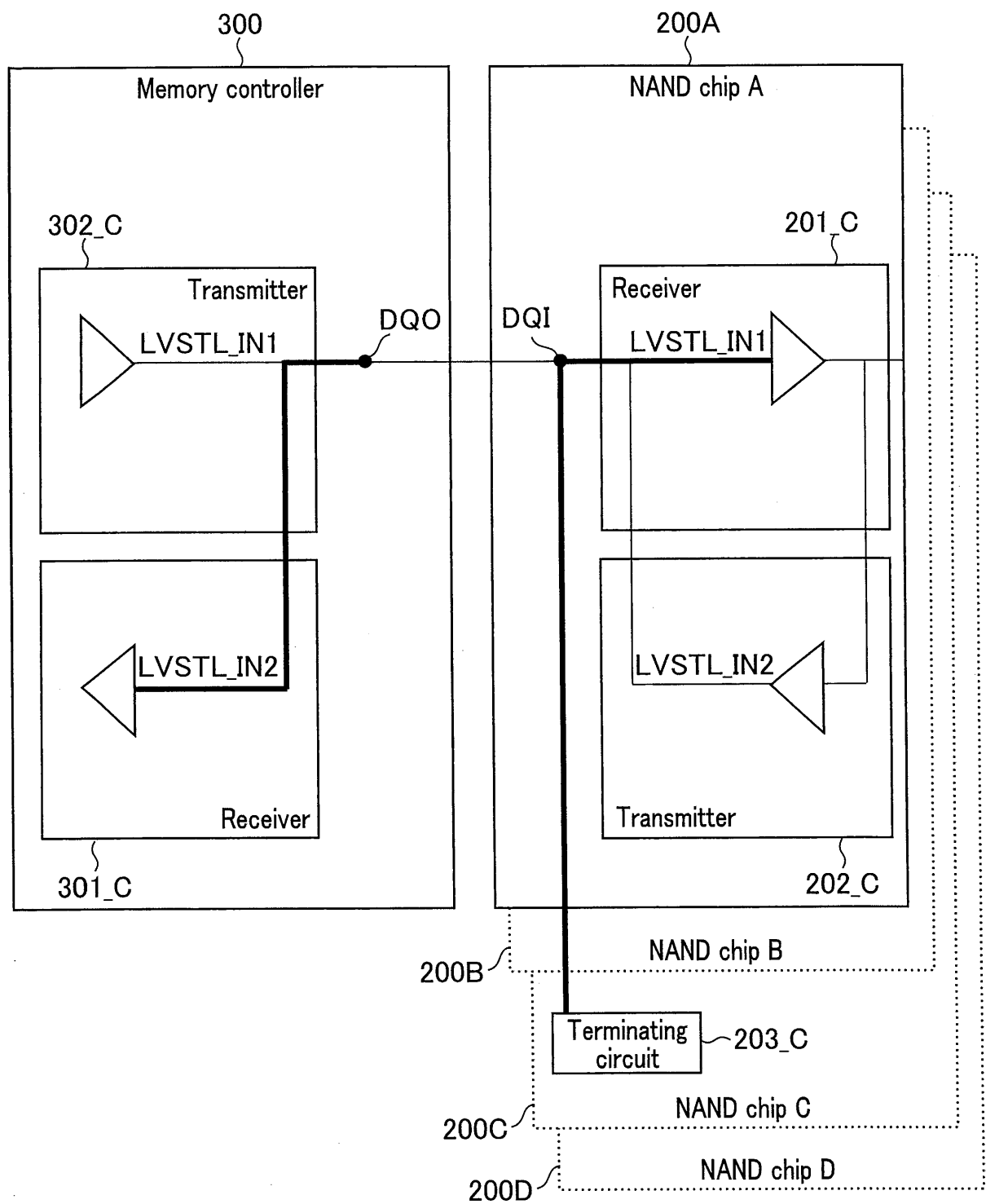


FIG. 44

Command & address

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1	LVSTL_IN1	Terminate	
DQS	floating			Terminate	
RE	floating			Terminate	

Status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2		Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2		Terminate	
RE	LVSTL_RE1	LVSTL_RE1		Terminate	

Parallel status

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2	LVSTL_IN2	Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2	LVSTL_DQS2	Terminate	
RE	LVSTL_RE1	LVSTL_RE1	LVSTL_RE1	Terminate	

FeatureData

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	floating			Terminate	

DataOutput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN2	LVSTL_IN2		Terminate	
DQS	LVSTL_DQS2	LVSTL_DQS2		Terminate	
RE	LVSTL_RE1	LVSTL_RE1		Terminate	

DataInput

	Memory controller	NAND chip A	NAND chip B	NAND chip C	NAND chip D
DQ	LVSTL_IN1	LVSTL_IN1		Terminate	
DQS	LVSTL_DQS1	LVSTL_DQS1		Terminate	
RE	floating			Terminate	

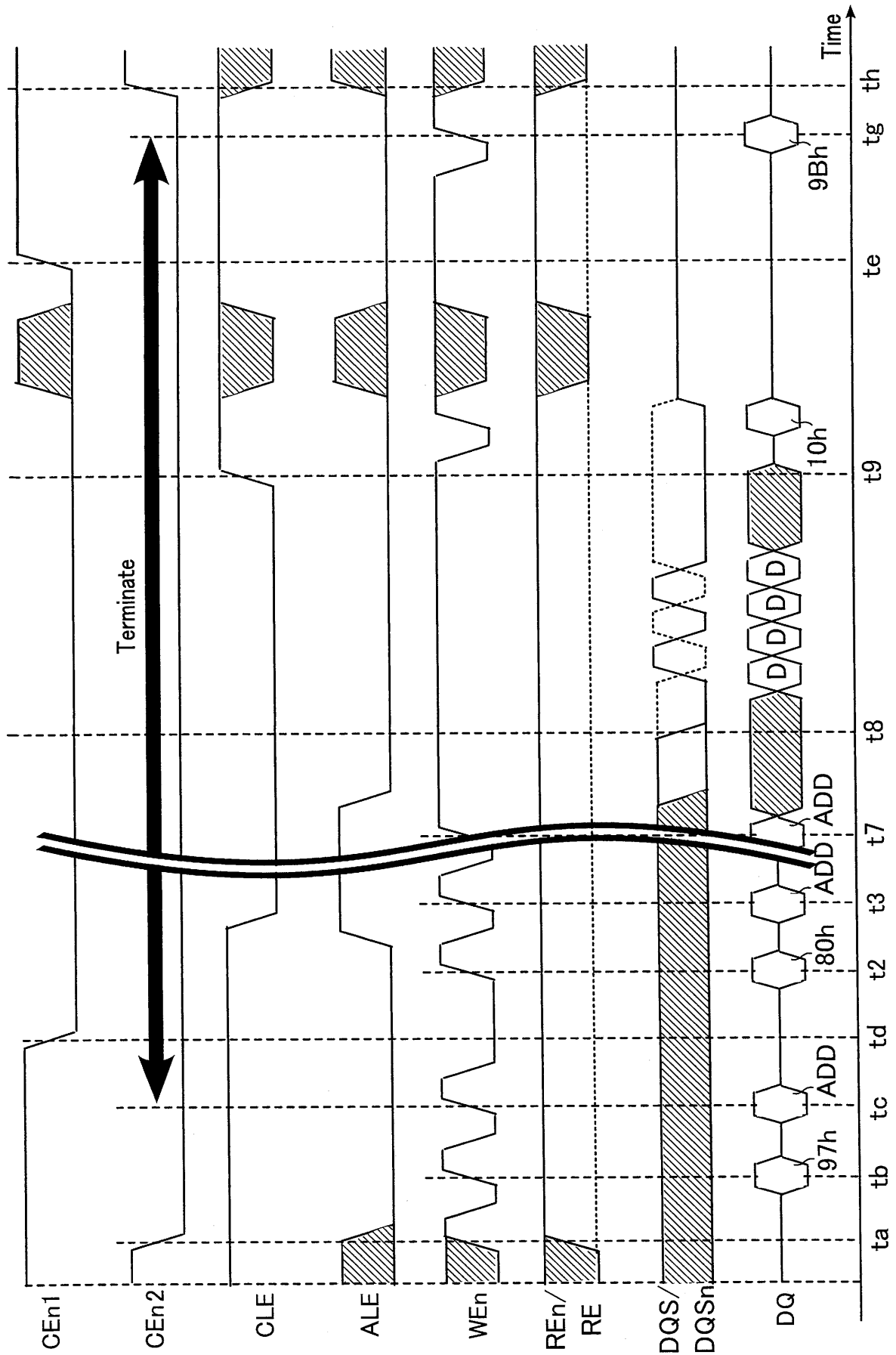


FIG. 46

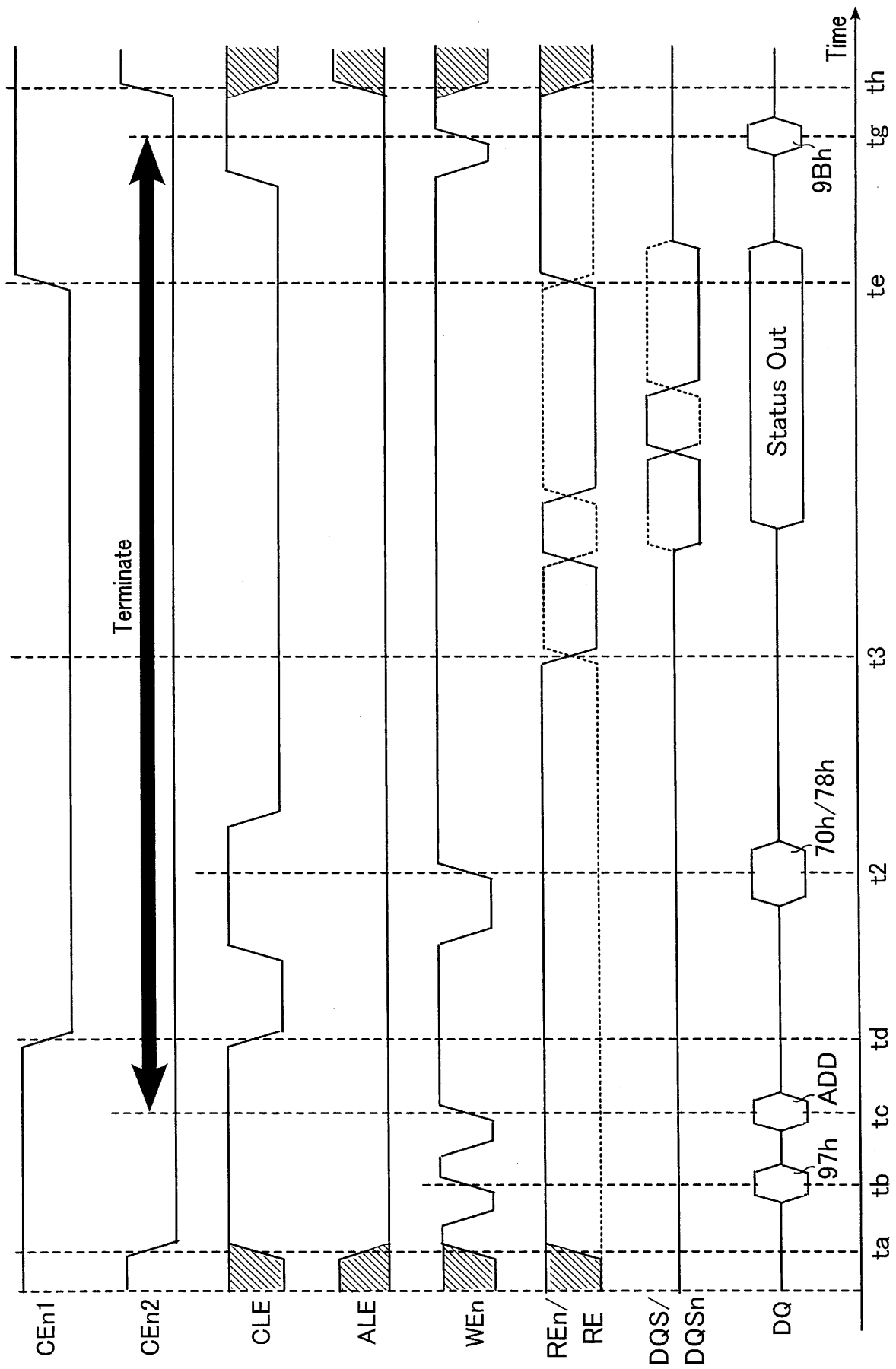


FIG. 47

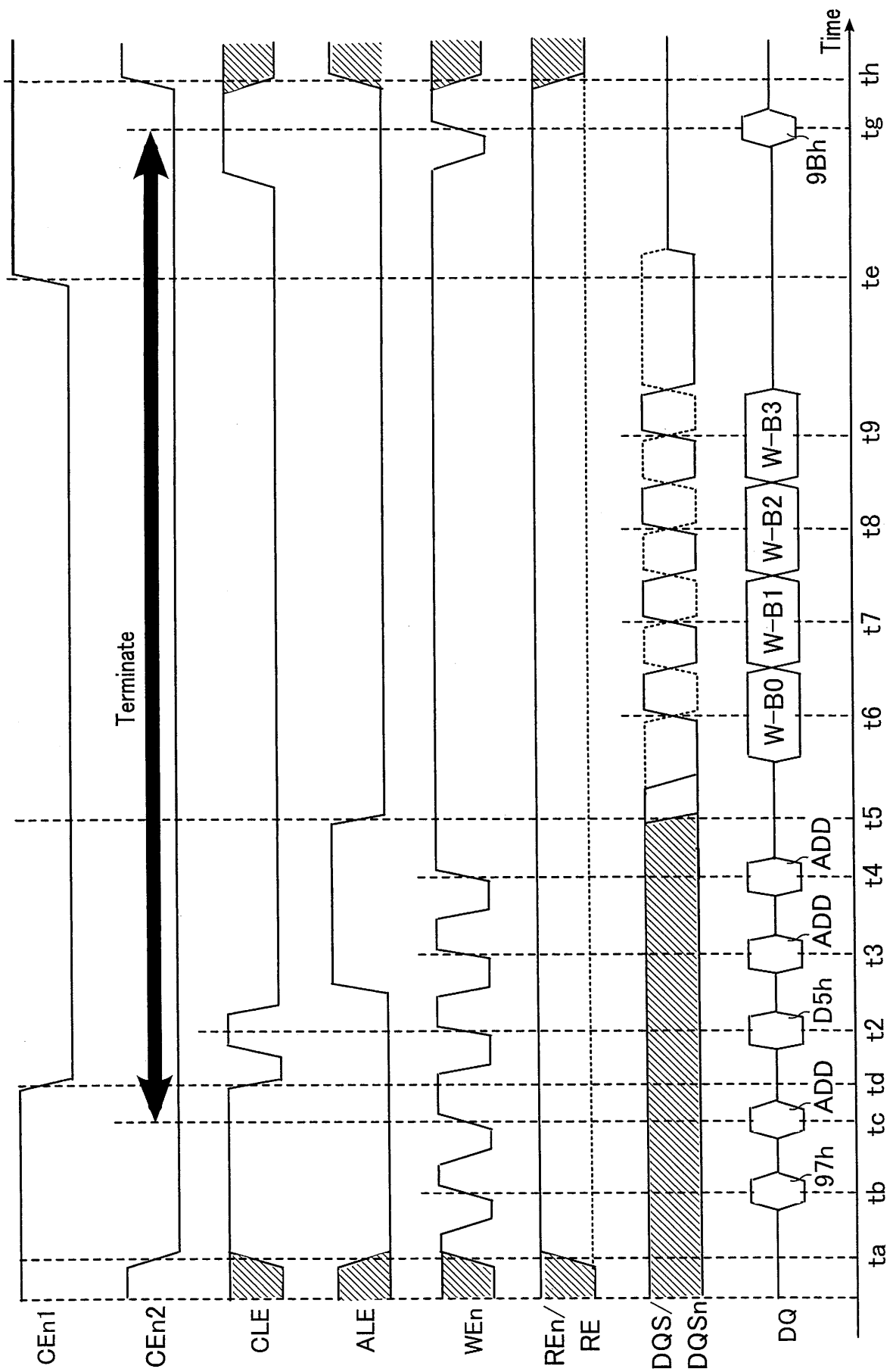


FIG. 48

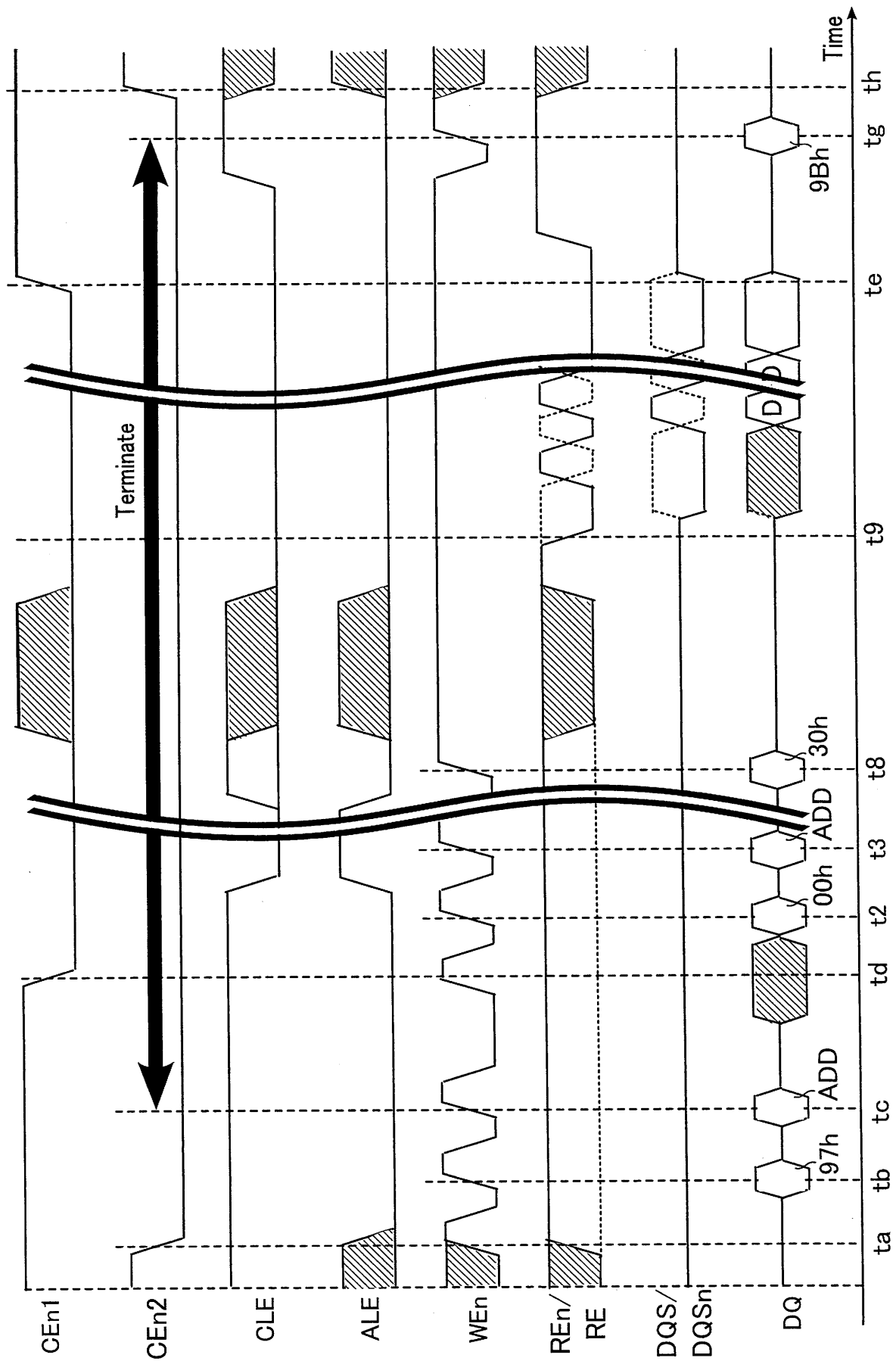


FIG. 49