

SEMICONDUCTOR DEVICE MANUFACTURING METHOD

TECHNICAL FIELD

5 [0001] The present disclosure belongs to the field of semiconductor technology, and particularly relates to a semiconductor device manufacturing method.

BACKGROUND

10 [0002] At present, a Forksheet structure is proposed for meeting the challenges of continuous reduction of critical dimensions of semiconductor devices and continuous increase of device density, and introduces a dielectric wall between two transistors, so as to further shorten the spacing between the two transistors.

15 [0003] However, in the conventional Forksheet structure, channel regions of the two transistors are attached to both sides of the dielectric wall, and a gate structure when being subsequently formed outside each channel region can only surround three sides of the channel region, such that it is hard to reduce Drain Induced Barrier Lowering (DIBL) in 3nm and more advanced semiconductor manufacturing processes.

SUMMARY

20 [0004] An embodiment of the present disclosure discloses a semiconductor device manufacturing method, so as to solve the problem of high DIBL of the semiconductor devices in the related art.

[0005] In order to solve the above technical problem, an embodiment of the present disclosure discloses a semiconductor device manufacturing method, including:

25 forming a first stacked structure and a second stacked structure spaced apart from each other on a substrate, each of the first stacked structure and the second stacked structure including first semiconductor layers and second semiconductor layers which are alternately stacked;

filling a dielectric wall and sacrificial layers between the first stacked structure and the second stacked structure, the sacrificial layers being located on both sides of the dielectric wall to respectively separate the dielectric wall from the first stacked structure and separate the dielectric wall from the second stacked structure, and the sacrificial layers having a high etch selectivity relative to the first semiconductor layers or the second semiconductor layers;

removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers; and

forming a gate structure around the other of the first semiconductor layers and the second semiconductor layers.

[0006] In some alternative implementations, forming the first stacked structure and the second stacked structure spaced apart from each other on the substrate includes:

alternately stacking the first semiconductor layers and the second semiconductor layers on the substrate; and

etching the alternately stacked first semiconductor layers and second semiconductor layers to form an isolation trench, the isolation trench dividing the alternately stacked first semiconductor layers and second semiconductor layers into the first stacked structure and the second stacked structure, the first stacked structure being configured to form a first semiconductor device, and the second stacked structure being configured to form a second semiconductor device.

[0007] In some alternative implementations, filling the dielectric wall and the sacrificial layers between the first stacked structure and the second stacked structure includes:

forming a liner layer to cover sidewalls and a bottom surface of the isolation trench;

forming the dielectric wall on the liner layer to fill the isolation trench;

removing at least part of the liner layer on the sidewalls of the isolation trench to form a cavity; and

filling the cavity with the sacrificial layers.

[0008] In some alternative implementations, removing at least part of the liner layer on the sidewalls of the isolation trench to form the cavity includes:

removing at least part of the liner layer between the dielectric wall and the first stacked structure to form a first cavity; and

removing at least part of the liner layer between the dielectric wall and the second stacked structure to form a second cavity; and

filling the cavity with the sacrificial layers includes:

filling the first cavity with a first sub-sacrificial layer, the first sub-sacrificial layer having a high etch selectivity relative to one of the first semiconductor layers and the second semiconductor layers; and

5 filling the second cavity with a second sub-sacrificial layer, the second sub-sacrificial layer having a high etch selectivity relative to the other of the first semiconductor layers and the second semiconductor layers.

[0009] In some alternative implementations, the sacrificial layers include a first sub-sacrificial layer and a second sub-sacrificial layer;

10 the first sub-sacrificial layer is located between the dielectric wall and the first stacked structure to separate the dielectric wall from the first stacked structure, and has a high etch selectivity relative to one of the first semiconductor layers and the second semiconductor layers; and

the second sub-sacrificial layer is located between the dielectric wall and the second
15 stacked structure to separate the dielectric wall from the second stacked structure, and has a high etch selectivity relative to the other of the first semiconductor layers and the second semiconductor layers.

[0010] In some alternative implementations, a material of the first sub-sacrificial layer is the same as a material of one of the first semiconductor layers and the second
20 semiconductor layers; and

a material of the second sub-sacrificial layer is the same as a material of the other of the first semiconductor layers and the second semiconductor layers.

[0011] In some alternative implementations, the first semiconductor layers are made of Si, and the second semiconductor layers are made of SiGe;

25 the first sub-sacrificial layer is made of one of polycrystalline Si and polycrystalline SiGe; and

the second sub-sacrificial layer is made of the other of polycrystalline Si and polycrystalline SiGe.

[0012] In some alternative implementations, the first semiconductor layers have a high etch
30 selectivity relative to the second semiconductor layers; or

the second semiconductor layers have a high etch selectivity relative to the first semiconductor layers.

[0013] In some alternative implementations, a material of the sacrificial layers is the same as a material of the first semiconductor layers or a material of the second semiconductor layers;

in a case where the material of the sacrificial layers is the same as the material of the first semiconductor layers, the sacrificial layers and the first semiconductor layers have a high etch selectivity relative to the second semiconductor layers, and removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers includes: removing the first semiconductor layers and the sacrificial layers; and

in a case where the material of the sacrificial layers is the same as the material of the second semiconductor layers, the sacrificial layers and the second semiconductor layers have a high etch selectivity relative to the first semiconductor layers, and removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers includes: removing the second semiconductor layers and the sacrificial layers.

[0014] In some alternative implementations, the first semiconductor layers are made of Si, and the second semiconductor layers are made of SiGe; and

the sacrificial layers are made of polycrystalline Si or polycrystalline SiGe.

[0015] In some alternative implementations, at least part of the liner layer on the sidewalls of the isolation trench is removed by a dry etching process or a wet etching process;

the liner layer has a high etch selectivity relative to the dielectric wall; and

the sacrificial layers have a high etch selectivity relative to the dielectric wall.

[0016] In some alternative implementations, before removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers, the semiconductor device manufacturing method further includes:

forming source and drain regions on both sides of the first stacked structure and the second stacked structure along a second direction, the second direction being perpendicular to a first direction, and the first direction being an arrangement direction of the first stacked structure and the second stacked structure.

[0017] In some alternative implementations, forming the source and drain regions on the both sides of the first stacked structure and the second stacked structure along the second direction includes:

removing one of the first semiconductor layers and the second semiconductor layers by a predetermined thickness along the second direction;

filling the one of the first semiconductor layers and the second semiconductor layers which is removed with insulating layers; and

performing epitaxial growth on surfaces of the other of the first semiconductor layers and the second semiconductor layers to form the source and drain regions.

- 5 [0018] With the semiconductor device manufacturing method according to the embodiment of the present disclosure, by forming the dielectric wall and the sacrificial layers in the isolation trench, and removing the sacrificial layers by the subsequent etching process, the gate structure surrounding entire channel regions can be formed, which can reduce DIBL and achieve better control on a leakage current of the semiconductor device.

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BRIEF DESCRIPTION OF DRAWINGS

[0019] FIG. 1 is a flowchart illustrating a semiconductor device manufacturing method according to an embodiment of the present disclosure;

- 15 [0020] FIG. 2 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0021] FIG. 3 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0022] FIG. 4 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

- 20 [0023] FIG. 5 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0024] FIG. 6 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

- 25 [0025] FIG. 7 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0026] FIG. 8 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0027] FIG. 9 to FIG. 12 are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

- 30 [0028] FIG. 13 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0029] FIG. 14 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0030] FIG. 15A and FIG. 15B are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0031] FIG. 16A and FIG. 16B are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0032] FIG. 17A and FIG. 17B are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0033] FIG. 18A and FIG. 18B are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0034] FIG. 19A and FIG. 19B are schematic diagrams illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure;

[0035] FIG. 20 is a schematic diagram illustrating one stage of a semiconductor device manufacturing method according to an embodiment of the present disclosure.

DETAIL DESCRIPTION OF EMBODIMENTS

[0036] In order to make the objective, technical solutions and advantages of the present disclosure clearer, the technical solutions in the embodiment of the present disclosure are clearly and thoroughly described below with reference to the drawings for the embodiment of the present disclosure. Apparently, the embodiment described herein only covers some embodiments of the present disclosure, and do not cover all embodiments. All other embodiments derived by those of ordinary skill in the art from the embodiment described herein without inventive work fall within the scope of the present disclosure.

[0037] It should be understood by those of ordinary skill in the art that the embodiment of the present disclosure is just an explanation of the structure and method which are claimed by the present disclosure and can be embodied in various forms. Further, each example given in connection with each embodiment is for the purpose of illustration, rather than for

the purpose of limitation. Further, the drawings are not necessarily to scale, some features may be exaggerated to show details of particular components. Therefore, the specific structural and functional details in the embodiment of the present disclosure should not be interpreted as being for the purpose of limitation, and just representative bases for teaching those of ordinary skill in the art to adopt the method and structure according to the embodiment of the present disclosure in various forms. It should be further noted that the same elements and the corresponding elements are referred to by the same reference numerals.

[0038] In the following description, many specific details such as particular structures, components, materials, dimensions, processing steps, and techniques are described, so as to provide understanding of each embodiment of the present disclosure. However, it should be understood by those of ordinary skill in the art that each embodiment of the present disclosure may be practiced without these specific details. In other cases, well-known structures or processing steps are not described in detail for avoiding obscuring the present disclosure.

[0039] For the purpose of description, the terms “on”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom” and derivative terms thereof relate to the orientations of the structure and method disclosed in the drawings of the specification. It should be understood that when an element as a layer, region or substrate is referred to as being “on” the other element, the element may be directly on the other element, or an intermediate element may be present. In contrast, when an element is referred to as being “directly on” the other element, there is no intermediate element between the two elements. It should be further understood that when an element is referred to as being “under” the other element, the element may be directly under the other element, or an intermediate element may be present. In contrast, when an element is referred to as being “directly under” the element, there is no intermediate element between the two elements.

[0040] The technical solutions provided in the embodiment of the present disclosure will be described in detail below with reference to the drawings.

[0041] An embodiment of the present disclosure provides a semiconductor device manufacturing method. As shown in FIG. 1, the method may include the following steps S110 to S150.

[0042] At S110, a first stacked structure and a second stacked structure spaced apart from each other are formed on a substrate.

[0043] As shown in FIG. 3, a first stacked structure 200A and a second stacked structure 200B spaced apart from each other are formed on a substrate 100, and each of the first stacked structure 200A and the second stacked structure 200B includes first semiconductor layers 110 and second semiconductor layers 120 which are alternately stacked. In some alternative implementations, the first stacked structure 200A and the second stacked structure 200B may be spaced apart from each other by an isolation trench 130, for example.

[0044] At least a surface of the substrate 100 is provided thereon with a single crystal semiconductor layer. The substrate 100 may be made of a single-crystal semiconductor material including, but not limited to, Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, or InP. In some alternative implementations, the substrate 100 may be made of crystalline Si. The substrate 100 may include one or more buffer layers (not shown) in a surface region of the substrate 100. The buffer layer may be configured to gradually change a lattice constant from that of the substrate to that of a source/drain region. The buffer layer may be made of an epitaxially grown single-crystal semiconductor material, including, but not limited to, Si, Ge, GeSn, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, GaN, GaP, or InP. In some alternative implementations, the substrate 100 may include a silicon germanium (SiGe) buffer layer epitaxially grown on a silicon substrate. The substrate 100 may further include regions appropriately doped with impurities (e.g., with p-type or n-type conductivity).

[0045] The first semiconductor layers 110 and the second semiconductor layers 120 may be made of materials having different lattice constants, and may include one or more layers of Si, Ge, SiGe, GeSn, SiGeSn, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, or InP. In some alternative implementations, the first semiconductor layers 110 and the second semiconductor layers 120 are made of Si, a Si compound, SiGe, Ge, or a Ge compound. In some alternative implementations, the first semiconductor layers 110 are made of Si, and the second semiconductor layers 120 are made of SiGe. In other alternative implementations, the first semiconductor layers 110 may be made of SiGe, and a Ge content of the first semiconductor layers 110 is different from that of the second semiconductor layers 120. For conciseness, the embodiment of the present disclosure is described in detail herein by taking the first semiconductor layers 110 being made of Si and the second semiconductor layers 120 being made of SiGe as an example.

[0046] It should be noted that the first semiconductor layers 110 have a high etch selectivity relative to the second semiconductor layers 120 or the second semiconductor layers 120 have a high etch selectivity relative to the first semiconductor layers 110 in a subsequent etching process, so that the first semiconductor layers 110 or the second semiconductor layers 120 may be selectively removed. Here, the high etch selectivity refers to that the etch selectivity is greater than 10 and the etch selectivity is preferably greater than 50, and more preferably, greater than 100, so that a selective etch process may be precisely performed to avoid damaging to one of the first semiconductor layers 110 and the second semiconductor layers 120 as much as possible while removing the other of the first semiconductor layers 110 and the second semiconductor layers 120.

[0047] In the present embodiment, the first stacked structure 200A is configured to form a first semiconductor device, the second stacked structure 200B is configured to form a second semiconductor device, and the first semiconductor device and the second semiconductor device may be, for example, field effect transistors. Taking the first semiconductor layers 110 being made of Si and the second semiconductor layers 120 being made of SiGe as an example, when a semiconductor device to be formed has the first semiconductor layers 110 removed and the second semiconductor layers 120 kept, the semiconductor device may be used as a P-type semiconductor device; and when the semiconductor device to be formed has the second semiconductor layers 120 removed and the first semiconductor layers 110 kept, the semiconductor device may be used as an N-type semiconductor device.

[0048] In an example illustrated by FIG. 3, the first semiconductor layers 110 in the first stacked structure 200A and the first semiconductor layers 110 in the second stacked structure 200B are disposed in same-layer arrangement, and the second semiconductor layers 120 in the first stacked structure 200A and the second semiconductor layers 120 in the second stacked structure 200B are disposed in same-layer arrangement. In some alternative implementations of the embodiment of present disclosure, the first semiconductor layers 110 in the first stacked structure 200A and the first semiconductor layers 110 in the second stacked structure 200B may be disposed in staggered-layer arrangement, and the second semiconductor layers 120 in the first stacked structure 200A and the second semiconductor layers 120 in the second stacked structure 200B may be disposed in staggered-layer arrangement, that is, the first semiconductor layers 110 in the first stacked structure 200A and the second semiconductor layers 120 in the second stacked

structure 200B are located at same levels, and the second semiconductor layers 120 in the first stacked structure 200A and the first semiconductor layers 110 in the second stacked structure 200B are located at same levels.

[0049] In some alternative implementations of the embodiment of the present disclosure, step S110 may include the following steps S111 and S112.

[0050] At S111, the first semiconductor layers and the second semiconductor layers are alternately stacked on the substrate.

[0051] As shown in FIG. 2, the first semiconductor layers 110 and the second semiconductor layers 120 are alternately stacked on the substrate 100.

[0052] At S112, the alternately stacked first semiconductor layers and second semiconductor layers are etched to form the isolation trench.

[0053] As shown in FIG. 3, the isolation trench 130 is formed in the alternately stacked first semiconductor layers 110 and second semiconductor layers 120 by an etching process, and the isolation trench 130 separates the first stacked structure 200A for forming the first semiconductor device from the second stacked structure 200B for forming the second semiconductor device. In some alternative implementations of the embodiment of the present disclosure, the first semiconductor device and the second semiconductor device may be of a same type of conductivity, for example, both the first semiconductor device and the second semiconductor device are N-type semiconductor devices or P-type semiconductor devices. In some other alternative implementations, the first semiconductor device and the second semiconductor device may be of different types of conductivity, for example, the first semiconductor device is an N-type semiconductor device, and the second semiconductor device is a P-type semiconductor device. In some alternative implementations of the embodiment of the present disclosure, the isolation trench 130 may extend into the substrate 100 as shown in FIG. 3, and thus may serve as a Shallow Trench Isolation (STI) structure to separate the two semiconductor devices from each other.

[0054] At S120, a dielectric wall and sacrificial layers are filled between the first stacked structure and the second stacked structure.

[0055] As shown in FIG. 7, a dielectric wall 132 and sacrificial layers 134 are formed between the first stacked structure 200A and the second stacked structure 200B, and fill the space between the first stacked structure 200A and the second stacked structure 200B. The sacrificial layers 134 are located on both sides of the dielectric wall 132 to respectively separate the dielectric wall 132 from the first stacked structure 200A and separate the

dielectric wall 132 from the second stacked structure 200B, that is, the both sides of the dielectric wall 132 are respectively separated from the first stacked structure 200A and the second stacked structure 200B by the sacrificial layers 134. In order to ensure that the sacrificial layers 134 are removed together with the first semiconductor layers 110 or the second semiconductor layers 120 in the subsequent etching process, the sacrificial layers 134 needs to have a high etch selectivity relative to the first semiconductor layers 110 or the second semiconductor layers 120.

[0056] In some alternative implementations of the embodiment of the present disclosure, step S120 may include the following steps S121 to S124.

[0057] At S121, a liner layer is formed to cover sidewalls and a bottom surface of the isolation trench.

[0058] As shown in FIG. 4, a liner layer 131 may be formed by Chemical Vapor Deposition (CVD) (including Low Pressure Chemical Vapor Deposition (LPCVD) and Plasma Enhanced Chemical Vapor Deposition (PECVD)), Physical Vapor Deposition (PVD), Atomic Layer Deposition (ALD), or other suitable processes to cover a top surface, the bottom surface, and the sidewalls of the isolation trench 130. In some alternative implementations, the liner layer 131 may be made of silicon oxide, and may be manufactured by an ALD process, for example.

[0059] At S122, the dielectric wall is formed on the liner layer to fill the isolation trench.

[0060] As shown in FIG. 5, the dielectric wall 132 is formed on the liner layer 131 to fill the isolation trench 130. At this step, the dielectric wall 132 may be formed by ALD or CVD, for example. The dielectric wall 132 may be made of silicon nitride, aluminum oxide, hafnium oxide (HfO_2), or other high-k dielectric materials. Although not shown, it should be understood by those of ordinary skill in the art that the liner layer 131 and the dielectric wall 132 beyond the isolation trench 130 may be removed by etching or Chemical Mechanical Polishing (CMP) after the dielectric wall 132 is formed to fill the isolation trench 130, thereby obtaining the semiconductor structure shown in FIG. 5.

[0061] At S123, at least part of the liner layer on the sidewalls of the isolation trench is removed to form a cavity.

[0062] As shown in FIG. 6, at least part of the liner layer 131 on the sidewalls of the isolation trench 130 is removed to form a cavity 133. In an example illustrated by FIG. 6, part of the liner layer 131 on the sidewalls of the isolation trench 130 is removed, and the

cavity 133 extends below the surface of the substrate 100. Certainly, the entire liner layer 131 on the sidewalls of the isolation trench 130 may be removed.

[0063] In some alternative implementations of the embodiment of the present disclosure, in order to avoid damaging the dielectric wall 132 while etching the liner layer 131, the liner layer 131 needs to have a high etch selectivity relative to the dielectric wall 132, step S123 may be performed by a dry etching process, for example, a relatively low chamber pressure may be adopted to increase a mean free path of etching plasma, so as to enable the cavity 133 to extend below the surface of the substrate 100. In some other alternative implementations of the embodiment of the present disclosure, step S123 may be performed by a wet etching process.

[0064] At step S124, the cavity is filled with the sacrificial layers.

[0065] As shown in FIG. 7, the cavity 133 is filled with the sacrificial layers 134. At this step, a relatively low chamber pressure may be adopted to increase a mean free path of depositing plasma, so as to sufficiently fill the cavity 133.

[0066] In some alternative implementations of the embodiment of the present disclosure, the sacrificial layers 134 have a high etch selectivity relative to the dielectric wall 132. For this purpose, the sacrificial layers 134 may be made of a material the same as that of the first semiconductor layers 110 or that of the second semiconductor layers 120. Specifically, when the material of the sacrificial layers 134 are the same as that of the first semiconductor layers 110, the sacrificial layers 134 and the first semiconductor layers 110 have a high etch selectivity relative to the second semiconductor layers 120, so that the sacrificial layers 134 are removed together with the first semiconductor layers 110 in the subsequent etching process; and when the material of the sacrificial layers 134 are the same as that of the second semiconductor layers 120, the sacrificial layers 134 and the second semiconductor layers 120 have a high etch selectivity relative to the first semiconductor layers 110, so that the sacrificial layers 134 are removed together with the second semiconductor layers 120 in the subsequent etching process. Moreover, the dielectric wall 132 needs to be prevented from being etched while removing the sacrificial layers 134 and the first semiconductor layers 110 or the second semiconductor layers 120. In view of the above, in the present embodiment, a part of the liner layer 131 is replaced with the sacrificial layers 134, so as to enable the subsequent selective etching.

[0067] In some more specific alternative implementations of the embodiment of the present disclosure, the first semiconductor layers 110 are made of Si, and the second semiconductor

layers 120 are made of SiGe; and the sacrificial layers 134 are made of polycrystalline Si or polycrystalline SiGe. When the sacrificial layers 134 are made of polycrystalline Si, the sacrificial layers 134 are removed together with the first semiconductor layers 110 in the subsequent etching process; and when the sacrificial layers 134 are made of polycrystalline SiGe, the sacrificial layers 134 are removed together with the second semiconductor layers 110 in the subsequent etching process. Specifically, filling the cavity 133 with the sacrificial layers 134 may include: filling the cavity 133 with monocrystalline Si or monocrystalline SiGe; and annealing monocrystalline Si or monocrystalline SiGe to form polycrystalline Si or polycrystalline SiGe. For example, the cavity 133 may be filled with monocrystalline Si or monocrystalline SiGe by LPCVD, and then the filled monocrystalline Si or monocrystalline SiGe may be subjected to a high temperature annealing process to recrystallize monocrystalline Si or monocrystalline SiGe into polycrystalline Si or polycrystalline SiGe.

[0068] At S130, source and drain regions of the first semiconductor device and the second semiconductor device are formed. This step will be described in detail below for avoiding obscuring the main concept of the present disclosure.

[0069] At S140, one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers are removed.

[0070] In an example illustrated by FIG. 8, the second semiconductor layers 120 in the first stacked structure 200A and the second stacked structure 200B and the sacrificial layers 134 are removed, and only the first semiconductor layers 110 are kept. As described above, for example, the first semiconductor layers 110 may be made of Si, the second semiconductor layer 120 may be made of SiGe, and the sacrificial layers 134 may be made of polycrystalline SiGe; and in the etching process at this step, by endowing SiGe with a high etch selectivity relative to Si, the second semiconductor layers 120 and the sacrificial layers 134 are removed, and only the first semiconductor layers 110 are kept, so that two N-type semiconductor devices are formed by subsequent processes. However, the present disclosure is not limited thereto. In some alternative implementations, for example, the first semiconductor layer 110 may be made of Si, the second semiconductor layer 120 may be made of SiGe, and the sacrificial layers 134 may be made of polycrystalline Si; and in this case, by endowing Si with a high etch selectivity relative to SiGe in the etching process, the first semiconductor layers 110 and the sacrificial layers 134 are removed, and only the second semiconductor layers 120 are kept, so that two P-type semiconductor devices are

formed by subsequent processes. Meanwhile, in order to avoid damaging the dielectric wall 132 while removing the sacrificial layers 134, the sacrificial layers 134 need to have a high etch selectivity relative to the dielectric wall 132.

[0071] In some other alternative implementations of the embodiment of the present disclosure, as shown in FIG. 9 to FIG. 12, the sacrificial layers on the both sides of the dielectric wall 132 may be different, and may include a first sub-sacrificial layer 134a and a second sub-sacrificial layer 134b, the first sub-sacrificial layer 134a is located between the dielectric wall 132 and the first stacked structure 200A to separate the dielectric wall 132 from the first stacked structure 200A; and the second sub-sacrificial layer 134b is located between the dielectric wall 132 and the second stacked structure 200B to separate the dielectric wall 132 from the second stacked structure 200B. The first sub-sacrificial layer 134a has a high etch selectivity relative to one of the first semiconductor layers 110 and the second semiconductor layers 120, and the second sub-sacrificial layer 134b has a high etch selectivity relative to the other of the first semiconductor layers 110 and the second semiconductor layers 120. For example, the first sub-sacrificial layer 134a has a high etch selectivity relative to the first semiconductor layers 110, and the second sub-sacrificial layer 134b has a high etch selectivity relative to the second semiconductor layers 120, so that the first sub-sacrificial layer 134a is removed together with the second semiconductor layers 120 and only the first semiconductor layers 110 are kept in the first stacked structure 200A in an etching process subsequently performed on the first stacked structure 200A, and the second sub-sacrificial layer 134b is removed together with the first semiconductor layers 110 and only the second semiconductor layers 120 are kept in the second stacked structure 200B in an etching process subsequently performed on the second stacked structure 200B, thereby forming an N-type semiconductor device and a P-type semiconductor device by the subsequent processes.

[0072] Specifically, a material of the first sub-sacrificial layer 134a is the same as that of one of the first semiconductor layers 110 and the second semiconductor layers 120, and a material of the second sub-sacrificial layer 134b is the same as that of the other of the first semiconductor layers 110 and the second semiconductor layers 120. For example, the material of the first sub-sacrificial layer 134a is the same as that of the second semiconductor layers 120, and the material of the second sub-sacrificial layer 134b is the same as that of the first semiconductor layers 110. More specifically, the first semiconductor layers 110 are made of Si, the second semiconductor layers 120 are made of

SiGe, the first sub-sacrificial layer 134a is made of one of polycrystalline Si and polycrystalline SiGe, and the second sub-sacrificial layer 134b is made of the other of polycrystalline Si and polycrystalline SiGe. For example, the first sub-sacrificial layer 134a is made of polycrystalline SiGe, and the second sub-sacrificial layer 134b is made of polycrystalline Si.

[0073] Specifically, a method for forming the first sub-sacrificial layer 134a and the second sub-sacrificial layer 134b may include the following steps S123a, S124a, S123b, and S124b.

[0074] At S123a, at least part of the liner layer between the dielectric wall and the first stacked structure is removed to form a first cavity.

[0075] As shown in FIG. 9, a mask layer for protecting the liner layer 131b between the dielectric wall 132 and the second stacked structure 200B needs to be formed, and the mask layer may cover, for example, the dielectric wall 132, the liner layer 131b, and the second stacked structure 200B, so that at least part of the exposed liner layer 131 between the dielectric wall 132 and the first stacked structure 200A may be etched to form a first cavity 133a.

[0076] At S124a, the first cavity is filled with the first sub-sacrificial layer.

[0077] As shown in FIG. 10, the first cavity 133a shown in FIG. 9 is filled with the first sub-sacrificial layer 134a, which has the high etch selectivity relative to one of the first semiconductor layers 110 and the second semiconductor layers 120. In an alternative implementation, the first semiconductor layers 110 are made of Si, the second semiconductor layers 120 are made of SiGe, and the first sub-sacrificial layer 134a is made of polycrystalline SiGe.

[0078] At S123b, at least part of the liner layer between the dielectric wall and the second stacked structure is removed to form a second cavity.

[0079] As shown in FIG. 11, the mask layer formed at step S123a is removed, a mask layer for protecting the first sub-sacrificial layer 134a between the dielectric wall 132 and the first stacked structure 200A is formed, and the mask layer may cover, for example, the dielectric wall 132, the first sub-sacrificial layer 134a, and the first stacked structure 200A, so that at least part of the exposed liner layer 131b between the dielectric wall 132 and the second stacked structure 200B may be etched to form a second cavity 133b.

[0080] At S124b, the second cavity is filled with the second sub-sacrificial layer.

[0081] As shown in FIG. 12, the second cavity 133b shown in FIG. 11 is filled with the second sub-sacrificial layer 134b, and the mask layer formed at step S123b is removed, thereby obtaining a semiconductor structure shown in FIG. 12.

[0082] The first sub-sacrificial layer 134a and the second sub-sacrificial layer 134b can be respectively formed on the both sides of the dielectric wall 132 by the above steps S123a, S124a, S123b, and S124b, so that an N-type semiconductor device and a P-type semiconductor device can be formed on the both sides of the dielectric wall 132 by subsequent processes, respectively.

[0083] At S150, a gate structure is formed around the other of the first semiconductor layers and the second semiconductor layers.

[0084] The gate structure may include a gate dielectric layer 141 and a gate electrode layer 142 which are disposed around the other of the first semiconductor layers and the second semiconductor layers (i.e., the first semiconductor layers or the second semiconductor layers kept after step S140).

[0085] In an example illustrated by FIG. 13, the second semiconductor layers 120 are removed, only the first semiconductor layers 110 are kept, and the sacrificial layers 134 are removed, so that gap are formed between the first semiconductor layers 110 and the dielectric wall 132, which enables the gate dielectric layer 141 to be formed around the entire first semiconductor layers 110, and the first semiconductor layers 110 enclosed with the gate dielectric layer 141 form channel regions of the semiconductor device. In some alternative implementations, the gate dielectric layer 141 may include one or more layers of a dielectric material (such as silicon oxide, silicon nitride, or a high-k dielectric material), other suitable dielectric materials, and/or combinations thereof. The high-k dielectric material may include, for example, HfO₂, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconia, alumina, titania, a hafnium dioxide-alumina (HfO₂-Al₂O₃) alloy, other suitable high-k dielectric materials, and/or combinations thereof. In some implementations, interface layers may be further formed between the channel regions (i.e., the first semiconductor layers 110) and the gate dielectric layer 141. The gate dielectric layer 141 may be formed with CVD, ALD, or any suitable methods. In an alternative implementation, a thickness of the gate dielectric layer 141 is in a range from about 1 nm to about 6 nm.

[0086] As shown in FIG. 14, the space outside the gate dielectric layer 141 is filled with the gate electrode layer 142, thereby forming the gate electrode layer 142 around the first semiconductor layers 110. In some alternative implementations, the gate electrode layer

142 may include one or more layers of a conductive material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, alloys thereof, other suitable materials, and/or combinations thereof. The gate electrode layer 142 may be
5 formed with CVD, ALD, plating, or other suitable methods.

[0087] Unlike the conventional Forksheet structure in which the gate structure can surround only three sides of the channel, with the semiconductor device manufacturing method according to the embodiment of the present disclosure, by forming the dielectric wall and the sacrificial layers in the isolation trench, and removing the sacrificial layers by the
10 subsequent etching process, the gate structure surrounding the entire channel regions can be formed, which can reduce DIBL and achieve better control on a leakage current of the semiconductor device.

[0088] Step S130 is described in detail below. More specifically, source and drain regions 160 need to be formed on both sides of the first stacked structure 200A and the second stacked structure 200B along a second direction, and the second direction is perpendicular
15 to a first direction, which is an arrangement direction of the first stacked structure 200A and the second stacked structure 200B. Step S130 may specifically include the following steps S131 to S135.

[0089] At S131, a dummy gate structure 140 is formed to cover the first stacked structure
20 200A, the second stacked structure 200B, the dielectric wall 132, and the sacrificial layers 134, as shown in FIG. 15A and FIG. 15B.

[0090] At S132, one of the first semiconductor layers 110 and the second semiconductor layers 120 is removed by a predetermined thickness along the second direction.

[0091] In an example illustrated by FIG. 16A and FIG. 16B, the second semiconductor
25 layers 120 are removed by the predetermined thickness, which is about 3 nm to 10 nm, and more preferably, about 5 nm.

[0092] At S133, the one of the first semiconductor layers 110 and the second semiconductor layers 120 which is removed (i.e., the first semiconductor layers 110 or the second semiconductor layers 120 which are removed by the predetermined thickness after
30 step S132) is filled with insulating layers 150.

[0093] In an example illustrated by FIG. 17A and FIG. 17B, the removed second semiconductor layers 120 are filled with the insulating layers 150. The insulating layers 150 may be made of, for example, silicon nitride. For example, the insulating layers 150

may be formed on sidewalls of the first semiconductor layers 110 and sidewalls of the second semiconductor layers 120 by ALD, and then the insulating layers 150 are removed from the first semiconductor layers 110 by an etching process. The insulating layers 150 are configured to prevent the subsequently formed gate structure from being electrically
5 connected to source regions or drain regions.

[0094] At S134, epitaxial growth is performed on surfaces of the other of the first semiconductor layers 110 and the second semiconductor layers 120 to form the source and drain regions 160.

[0095] In an example illustrated by FIG. 18A and FIG. 18B, the source and drain regions
10 160 are formed on the surfaces of the first semiconductor layers 110 by epitaxial growth, and then the dummy gate structure is removed, thereby obtaining a semiconductor structure shown in FIG. 18A and FIG. 18B.

[0096] In some implementations, after completing step S134, the method may further include the following step:

15 S135, insulating structures 161 are formed on the source and drain regions 160, as shown in FIG. 19A and FIG. 19B.

[0097] In this way, fabrication of a source and drain structure of the semiconductor device according to the embodiment of the present disclosure is achieved by steps S131 to S135. In the subsequent processes, fabrication of the gate structure of the semiconductor device is
20 achieved by steps S140 and S150 as described above.

[0098] In order to clearly illustrate the semiconductor structure obtained after step S140, FIG. 20 shows a sectional axonometric view of the semiconductor structure obtained after step S140. As shown in FIG. 20, both ends of each channel region (i.e., each first semiconductor layer 110) are connected to the source and drain regions 160 along the
25 second direction respectively, so that the first semiconductor layers 110 are suspended in FIG. 8 which is the cross-sectional view in the first direction. The insulating layers 150 are formed between the source and drain regions 160 and the gate structure to be formed, so as to prevent the gate structure from being connected to the source and drain regions 160. With the semiconductor device manufacturing method according to the embodiment of the
30 present disclosure, by forming the dielectric wall and the sacrificial layers in the isolation trench, and removing the sacrificial layers by the subsequent etching process, the gate structure surrounding the entire channel regions can be formed, which can reduce DIBL and achieve better control on a leakage current of the semiconductor device.

[0099] The above embodiment of the present disclosure focuses on the differences between the implementations, and different optimization features of the implementations can be combined to form better implementations as long as the different optimization features are not contradictory, which will not be described in detail here for conciseness of the description.

[0100] What is described above is just the embodiment of the present disclosure, but is not intended to limit the present disclosure. Various modifications and changes may be made to the present disclosure by those of ordinary skill in the art. Any modification, equivalent replacement and improvement made within the spirit and principle of the present disclosure should be included in the scope of the appended claims of the present disclosure.

What is claimed is:

1. A semiconductor device manufacturing method, comprising:

forming a first stacked structure and a second stacked structure spaced apart from each other on a substrate, each of the first stacked structure and the second stacked structure comprising first semiconductor layers and second semiconductor layers which are alternately stacked;

filling a dielectric wall and sacrificial layers between the first stacked structure and the second stacked structure, the sacrificial layers being located on both sides of the dielectric wall to respectively separate the dielectric wall from the first stacked structure and separate the dielectric wall from the second stacked structure, and the sacrificial layers having a high etch selectivity relative to the first semiconductor layers or the second semiconductor layers;

removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers; and

forming a gate structure around the other of the first semiconductor layers and the second semiconductor layers.

2. The semiconductor device manufacturing method of claim 1, wherein forming the first stacked structure and the second stacked structure spaced apart from each other on the substrate comprises:

alternately stacking the first semiconductor layers and the second semiconductor layers on the substrate; and

etching the alternately stacked first semiconductor layers and second semiconductor layers to form an isolation trench, the isolation trench dividing the alternately stacked first semiconductor layers and second semiconductor layers into the first stacked structure and the second stacked structure, the first stacked structure being configured to form a first semiconductor device, and the second stacked structure being configured to form a second semiconductor device.

3. The semiconductor device manufacturing method of claim 2, wherein filling the dielectric wall and the sacrificial layers between the first stacked structure and the second stacked structure comprises:

forming a liner layer to cover sidewalls and a bottom surface of the isolation trench;

forming the dielectric wall on the liner layer to fill the isolation trench;

5 removing at least part of the liner layer on the sidewalls of the isolation trench to form a cavity; and
filling the cavity with the sacrificial layers.

10 4. The semiconductor device manufacturing method of claim 3, wherein removing the at least part of the liner layer on the sidewalls of the isolation trench to form the cavity comprises:

removing at least part of the liner layer between the dielectric wall and the first stacked structure to form a first cavity; and

removing at least part of the liner layer between the dielectric wall and the second stacked structure to form a second cavity; and

15 filling the cavity with the sacrificial layers comprises:

filling the first cavity with a first sub-sacrificial layer, the first sub-sacrificial layer having a high etch selectivity relative to one of the first semiconductor layers and the second semiconductor layers; and

20 filling the second cavity with a second sub-sacrificial layer, the second sub-sacrificial layer having a high etch selectivity relative to the other of the first semiconductor layers and the second semiconductor layers.

5. The semiconductor device manufacturing method of claim 1, wherein the sacrificial layers comprise a first sub-sacrificial layer and a second sub-sacrificial layer;

25 the first sub-sacrificial layer is located between the dielectric wall and the first stacked structure to separate the dielectric wall from the first stacked structure, and has a high etch selectivity relative to one of the first semiconductor layers and the second semiconductor layers; and

30 the second sub-sacrificial layer is located between the dielectric wall and the second stacked structure to separate the dielectric wall from the second stacked structure, and has a high etch selectivity relative to the other of the first semiconductor layers and the second semiconductor layers.

6. The semiconductor device manufacturing method of claim 5, wherein a material of the first sub-sacrificial layer is the same as a material of one of the first semiconductor layers and the second semiconductor layers; and

5 a material of the second sub-sacrificial layer is the same as a material of the other of the first semiconductor layers and the second semiconductor layers.

7. The semiconductor device manufacturing method of claim 6, wherein the first semiconductor layers are made of Si, and the second semiconductor layers are made of SiGe;

10 the first sub-sacrificial layer is made of one of polycrystalline Si and polycrystalline SiGe; and

the second sub-sacrificial layer is made of the other of polycrystalline Si and polycrystalline SiGe.

15 8. The semiconductor device manufacturing method of claim 1, wherein the first semiconductor layers have a high etch selectivity relative to the second semiconductor layers; or

the second semiconductor layers have a high etch selectivity relative to the first semiconductor layers.

20 9. The semiconductor device manufacturing method of claim 8, wherein a material of the sacrificial layers is the same as a material of the first semiconductor layers or a material of the second semiconductor layers;

25 in a case where the material of the sacrificial layers is the same as the material of the first semiconductor layers, the sacrificial layers and the first semiconductor layers have a high etch selectivity relative to the second semiconductor layers, and removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers comprises: removing the first semiconductor layers and the sacrificial layers; and

30 in a case where the material of the sacrificial layers is the same as the material of the second semiconductor layers, the sacrificial layers and the second semiconductor layers have a high etch selectivity relative to the first semiconductor layers, and removing one of the first semiconductor layers and the second semiconductor layers and

the sacrificial layers comprises: removing the second semiconductor layers and the sacrificial layers.

10. The semiconductor device manufacturing method of claim 9, wherein the first
5 semiconductor layers are made of Si, and the second semiconductor layers are made of SiGe; and
the sacrificial layers are made of polycrystalline Si or polycrystalline SiGe.

11. The semiconductor device manufacturing method of claim 3, wherein the at
10 least part of the liner layer on the sidewalls of the isolation trench is removed by a dry etching process or a wet etching process;
the liner layer has a high etch selectivity relative to the dielectric wall; and
the sacrificial layers have a high etch selectivity relative to the dielectric wall.

12. The semiconductor device manufacturing method of any one of claims 1 to 11,
15 wherein before removing one of the first semiconductor layers and the second semiconductor layers and the sacrificial layers, the semiconductor device manufacturing method further comprises:

forming source and drain regions on both sides of the first stacked structure and
20 the second stacked structure along a second direction, the second direction being perpendicular to a first direction, and the first direction being an arrangement direction of the first stacked structure and the second stacked structure.

13. The semiconductor device manufacturing method of claim 12, wherein
25 forming the source and drain regions on the both sides of the first stacked structure and the second stacked structure along the second direction comprises:

removing one of the first semiconductor layers and the second semiconductor
layers by a predetermined thickness along the second direction;

filling the one of the first semiconductor layers and the second semiconductor
30 layers which is removed with insulating layers; and

performing epitaxial growth on surfaces of the other of the first semiconductor
layers and the second semiconductor layers to form the source and drain regions.