PROCESS FOR FABRICATING THIN FILM TRANSISTORS

This invention relates to a process for fabricating thin film transistors.

Thin film transistors (TFT's) are known to be useful for, *inter alia*, controlling various types of display; for example TFT's are commonly used to control liquid crystal displays used in portable computers and similar electronic devices. TFT's can also be used to control electrophoretic displays; see, for example, WO-A-00/67327; WO-A-01/08241; WO-A-01/17029; WO-A-01/17040; and WO-A-01/17041. The disclosures of all these applications are herein incorporated by reference.

Although most TFT's have hitherto been fabricated on rigid substrates, there is increasing interest in fabricating TFT's on flexible substrates, especially flexible polymeric films. TFT's fabricated on such flexible substrates could form the basis for large displays which would be light-weight yet rugged, thus permitting their use in mobile devices. TFT's based upon amorphous silicon semiconductors are attractive for use on such flexible substrates since they allow fabrication with a minimum number of process steps and with a low thermal budget. Amorphous silicon transistors have been fabricated on ultra-thin stainless steel substrates (see, for example, Ma et al., Applied Physics Letters, 74(18), 2661 (1999)) and on polyimide films (see Gleskova et al., IEEE Electron Device Letters, 20(9), 473 (1999)).

However, the polyimide used in the process described in the latter paper, sold commercially under the name "Kapton" (Registered Trade Mark) has a glass transition temperature of only about 300°C, which restricts the temperatures which can be employed during the fabrication process, and results in a less satisfactory amorphous silicon semiconductor layer. This polyimide also has a high moisture absorption (about 4 percent by weight) and such high moisture absorption can result in swelling of the substrate and consequent cracking of thin layers deposited on the substrate, or delamination of thin layers from the substrate.

Although stainless steel substrates can withstand process temperatures much higher than 300°C, such substrates require both passivation and planarization steps before transistors can be fabricated thereon. Passivation is required to ensure proper electrical isolation between adjoining metal conductors to be formed on the substrate, and to ensure that potential contaminants within the stainless steel do not diffuse into the transistors. Stainless steel substrates do, however, have the advantages of high dimensional stability and ease of handling in a manufacturing environment.

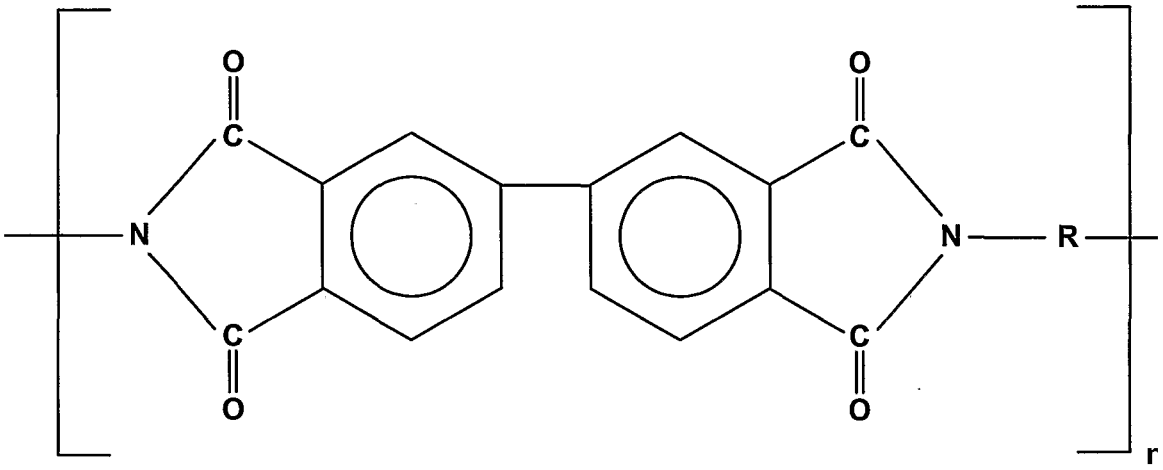
It has now been discovered that certain types of polyimides possess properties which render them very suitable for use as substrates in the fabrication of TFT's. These polyimide substrates may be used with or without a metal backing layer.

Accordingly, this invention provides a process for forming at least one transistor on a substrate by depositing on the substrate at least one layer of semiconductor material. In the present process, the substrate comprises a polyphenylene polyimide. This process is especially intended for the formation of amorphous silicon transistors, and in such a case the semiconductor material is of course an amorphous silicon.

This invention also provides a transistor formed on a substrate comprising a polyphenylene polyimide, the substrate bearing at least one transistor.

The sole Figure of the accompanying drawing is a schematic cross-section through a single transistor of a thin film transistor array formed on a polyimide substrate by the process of the present invention.

Preferred polyphenylene polyimides for use in the present process are those sold commercially under the trade names Upilex-S and Upilex-VT by UBE America, Inc., 55 East 59th Street, 18th Floor, New York NY 10022, United States of America. Both these materials are stated by the manufacturer to be of the formula:



in which R is an alkylene group. These polyimides are derivatives of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine, for example 1,6-hexamethylene diamine (formally hexane-1,6-diamine). The main difference between the two materials is that Upilex-S is a simple polyimide film, while Upilex-VT is surface-treated on one face to facilitate hot lamination of the film, without adhesive, to ceramics or metal foils. For purposes of the present invention, the Upilex VT may be laminated to a stainless steel backing film. Another preferred polyimide for use in the present process is Upilex-50SS, from the same manufacturer.

Polyphenylene polyimides have glass transition temperatures considerably higher, and water absorptions considerably lower, than those of the other polyimides previously used as transistor substrates. The commercial Upilex materials already mentioned have glass transition temperatures in excess of 400°C and water absorptions not greater than about 1.4 percent. These high glass transition temperatures allow the use of higher temperatures (greater than about 300°C, and preferably greater than about 400°C) in the fabrication process than has hitherto been possible with the polyimides previously used as transistor substrates, and these higher process temperatures result in higher quality silicon layers having higher mobility and low off-state current leakage. Polyphenylene polyimides also have the advantages of high dimensional stability during processing and smooth surfaces, which is important for the deposition of the thin layers of material used in

the formation of thin film transistors; for example, the aforementioned Upilex-50SS has a dimensional stability of about 0.01% and an average surface roughness of about 20 to 30 nm. An additional advantage of polyphenylene polyimides is their low coefficients of thermal expansion, which are typically about 2-10 x 10^{-6} $°C^{-1}$, in contrast to the 35 x 10^{-6} $°C^{-1}$ typical of the polyimides previously used. Since silicon has a coefficient of thermal expansion of about 3 x 10^{-6} $°C^{-1}$, the coefficient of a polyphenylene polyimide substrate is much more closely matched to a silicon layer deposited thereon, so that the silicon layer is much less prone to cracking and/or delamination.

The aforementioned properties of polyphenylene polyimide substrates render the present process well adapted for use in a roll-to-roll process, in which deposition of the semiconductor material is effected on a continuous web of the polyimide substrate.

As already mentioned, the polyphenylene polyimide substrate used in the present process may or may not have a metal backing layer on its surface opposite to that on which the semiconductor material is to be deposited. Such a metal backing layer is useful in enhancing the mechanical integrity of the film during the transistor fabrication process, thus avoiding, for example, any tendency for the polyimide film to stretch or otherwise distort during handling, and thus reducing distortion of the substrate during formation of the transistors thereon. In addition, a metal backing layer can act as a light barrier to decrease any unwanted photo-effects in the semiconductor material (for example, photogenerated current in an amorphous silicon film) caused by light incident on the rear surface of the polyimide film. The metal backing layer need not be continuous; this layer may have apertures extending through it to reduce its stiffness and thus give the metal-backed substrate more flexibility. If such apertures are to be provided, for obvious reasons it is desirable that they be formed in a regular pattern, and accordingly some or all of the apertures may be used for mechanical registration of the substrate with apparatus used in the fabrication process. Indeed, in some cases, a patterned metal backing layer might be used as a shadow mask for exposure of

photoresist in a patterning step during formation of the transistors on the substrate. Alternatively or in addition, it may be advantageous to incorporate a dye into the polyimide itself to refuse or eliminate such undesirable photo-effects.

As in certain prior art processes, it may be desirable to deposit a passivating layer of silica, aluminum nitride, silicon nitride or other material on the substrate prior to the deposition of the transistors on this substrate. Typically, such a passivating layer will have a thickness in the range of about 20 to about 100 nm. Passivation is useful not only for increasing the surface resistance of the polyimide surface, and thus for increasing electrical insulation between adjacent conductors, but also for increasing the dimensional stability of the substrate by preventing the substrate absorbing water during processing, and for the latter purpose it is desirable to place the passivating layer on both surfaces of the substrate. It is also desirable to heat treat ("bake") the substrate to remove water from the substrate prior to the deposition of the passivating layer; such baking will generally be carried out at a temperature of at least about 150°C for a period of at least about 1 minute, and preferably for about 3 minutes.

It may also be advantageous to post-bake the passivated substrate. According to a paper by Philips Research Laboratories entitled "AMLCDs and Electronics on Polymer Substrates" (Euro Display 1996), the shrinkage rate of a free-standing polyimide film can be reduced by two orders of magnitude after 10 hours of heating at 275°C, and by 2.4 orders of magnitude after 100 hours at the same temperature. In one specific experiment described in this paper, after 100 baking at 275°C, a polyimide film (brand not specified) shrank at 3 ppm hr^{-1}. Accordingly, if such post-baking of the passivated substrate is desired, it should be carried out at a temperature of at least 250°C for a period of at least 5 hours. It has not been determined experimentally whether these results apply the substrate in the form of a tensioned roll, nor has it been determined experimentally whether the reduction in shrinkage still applies after the pre-baked substrate is cooled, unrolled, exposed to the processing necessary to form transistors thereon, re-rolled under

tension and reheated several days later, as is necessary for formation of transistors on the substrate in a roll-to-roll process. Alternatively, the substrate could be pre-baked in a conveyor oven immediately before deposition of the layers required to form the transistor.

The surface electrical resistivity of polyphenylene polyimides is, however, so high (typically > 10^{16} Ω) that in many cases it may be possible to obtain adequate electrical insulation between adjacent conductors without such a passivating layer. If the passivating layer is omitted, it is still advantageous to bake the substrate before deposition of the semiconductor layer thereon in order to drive off water and any other volatile materials absorbed on the polyimide, thus reducing swelling of the polyimide due to water absorption and increasing the dimensional stability of the polyimide during the formation of transistors thereon. Such baking is desirably effected at a temperature greater than 250°C for a period of at least 1 hour. In one preferred embodiment described below, the substrate is heated to 350°C, close to its glass transition temperature, for a period of 4 hours.

The presently preferred embodiments of the invention described below use an inverted transistor design, in which the gate electrodes lie adjacent the substrate. To form such inverted transistors, the first step (after any passivation and/or pre-baking of the substrate in the ways already described) is the deposition of a metal layer on the substrate. The preferred metal for this purpose is chromium. It is generally preferred to deposit the chromium or other metal as a continuous film, typically having a thickness in the range of 50 to 200 nm, and thereafter to pattern the metal film, typically by conventional photolithographic techniques, prior to the deposition of the semiconductor material, to form the gate electrodes and the select lines of the transistor array to be formed. The next step in the process is normally the deposition of a layer of dielectric material, for example silicon nitride; this deposition is conveniently effected by plasma enhanced chemical vapor deposition. The semiconductor material, preferably amorphous silicon, is then deposited, again conveniently by plasma enhanced chemical vapor

deposition. As discussed in the aforementioned WO-A-00/67327, the amorphous silicon layer (and the associated dielectric layer) can, in an appropriate design, be left unpatterned so that the amorphous silicon layer extends continuously between pairs of adjacent transistors. Next, a layer of n-type silicon is deposited over the amorphous silicon, again conveniently by plasma enhanced chemical vapor deposition. Finally, normally after a cleaning step to remove residues from the chemical vapor deposition processes, a metal layer, for example an aluminum layer, is deposited over the n-type silicon layer, this metal layer conveniently being deposited by thermal evaporation. The metal layer can then be patterned to form source and drain electrodes by conventional photolithographic techniques, and the patterned metal layer used as an etch mask for a reactive ion etch of the n-type silicon layer; etching with a carbon tetrafluoride/oxygen mixture has been found satisfactory.

Preferred embodiments of the invention will now be described in more detail, though by way of illustration only, with reference to the accompanying drawing, which shows a schematic cross-section through a single transistor formed on a polyphenylene polyimide substrate by the process of the present invention.

The accompanying drawing shows a single transistor of a transistor array (generally designated 10) formed on a polyphenylene polyimide substrate 12. This substrate 12 is shown in the drawing provided with a stainless steel metal backing layer 14 through which extend regularly-spaced apertures 16, only one of which is visible in the drawing. As already mentioned, the presence of the metal backing layer 14 is optional in the process of the present invention, although such a metal backing layer does provide additional mechanical integrity to the substrate and may thus facilitate handling of the substrate, especially when the invention is to be carried out on roll-to-roll coating apparatus.

On the upper surface of the substrate 12 (as shown in the drawing), there is deposited a passivating layer 18 formed of silica or silicon nitride. As previously mentioned, the presence of such a passivating layer 18 is optional, and

in some cases the passivating layer 18 may be omitted, since the high surface resistivity of the polyphenylene polyimide provides sufficient insulation between adjacent transistors. Care should, however, be taken in eliminating the passivating layer 18 since if this layer is not present out-gassing from the polyimide substrate 12 may tend to cause delamination of various layers from this substrate.

On the upper surface of passivating layer 18, there are deposited an array of spaced metal gate electrodes 20 (only one of which is seen in the drawing), and above the electrodes 20 are deposited successively a dielectric layer 22, formed of silicon nitride, and a layer 24 of amorphous silicon. As discussed in the aforementioned WO-A-00/67327, the dielectric layer 22 and the amorphous silicon layer 24 can be left unpatterned, and avoiding the need to pattern these layers substantially reduces the cost of the transistor array. Finally, the transistor array comprises a layer 26 of n-type silicon and a metal electrode layer 28; both of these layers are patterned using any conventional process to provide the source and drain electrodes of the transistors.

A second preferred embodiment of the invention is generally similar to that described above, but used a polyimide substrate without a metal backing or passivating layer. In this second preferred embodiment, the aforementioned Upilex-50SS was first baked for 4 hours at 350°C to remove water and any other solvents present. A layer of chrome 100 nm. thick was deposited upon the baked substrate by thermal evaporation and photolithographically patterned to form the gate electrodes and select lines of the final transistor array. Next, a 320 nm. layer of silicon nitride dielectric was deposited on the substrate by plasma enhanced chemical vapor deposition (PECVD) using a silane/ammonia mixture; during this deposition, the substrate reached its maximum processing temperature of 350°C. A 160 nm layer of amorphous silicon semiconductor material was then deposited by PECVD from pure silane, followed by deposition of a 40 nm layer of n-type amorphous silicon by PECVD from a silane/phosphine mixture.

Following these PECVD steps, a layer of aluminum was deposited on the substrate and patterned photolithographically to form the source and drain

electrodes of the transistor array. The substrate was then subjected to a reactive ion etch using a carbon tetrafluoride/oxygen mixture to pattern the n-type silicon layer using the patterned aluminum layer as an etch mask; for the reasons already explained, the amorphous silicon and silicon nitride layers were not patterned during this step. Finally, a low resolution patterning step was used to pattern the amorphous silicon and silicon nitride layers to enable electrical contact to be made with the select bond line sites.

The thin film transistor array thus fabricated can be used directly in the manufacturer of an electrophoretic display, or other types of display, without further processing. For example, the thin film transistor array shown in the drawing could be incorporated into an electrophoretic display by the process described in WO-A-00/36465; the entire disclosure of this co-pending application is herein incorporated by reference. In some cases, it is desirable to provide a barrier layer covering the thin film transistors to protect the transistors against the effects of solvents or other materials which may tend to diffuse out of the electrophoretic display.

The thin film transistor arrays produced by the process of the present invention are especially intended for use in electrophoretic displays, especially encapsulated electrophoretic displays such as those described in U.S. Patents Nos. 5,930,026; 5,961,804; 6,017,584; 6,067,185; 6,118,426; 6,120,588; 6,120,839; 6,124,851; 6,130,773; 6,130,774; and 6,172,798, and in International Applications Publication Nos. WO 97/04398; WO 98/03896; WO 98/19208; WO 98/41898; WO 98/41899; WO 99/10769; WO 99/10768; WO 99/10767; WO 99/53373; WO 99/56171; WO 99/59101; WO 99/47970; WO 00/03349; WO 00/03291; WO 99/67678; WO 00/05704; WO 99/53371; WO 00/20921; WO 00/20922; WO 00/20923; WO 00/26761; WO 00/36465; WO 00/38000; WO 00/38001; WO 00/36560; WO 00/20922; WO 00/36666; WO 00/59625; WO 00/67110; WO 00/67327 and WO 01/02899. The entire disclosures of all these patents and published applications are herein incorporated by reference.

Numerous changes and modifications can be made in the preferred embodiments of the present process already described without departing from the spirit and skill of the invention. For example, the present invention is not restricted to the fabrication of bottom gate transistors such as that shown in the accompanying drawings, the court also be used in the fabrication of top gate transistors, in which the source and drain electrodes are first fabricated on the substrate (with or without a passivating layer), then an amorphous silicon layer and a dielectric layer are formed on top of the electrodes, and finally the gate electrodes are formed as the top layer of the structure. Accordingly, the foregoing description is to be construed in an illustrative and not in a limitative sense.

From the foregoing, it will be seen that the process of the present invention provides a process for forming transistors on a flexible substrate which permits the use of higher processing temperatures than prior art processes, and which can thus produce semiconductor layers of higher quality than prior art processes. The substrate used in the present process has a coefficient of thermal expansion which closely matches that of most semiconductor layers, so reducing the risk of cracking and/or delamination of the semiconductor layer due to differences in thermal expansion between this layer and the substrate. The present invention provides a process which is well-adapted to roll-to-roll operation, and thus the present process is very suitable for the fabrication of large area transistor arrays on flexible substrates.

CLAIMS

1. A process for forming at least one transistor (10) on a substrate (12), which process comprises depositing on the substrate (12) at least one layer of semiconductor material (24, 26), characterized in that the substrate (12) comprises a polyphenylene polyimide.

2. A process according to claim 1 characterized in that the polyphenylene polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.

3. A process according to claim 2 characterized in that the polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine.

4. A process according to any one of the preceding claims characterized in that a passivating layer (18) is deposited on one or both surfaces of the substrate (12) before the semiconductor material (24, 26) is deposited thereon.

5. A process according to claim 4 characterized in that the passivating layer (18) comprises silicon dioxide or aluminum nitride, and/or has a thickness in the range of 20 to 100 nm.

6. A process according to claim 4 or 5 characterized in that the substrate (12) is heated to a temperature greater than 150°C for a period of at least 1 minute before deposition of the passivating layer (18).

7. A process according to any one of claims 4 to 6 characterized in that the substrate (12) is heated to a temperature greater than 250°C for a period of at least 5 hours after deposition of the passivating layer (18).

8. A process according to any one of the preceding claims characterized in that the substrate (12) is heated to a temperature greater than 250°C for a period of at least 1 hour before deposition of the semiconductor material (24, 26).

9. A process according to any one of the preceding claims characterized in that the substrate (12) comprises a metal layer (14) on the side thereof remote from the semiconductor material (24, 26).

10. A process according to claim 9 characterized in that the metal layer (14) has apertures (16) extending therethrough.

11. A process according to any one of the preceding claims characterized in that the deposition of the semiconductor material (24) is effected at a temperature in excess of 300°C.

12. A process according to any one of the preceding claims characterized in that the semiconductor material (24) comprises amorphous silicon.

13. A process according to claim 12 characterized in that the amorphous silicon is not patterned so that it extends continuously between at least some pairs of adjacent transistors.

14. A process according to any one of the preceding claims characterized in that deposition of the semiconductor material (24, 26) is effected on a continuous web of substrate (12).

15. A substrate (12) comprising a polyphenylene polyimide, the substrate bearing at least one transistor (10).

16. A substrate according to claim 15 characterized by any one or more of the features defined in any of claims 2 to 14.