

LAYOUT METHOD AND DEVICE FOR INTEGRATED CIRCUIT

ABSTRACT

The present application relates to a layout method and device for an integrated circuit. The layout method for an integrated circuit comprises the following steps: providing a layout that comprises a first element region and a second element region, there being a spacing region between the first element region and the second element region; and detecting whether the width of the spacing region is less than a preset width, and if yes, labeling at least one of the first element region, the second element region, and the spacing region, the preset width being a minimum width that satisfies a requirement, and the requirement being loading at least one virtual pattern in the spacing region. The present application allows for quick and accurate positioning of an element region, which is not placed at a good position, in a layout, improves of layout efficiency of integrated circuits and layout precision, and lays a foundation for improving the quality of photolithography, shortening integrated circuit development cycles, improving the yield of semiconductor products.

[Fig. 1]