

CLAIMS:

1. A semiconductor processing method comprising:
forming a silicon oxide material on exposed surfaces of a processing region of a semiconductor processing chamber;
forming a silicon nitride material overlying the silicon oxide material;
5 performing a deposition process on a semiconductor substrate disposed within the processing region of the semiconductor processing chamber; and
performing a chamber cleaning process.
2. The semiconductor processing method of claim 1, wherein the deposition process comprises a carbon-containing hardmask film.
- 10 3. The semiconductor processing method of claim 1, wherein the silicon oxide material and the silicon nitride material are formed on a substrate support within the processing region of the semiconductor processing chamber.
4. The semiconductor processing method of claim 3, further comprising:
positioning the semiconductor substrate on the substrate support prior to
15 performing the deposition process, wherein the semiconductor substrate is positioned on the silicon nitride material formed on the substrate support.
5. The semiconductor processing method of claim 1, wherein the chamber cleaning process comprises a plasma enhanced clean with a halogen-containing precursor.
6. The semiconductor processing method of claim 1, wherein the
20 semiconductor substrate is disposed on a substrate support comprising a bipolar electrostatic chuck having a planar support surface.
7. The semiconductor processing method of claim 1, wherein the silicon oxide material is formed to a first thickness, and wherein the silicon nitride material is formed to a second thickness greater than the first thickness.
- 25 8. A semiconductor processing method comprising:

performing a chamber cleaning process in a processing region of a semiconductor processing chamber;

forming a silicon oxide material on exposed surfaces of the processing region of the semiconductor processing chamber;

5 forming a silicon nitride material overlying the silicon oxide material;

 providing a semiconductor substrate to a substrate support positioned in the processing region of the semiconductor processing chamber; and

 performing a deposition process on the semiconductor substrate.

9. The semiconductor processing method of claim 8, wherein the deposition
10 process comprises a tungsten carbide hardmask film.

10. The semiconductor processing method of claim 8, wherein the silicon oxide material and the silicon nitride material are formed on the substrate support prior to providing the semiconductor substrate to the substrate support.

11. The semiconductor processing method of claim 8, wherein the silicon
15 oxide material is formed to a first thickness less than or about 20 nm, and wherein the silicon nitride material is formed to a second thickness greater than or about 50 nm.

12. The semiconductor processing method of claim 8, wherein the substrate support is a bipolar electrostatic chuck characterized by a first surface on which the semiconductor substrate is positioned, and wherein the first surface is substantially planar across
20 a diameter of the first surface.

13. A semiconductor processing method comprising:
 forming a silicon oxide material to a first thickness on interior surfaces of a processing region of a semiconductor processing chamber;
 forming a silicon nitride material overlying the silicon oxide material, wherein the
25 silicon nitride material is formed to a second thickness greater than the first thickness;
 providing a semiconductor substrate to a substrate support positioned in the processing region of the semiconductor processing chamber; and
 forming a tungsten-containing material on the semiconductor substrate.

14. The semiconductor processing method of claim 13, further comprising:
removing the semiconductor substrate from the semiconductor processing
chamber; and

5 performing a chamber cleaning process in the processing region of the
semiconductor processing chamber.

15. The semiconductor processing method of claim 13, wherein the substrate
support is a bipolar electrostatic chuck characterized by a first surface on which the
semiconductor substrate is positioned, and wherein the first surface is substantially planar and
free of edge rings and alignment tabs on the first surface of the substrate support.

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