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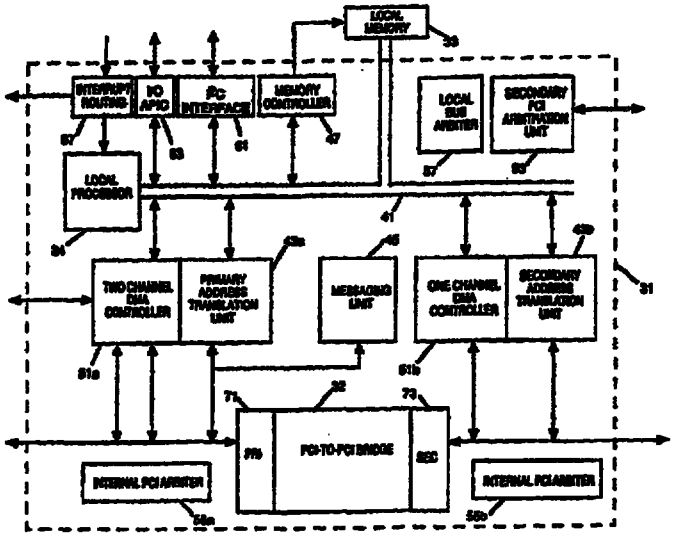
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(54) Title: ARCHITECTURE FOR AN I/O PROCESSOR THAT INTEGRATES A PCI TO PCI BRIDGE



(57) Abstract

A multi-functional device (31) that integrates a high performance processor to a PCI to PCI bus bridge (32). The invention consolidates a high performance processor, a PCI to PCI bus bridge (32), PCI bus-processor address translation units (43a, 43b), direct memory access (DMA) controllers (51a, 51b), memory controller (47), secondary PCI bus arbitration unit (53), inter-integrated (12C) circuit bus interface unit (61), advanced programmable interrupt (APIC) bus interface unit (63), and a messaging unit (45) into a single system which utilizes a local memory (33). The PCI bus is an industry standard high performance, low latency system bus. The PCI to PCI bridge (32) provides a connection path between two independent 32-bit PCI buses and provides the ability to overcome PCI electrical loading limits. The addition of the local processor (34) brings intelligence to the PCI bus bridge (32).