ABSTRACT

Provided herein is a memory device that may include a plurality of memory cells coupled to a plurality of bit lines and a common source line. The memory device may also include a control circuit configured to control a peripheral circuit to perform a program operation that includes two or more program steps on selected memory cells of a selected word line. The peripheral circuit may be configured to perform a first program step of the two or more program steps on the selected memory cells, then perform a detrap operation that applies a detrap voltage to the plurality of bit lines and the common source line for a predefined time, and thereafter perform a second program step of the two or more program steps on the selected memory cells.

FIG. 1