SEMICONDUCTOR DEVICE AND PROCESS THEREFOR

Abstract of the Disclosure

At least one process-assist feature (210, 70, 706, 806, 506, 406, 608, 904, 1106, 1108, 1206, 1208) at or near a via location of a wiring structure (75, 700, 800, 500, 400, 614, 908, 1205) within a semiconductor device is used to improve processing or processing margin during subsequent processing. For at least some of the embodiments of the present invention, the process-assist features feature (210, 70, 706, 806, 506, 406, 608, 904, 1106, 1108, 1206, 1208) help to make a flowable layer more uniform over via locations (84, 74, 704, 804, 504, 404, 603, 904, 1104, 1204). Typically, this can help in the formation of via openings. When a resist layer (204) is formed over the process-assist features, the resist layer (204) will have a more uniform thickness over most via locations within the device. When an insulating layer (197) is formed over the via locations, the insulating layer (107) will have a more uniform thickness over most via locations within the device. More control during resist exposure or via opening etching allow more process margin. The embodiments described herein illustrate the flexibility in placing process-assist features.

FIG. 16 to accompany abstract.