CLAIMS

What is claimed is:

1. A photonics device, comprising:

a photonics dielectric stack on a substrate, the photonics dielectric stack including a dielectric layer and one or more photonics devices having a photosensitive material formation;

a first dielectric material layer with a first portion thereof formed over the photosensitive material formation, and a second portion thereof formed over the dielectric layer of the dielectric stack;

an etch stop layer over the first layer of dielectric material; and

a second dielectric material layer over the etch stop layer, the second dielectric material layer including an etched trench over the photosensitive material formation wherein a bottom of the trench is delimited by the photosensitive material formation.

2. The device of claim 1, wherein the etched trench is formed by plasmaless etching.

3. The device of claim 1, wherein the photosensitive material formation is germanium.

4. The device of claim 1, wherein the etch stop layer is patterned such that a light signal propagating within the photonics device is coupled to the etch stop layer.

5 The device of claim 1, further including an aluminum deposit within the trench having a planarized top surface thereof such that that top surface is defined by, at least, the dielectric stack and the aluminum deposit.

6. The device of claim 5, further including a metallization layer formation over the aluminum deposit and in electrical communication therewith.

7. The device of claim 6, further including a termination metallization layer formation at an elevation higher than an elevation of the metallization layer formation, the

termination metallization layer formation in electrical communication with the metallization layer.

8. A photonics device, comprising:

a photonics dielectric stack on a substrate and including a dielectric layer, the photonics dielectric stack including one or more photonics devices having a photosensitive material formation;

a first dielectric material layer with a first portion thereof formed over the photosensitive material formation, and a second portion thereof formed over the dielectric layer of the dielectric stack;

an etch stop layer over the first layer of dielectric material;

a second dielectric material layer on the etch stop layer, the second dielectric material layer including an etched trench over the photosensitive material formation such that a bottom of the trench is delimited by the photosensitive material formation, the trench further including an upper region of wider diameter and a lower region of narrower diameter, the trench further including an aluminum deposit including a top surface thereof that is atomically smooth and planar, the top surface defined by a dielectric layer of the photonics dielectric stack and the aluminum.

9. The device of claim 8, wherein the photonics device further having a bottom elevation thereof that is higher than an elevation of the planar top surface of the aluminum deposit.

10. The device of claim 9, further including:

one or more dielectric layers over the planar top surface;

a layer of waveguiding material over the one or more dielectric layers such that the layer of waveguiding material patterns defines the photonics device.

11. The device of claim 10, wherein the waveguiding material is patterned to define a waveguide formed by a range of elevations between the upper region and lower region of the trench.

12. The device of claim 8, further including a barrier layer comprised of a copper metallization layer, and wherein the trench is formed from etching through the barrier layer.

13. A photonics device, comprising:

a first photonics device formed by a first waveguiding layer comprised of a waveguiding material over a substrate;

a first dielectric layer over the first waveguiding layer, the first dielectric layer having an atomically smooth surface;

a second dielectric layer over the atomically smooth surface of the first dielectric layer, the second dielectric layer having an atomically smooth dielectric surface; and

a second waveguiding layer comprised of a waveguiding material over the atomically smooth dielectric surface of the second dielectric layer, the second waveguiding layer patterned to define a second photonics device.

14. The device of claim 13, wherein the first and second waveguiding layers are patterned by anisotropic etching such that each of the first and second photonics devices includes a vertically extending sidewall.

15. The device of claim 13, wherein the first and second waveguiding layers are patterned by a reactive ion etching process that includes an iterative etch step followed by an iterative deposit step such that each of the first and second photonics devices includes a vertically extending sidewall.

16. The device of claim 13, wherein the first and second waveguiding layers are patterned layer to define a plurality of dummy form shapes, the dummy form shapes being spaced apart from the each of the first and second photonics devices.

17. The device of claim 13, wherein:

the first dielectric layer is formed by a silane-based high density plasma chemical vapor deposition such that the first dielectric layer is formed of silane based HDP oxide, and

the second dielectric layer is formed over the atomically smooth surface by using PECVD such that the second dielectric layer is formed of TEOS.

18. The device of claim 13, further comprising:

a third dielectric layer deposited over the second photonics device, the third dielectric layer including a polished surface;

a fourth dielectric layer over the polished surface of the third dielectric layer, the fourth dielectric layer including a polished dielectric surface; and

a third waveguiding layer over the polished dielectric surface of the fourth dielectric layer, the third waveguiding layer patterned to define a third photonics device.

19. The device of claim 13, wherein the first dielectric layer is formed from a first dielectric layer formation process, and the second dielectric layer is formed from a second dielectric layer formation process that is different from the first dielectric layer formation process.

20. The device of claim 18, wherein the third dielectric layer is formed from a third dielectric layer formation process, and the fourth dielectric layer is formed from a fourth dielectric layer formation process that is different from the third dielectric layer formation process.

CLAIMS

What is claimed is:

1. A method comprising:

depositing a layer of dielectric material so that a first portion of the layer of dielectric material is formed on a photosensitive material formation and so that a second portion of the layer of dielectric material is formed on a dielectric layer of a dielectric stack of a photonics structure having one or more photonics device;

depositing an etch stop layer on the layer of dielectric material;

forming a dielectric material layer on the etch stop layer;

performing first etching of the dielectric material layer selective to the etch stop layer to define a trench over the photosensitive material formation;

performing second etching of the etch stop layer, wherein the second etching removes material of the etch stop layer through a thickness of the etch stop layer and material of the layer of dielectric material through a portion of a thickness of the layer of dielectric material, the second etching increasing a depth of the trench; and

performing plasmaless etching of a remaining thickness of the layer of dielectric material to reveal the photosensitive material formation so that a bottom of the trench is delimited by the photosensitive material formation.

2. The method of claim 1, wherein the performing plasmaless etching includes performing of a remote plasmaless etch.

3. The method of claim 1, wherein the removing of the material of the layer of dielectric material includes performing of a remote plasmaless etch that is selective to germanium.

4. The method of claim 1, wherein the photosensitive material is germanium.

5. The method of claim 1, wherein prior to the depositing the layer of dielectric material, performing CMP planarizing so that the photosensitive material and the dielectric layer define a horizontally extending planar surface, and performing CMP polishing so that the photosensitive material and the dielectric layer define an atomically smooth surface.

6. The method of claim 1, wherein prior to the depositing the layer of dielectric material, performing CMP planarizing so that that the photosensitive material defines a horizontally extending

planar surface, and performing CMP polishing so that the photosensitive material defines an atomically smooth surface.

7. The method of claim 1, wherein the method includes depositing aluminum to overfill the trench and performing planarization to planarize an overfill portion so that a defined top surface is partially defined by the dielectric stack and partially defined by the aluminum.

8. The method of claim 1, wherein the method includes patterning the etch stop layer so that no light signal propagating within the photonics structure is coupled to the etch stop layer.

9. The method of claim 1, wherein the method includes patterning the etch stop layer so that the etch stop layer is optically isolated from one or more of the following selected from the group consisting of (a) one or more photonics device of the photonics structure; (b) a certain photonics device of the photonics structure, (c) a plurality of photonics devices of the photonics structure, and (d) each photonics device of the photonics structure.

10. The method of claim 1, wherein the method includes depositing aluminum to overfill the trench, and performing planarization to planarize an overfill portion so that a defined top surface is partially defined by the dielectric stack and partially defined by the aluminum, wherein the method includes fabricating a metallization layer formation over and aligned with a conductive material formation defined by the aluminum deposited in the trench, the metallization layer formation comprising copper and being in electrical communication with the conductive material formation.

11. The method of claim 1, wherein the method includes depositing aluminum to overfill the trench, and performing planarization to planarize an overfill portion so that a defined top surface is partially defined by the dielectric stack and partially defined by the aluminum, wherein the method includes fabricating a metallization layer formation over and aligned with the aluminum, the metallization layer formation comprising copper and being in electrical communication with a conductive material formation defined by the aluminum deposited in the trench, and wherein the method includes fabricating a termination metallization layer formation at an elevation higher than an elevation of the metallization layer formation, the termination metallization layer formation formed of aluminum and being in electrical communication with the conductive material formation, and the metallization layer formation.

12. The method of claim 1, wherein the method includes depositing aluminum to overfill the trench, and performing planarization to planarize an overfill portion so that a defined top surface is partially defined by the dielectric stack and partially defined by the aluminum, wherein the method includes fabricating a metallization layer formation over and aligned with the aluminum, the metallization layer formation comprising copper and being in electrical communication with a conductive material formation defined by aluminum deposited in the trench, and wherein the method includes fabricating a termination metallization layer formation at an elevation higher than an

elevation of the metallization layer formation, the termination metallization layer formation formed of aluminum and being in electrical communication with the conductive material formation, and the metallization layer formation, wherein the method includes fabricating a termination including an under bump metallization formation on the termination metallization layer.

13. A method comprising:

depositing one or more layer, wherein the depositing one or more layer includes one or more dielectric layer to extend an elevation of a dielectric stack, wherein a portion of the one or more layer is formed over a conductive material formation and a portion of the one or more layer is formed over dielectric material defining the dielectric stack;

etching the dielectric stack to define a trench, the trench being aligned to the conductive material formation;

further etching the dielectric stack to widen an upper region of the trench so that the trench has an upper region of wider diameter and a lower region of narrower diameter;

depositing in a single deposition stage aluminum into the trench so that with performance the single deposition stage the lower region and the upper region are filled with aluminum, wherein the depositing is performed so that the aluminum overfills the trench; and

planarizing an overfill portion of the aluminum so that a top surface of a photonics structure having the dielectric stack in an intermediary stage of fabrication on completion of the planarizing has an atomically smooth planar top surface defined by dielectric material of the dielectric stack and the aluminum.

14. The method of claim 13, wherein the method includes subsequently to the planarizing extending an elevation of the dielectric stack and integrally fabricating a photonics device within the dielectric stack, the photonics device having a bottom elevation higher than an elevation of the planar top surface.

15. The method of claim 13, wherein the method includes subsequently to the planarizing extending an elevation of the dielectric stack and fabricating a photonics device within the dielectric stack, the photonics device having a bottom elevation higher than an elevation of the planar top surface, wherein the fabricating the photonics device includes depositing and planarizing one or more dielectric layer over the planar top surface, depositing a layer of waveguiding material over the one or more dielectric layer, pattering the layer of waveguiding material to define the photonics device and depositing and planarizing one or more dielectric layer over the waveguide.

16. The method of claim 13, wherein the depositing one or more layer includes depositing a layer formed of waveguiding material, wherein the method includes patterning the waveguiding material to define a waveguide that occupies a range of elevations that include elevations that are between a top elevation of the trench and a bottom elevation of the trench.

17. The method of claim 13, wherein the etching the dielectric stack to define the trench includes etching through a barrier layer the barrier layer being formed on a copper metallization layer.

18. A method comprising:

patterning a first layer to define one or more photonics device;

performing ion implantation to define one or more ion implantation region in the first layer;

depositing one or more dielectric material layer over the first layer;

etching the one or more dielectric material layer to define one or more trench in the one or more dielectric layer so that a bottom of a first trench of the one or more trench is aligned to a certain ion implantation region of the one or more ion implantation region; and

filling the one or more trench, wherein the filling includes filling the first trench with conductive material so that the conductive material is in electrical communication with the certain ion implantation region, and wherein the conductive material includes aluminum.

19. The method of claim 18, wherein the patterning a first layer to define one or more photonics device includes patterning the first layer to define first and second photonics devices, wherein the etching the one or more dielectric material layer to define one or more trench includes etching the one or more dielectric material layer to define the first trench and a second trench, and wherein the filling includes filling the first trench and the second trench, the first trench aligned to an ion implantation region of the first photonics device, the second trench aligned to an ion implantation region of the second photonics device, wherein the filling the second trench includes filling the second trench with material selected from the group consisting of tungsten and copper.

20. The method of claim 18, wherein the patterning a first layer to define one or more photonics device includes patterning a first layer to define a first photonics device, wherein the patterning a first layer to define one or more photonics device includes patterning the first layer to define first and second photonics devices, wherein the etching the one or more dielectric material layer to define one or more trench includes etching the one or more dielectric material layer to define the first trench and a second trench, and wherein the filling includes filling the first trench and the second trench, the first

trench aligned to an ion implantation region of the first photonics device, the second trench aligned to an ion implantation region of the second photonics device, wherein the filling the second trench includes filling the second trench with material selected from the group consisting of tungsten and copper, the first photonics device being a photodetector, the second photonics device being a modulator.

21. The method of claim 18, wherein the patterning a first layer to define one or more photonics device includes patterning a first layer to define a first photonics device, wherein the etching the one or more dielectric material layer to define one or more trench includes etching the one or more dielectric material layer to define a first trench and a second trench, and wherein the filling includes filling the first trench and the second trench, the first trench aligned to an ion implantation region of the first photonics device, the second trench aligned to a second ion implantation region of the first photonics device, wherein the filling the second trench includes filling the second trench with material selected from the group consisting of tungsten and copper.

22. The method of claim 18, wherein the patterning a first layer to define one or more photonics device includes patterning a first layer to define a first photonics device, wherein the etching the one or more dielectric material layer to define one or more trench includes etching the one or more dielectric material layer to define a first trench and a second trench, and wherein the filling includes filling the first trench and the second trench, the first trench aligned to an ion implantation region of the first photonics device, the second trench aligned to a second ion implantation region of the first photonics device, wherein the filling the second trench includes filling the second trench with material selected from the group consisting of tungsten and copper, wherein the first photonics device is a photonics device selected from the group consisting of a photodetector and a modulator.

23. The method of claim 18, wherein the first layer is a silicon layer of a prefabricated silicon on insulator (SOI) wafer having a substrate, and insulator layer, and the silicon layer.

24. The method of claim 18, wherein the conductive material filled in the first trench defines a conductive materials formation comprising aluminum, wherein the method includes fabricating a metallization layer formation over and aligned with the conductive material formation, the metallization layer formation comprising copper and being in electrical communication with the conductive material formation.

25. The method of claim 18, wherein the conductive material filled in the first trench defines a conductive material formation comprising aluminum, wherein the method includes fabricating a metallization layer formation over and aligned with the conductive material formation, the metallization layer formation comprising copper and being in electrical communication with the conductive material formation, and wherein the method includes fabricating a termination metallization layer formation at an elevation higher than an elevation of the metallization layer

formation, the termination metallization layer formation formed of aluminum and being in electrical communication with the conductive material formation, and the metallization layer formation.

26. A method comprising:

patterning a waveguiding layer to define a photonics device, the waveguiding layer formed of a waveguiding material;

depositing a dielectric layer on the photonics device;

subjecting the dielectric layer to chemical mechanical planarization to reduce an elevation of the dielectric layer and subjecting the dielectric layer to chemical mechanical polishing so that the dielectric layer defines an atomically smooth surface;

depositing a second dielectric layer on the atomically smooth surface;

subjecting the second dielectric layer to chemical mechanical planarization to reduce an elevation of the second dielectric layer and subjecting the second dielectric layer to chemical mechanical polishing so that the second dielectric layer defines an atomically smooth dielectric surface;

depositing a second waveguiding layer over the atomically smooth dielectric surface; and

patterning the second waveguiding layer to define a second photonics device.

27. The method of claim 26, wherein the patterning the waveguiding layer includes patterning the waveguiding layer to define a plurality of dummy form shapes, the dummy form shapes being spaced apart from the photonics device and having heights in common with a height of the photonics device.

28. The method of claim 26, wherein the patterning the waveguiding layer includes performing anisotropic etching so that the photonics device features a vertically extending sidewall.

29. The method of claim 26, wherein the patterning the waveguiding layer includes performing a reactive ion etching process that comprises an iterative etch step followed by an iterative deposit step so that the photonics device features vertically extending sidewall.

30. The method of claim 26, wherein the patterning the waveguiding layer includes patterning the waveguiding layer to define a plurality of dummy form shapes, the dummy form shapes being spaced apart from the photonics device and having heights in common with a height of the photonics device, wherein the patterning the waveguiding layer includes performing a reactive ion etching process that comprises an iterative etch step followed by an iterative deposit step so that the photonics device features vertically extending sidewall.

31. The method of claim 26, wherein the depositing the dielectric layer over the photonics device includes using a silane based high density plasma chemical vapor deposition so that the dielectric layer is formed of silane based HDP oxide, and wherein the depositing the second dielectric layer over the atomically smooth surface includes using PECVD so that the second dielectric layer is formed of TEOS.

32. The method of claim 26, wherein the method includes: depositing a third dielectric layer on the second photonics device; subjecting the third dielectric layer to chemical mechanical planarization to reduce an elevation of the dielectric layer and subjecting the third dielectric layer to chemical mechanical polishing so that the dielectric layer defines a polished surface; depositing a fourth dielectric layer on the polished surface; subjecting the fourth dielectric layer to chemical mechanical planarization to reduce an elevation of the fourth dielectric layer and subjecting the second dielectric layer to chemical mechanical polishing so that the fourth dielectric layer defines a polished dielectric surface; depositing a third waveguiding layer over the polished dielectric surface; and patterning the third waveguiding layer to define a third photonics device, wherein the depositing the dielectric layer over the photonics device includes using a silane based high density plasma chemical vapor deposition so that the dielectric layer is formed of silane based HDP oxide, and wherein the depositing the third dielectric layer on the second photonics device includes using PECVD so that the second dielectric layer is formed of TEOS.

33. The method of claim 26, wherein the depositing the dielectric layer over the photonics device includes using a first dielectric layer formation process, and wherein the depositing the second dielectric layer over the atomically smooth surface includes using a second dielectric layer formation process.

34. The method of claim 26, wherein the method includes: depositing a third dielectric layer on the second photonics device; subjecting the third dielectric layer to chemical mechanical planarization to reduce an elevation of the dielectric layer and subjecting the third dielectric layer to chemical mechanical polishing so that the dielectric layer defines a polished surface; depositing a fourth dielectric layer on the polished surface; subjecting the fourth dielectric layer to chemical mechanical planarization to reduce an elevation of the fourth dielectric layer and subjecting the second dielectric layer to chemical mechanical polishing so that the fourth dielectric layer defines a polished dielectric surface; depositing a third waveguiding layer over the polished dielectric surface; and patterning the third waveguiding layer to define a third photonics device, wherein the depositing the dielectric layer over the photonics device includes using a first dielectric material formation process, and wherein the depositing the third dielectric layer on the second photonics device includes using a second dielectric material formation process.