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"A voltage controlled variable gain circuit and a signal transmission circuit incorporating same".

The present invention relates to a voltage controlled variable gain circuit and a signal transmission circuit incorporating the same.

A voltage controlled variable gain circuit is shown in Figure 1 of the accompanying drawings in which the gain is varied logarithmically linearly in accordance as the control voltage V_c is changed has been known as shown, for example, in a Japanese magazine entitled NIKKEI ELECTRONICS (pp 118 - 140, November 13, 1978).

In this known voltage controlled variable gain circuit, the inverting input terminal (-) of an operational amplifier circuit 21 is connected to an input terminal T_{IN} while the non-inverting terminal (+) is connected to earth. The output V_1 from the operational amplifier circuit 21 is subjected to a level shift by batteries 22 and 23. Two voltages thus shifted are applied to emitter electrodes of PNP transistors Q_2 and Q_4 and emitter electrodes of NPN transistors Q_3 and Q_4 . The base electrodes of the transistors Q_2 and Q_3 are connected to earth, whilst the gain controlling voltage V_c is applied on the base electrodes of the transistors

Q_4 and Q_1 .

Thus, the base-emitter connections of the four transistors $Q_1 - Q_4$ are formed as a bridge circuit network between the circuit connection points T_1 , T_2 , T_3 and T_4 .

The collector electrodes of the transistors Q_1 and Q_2 are connected to each other and also to the inverting input terminal (-) of the operational amplifier circuit 21.

The collector electrodes of the transistors Q_3 and Q_4 are connected to each other and also to a load resistor R_L .

The relationship between the input current i_{in} and the output current i_{out} in this known voltage control variable gain control circuit is given by the following equation, provided that factors of the transistors $Q_1 - Q_4$ such as V_{BE} (voltage differential between base and emitter) - I_E (emitter current) characteristic, reverse saturation current I_S , current amplification factor and so forth are equal.

$$\frac{i_{out}}{i_{in}} = \exp \frac{q(-V_c)}{KT} \quad (1)$$

Therefore, the output current i_{out} is changed logarithmically linearly in accordance with the change of the control voltage V_c .

We have found that when this known voltage controlled variable gain circuit is formed into a semi-

conductor integrated circuit, the integrated voltage control variable gain circuit exhibits a high distortion factor because of the following reason.

5 The waveform of the voltages VT_1 , VT_3 at the junction points T_1 and T_3 in the circuit of Figure 1, in response to the output V_1 from the operational amplifier circuit 21, take the same phase, as will be seen from Figures 2(a) and 2(b) of the accompanying drawings.

10 On the other hand, in the semiconductor integrated circuit, the NPN and PNP transistors are usually made in the form of vertical type NPN transistor and lateral type PNP transistor in a monolithic semiconductor integrated circuit.

15 In the formation of the vertical type NPN transistor and lateral type PNP transistor in a semiconductor integrated circuit, as is well known to those skilled in the art from the disclosure in United States Patent No. 3,197,710 the introduction of P type impurity for forming the P type base region of vertical type NPN transistor and introduction of P type impurity for forming
20 the P type emitter and collector of the lateral type PNP transistor are effected simultaneously. Also, the introduction of N type impurity for forming N^+ type emitter region of vertical type NPN transistor is made

simultaneously with the introduction of the N type impurity for the formation of N^+ type base ohmic contact region of the lateral type PNP transistor.

It is, therefore, possible to form a plurality of vertical type NPN transistors and a plurality of lateral type PNP transistors in a single semiconductor integrated circuit by a comparatively simple method.

On the other hand, in order to improve various characteristic parameters of the lateral type PNP transistor in

the integrated circuit, it is possible to obtain a modified lateral type PNP transistors having an improved emitter injection efficiency by further introducing P type impurity at a high density into the P type emitter region. The PNP transistor of a circuit type earthed

at the collector can be formed using a substrate type PNP transistor which makes use of the P type substrate of a bipolar integrated circuit as the collector region.

Therefore, the characteristic parameters of a plurality of NPN transistors formed in the integrated circuit conform at a comparatively high degree of accuracy, and similarly, the characteristic parameters of a plurality of PNP transistors formed in the integrated circuit conform at a comparatively high degree of accuracy. However, the average characteristic

parameters of a plurality of NPN transistors and a plurality of PNP transistors do not conform with each other, because of differences in the construction and the manufacturing process.

5 As the examples of disconformity of the characteristic parameters between the NPN transistors and PNP transistors in the integrated circuit, it is possible to list disconformities of characteristic parameters which are quite important in the bipolar
10 transistors such as base spreading resistance $r_{bb'}$, forward characteristic between base and emitter ($V_{BE}-I_E$ characteristic, emitter dynamic resistance r_e), common-emitter current amplification factor h_{FE} , cut-off frequency f_T and so forth.

15 In the known voltage controlled variable gain circuit shown in Figure 1, the conductivity of the PNP transistor Q_4 is increased during the period of positive half cycle of the voltage waveform V_{T1} applied to the circuit junction point T_1 to permit a collector current
20 i_4 to flow through this transistor, whereas the NPN transistor Q_3 increases its conductivity in the period of negative half cycle of the voltage waveform V_{T3} applied to the circuit junction point T_3 to permit the collector current i_3 to flow therethrough.

The following problems and disadvantages occur when this known voltage controlled variable gain circuit is constructed in the form of a semiconductor integrated circuit. The instantaneous value of the collector current i_4 of the PNP transistor Q_4 becomes smaller than the instantaneous value of the collector current i_3 of the NPN transistor Q_3 , due to the discordance of the characteristic parameter between the PNP transistor and the NPN transistors, even if the instantaneous voltages of the positive and negative half cycles of the voltage waveforms V_{T1} and V_{T3} are equal. In consequence, the instantaneous values of the waveform of the output current $i_{out} (= i_3 + i_4)$ in the positive and negative half cycles are different. The difference of waveform of the output current i_{out} between the positive and negative half cycles produces, across the load resistor R_L , an output V_{out} having a high distortion factor containing even higher harmonics of frequencies which is an even number times as high as the frequency of the fundamental wave, as shown in Figure 2d

A distorted waveform i having small instantaneous value i (+) of positive half cycle and large instantaneous value i (-) of negative half cycle is

obtained. This distorted waveform i can be developed into a Fourier series as follows. It will be seen that this distorted waveform includes even higher harmonics.

$$\begin{aligned}
 i = & i_{(+)} \sin \omega t + \frac{i_{(-)} - i_{(+)}}{2} + \frac{2(i_{(-)} - i_{(+)})}{2} \sin \omega t \\
 & - \frac{2(i_{(-)} - i_{(+)})}{\pi} \left[\frac{\cos 2\omega t}{3} + \frac{\cos 4\omega t}{15} + \dots \right. \\
 & \left. + \frac{\cos 2n\omega t}{4n^2 - 1} + \dots \right] \dots\dots (2)
 \end{aligned}$$

Japanese Patent Publication No. 101,859/73

proposes two gain control circuits employing diodes, the two circuits being connected to both inputs of a differential amplifier to cancel the influences of higher harmonics, in order to reduce the higher harmonic distortion, particularly the secondary distortion, of the diode in a variable gain circuit making use of diodes.

Furthermore, a technique similar to that proposed by the above-mentioned Japanese Patent Publication No. 101,859/73 is disclosed in United States Patent Specification No. 4,155,047.

According to the present invention there is provided a voltage controlled variable gain circuit constructed as a semiconductor integrated circuit including:

- (a) a first operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal leading out of said semiconductor integrated circuit to
5 act as a first input terminal of said semiconductor integrated circuit, said non-inverting input terminal being connected to a reference potential outside said semiconductor integrated circuit;
- (b) a second operational amplifier circuit having an
10 inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal leading out of said semiconductor integrated circuit to act as a second input terminal of said semiconductor integrated circuit, said non-inverting input terminal
15 being connected to said reference potential outside said semiconductor integrated circuit;
- (c) a first gain control section connected to the output terminal of the second operational amplifier circuit within said semiconductor integrated circuit and
20 having an input terminal, a control input terminal and an output terminal, said input terminal being electrically connected to said inverting input terminal of said first operational amplifier circuit within said semiconductor integrated circuit, said control input terminal being
25 provided for connection to circuits outside said semiconductor integrated circuit to act as a first control input terminal of said semiconductor integrated circuit;
- (d) a second gain control section connected to the

output terminal of the second operational amplifier circuit within said semiconductor integrated circuit and having an input terminal, a control input terminal and an output terminal, said input terminal being electrically
5 connected to said inverting input terminal of said second operational amplifier circuit within said semiconductor integrated circuit, said control input terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a second control

10 input terminal of said semiconductor integrated circuit;

(e) a third operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal being electrically connected to said output terminal of
15 said first gain control section within said semiconductor integrated circuit and being provided for connection to circuits outside said semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said semiconductor

20 integrated circuit and said output terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a first output terminal of said semiconductor integrated circuit;

(f) a fourth operational amplifier circuit having an
25 inverting terminal, a non-inverting terminal and an output terminal, said inverting input terminal being electrically connected to said output terminal of said "second" gain control section within said semiconductor integrated

circuit and leading to the outside of said semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said semiconductor integrated circuit and said output terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a second output terminal of said semiconductor integrated circuit; and

(g) a fifth operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as an optional input terminal for the semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said semiconductor integrated circuit, and said output terminal providing an external terminal to permit either the connection or disconnection of said fifth operational amplifier circuit to the inverting input terminal of the second operational amplifier circuit.

It will be appreciated that by the use of the above seven components constituting the voltage controlled variable gain circuit constructed as a semiconductor integrated circuit, and interconnected as outlined above, the problems and disadvantages of the known voltage controlled variable gain circuits with regard to waveform distortions are substantially overcome.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:-

- 5 Figure 3 shows a signal transmission circuit using a voltage controlled gain control circuit in accordance with a preferred embodiment of the present invention;

Figure 4 is a waveform diagram showing the

waveforms at various points in the circuit shown in Figure 3;

Figure 5 is a circuit diagram of a current voltage conversion circuit;

5 Figure 6 shows a signal transmission circuit using an integrated voltage controlled variable gain circuit and connected to an external circuit network in a first configuration of connection;

10 Figure 7 shows another signal transmission circuit using an integrated voltage controlled variable gain circuit of another embodiment, connected to an external circuit network connected in accordance with a second configuration of connection; and

15 Figures 8, 9 and 10 show alternative embodiments of the invention.

Referring first to Figure 3, a first gain controlling section VCA equivalent to the known voltage control circuit explained in connection with Figure 1 is arranged in a first signal line l_1 between an input terminal T_{IN} and output terminal T_{OUT} . A second signal line l_2 is connected between the input terminal T_{IN} and the output terminal T_{OUT} , in parallel with the first signal line l_1 . A second gain control section VCA' having an input/output transmitting characteristic

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substantially equal to that of the first gain control section VCA is connected in the second signal line l_2 . The first and second gain control sections VCA and VCA' are controlled by the control voltage V_c applied to a control terminal T_c . The gain V_{OUT}/V_{IN} is increased as a negative control voltage V_c is applied. On the contrary, the gain is lowered as a positive control voltage V_c is applied. The circuit arrangement and operation of the first and the second gain control sections VCA, VCA' are not described here, because they are materially identical to those of the known circuit shown in Figure 1.

A resistor R_{100} is connected between the input terminal T_{IN} and the inverting input terminal (-) of the operational amplifier circuit 21, in the first signal line l_1 . Therefore, the following relationship is established between the input voltage V_{IN} and the input current i_{in} flowing through the first gain control section VCA.

$$i_{in} = \frac{V_{IN}}{R_{100}} \dots\dots (3)$$

In order to obtain a low distortion factor, it is desirable to maintain the input current i_{in} at a low level. It is, therefore, desirable to select the value

of resistance of the resistor R_{100} to be about 300 Kohms.

An inverter circuit INV is connected between the input terminal T_{IN} and the inverting input terminal (-) of the operational amplifier circuit 21', in the

5 second signal line l_2 . The inverter circuit INV is constituted by an operational amplifier circuit 24, an input resistor R_{101} connected to the inverting input terminal (-) and a feedback resistor R_{102} connected between the output and the inverting input terminal (-).

10 In order to make the voltage gain between the input and output of the inverter circuit INV equal to one, the resistors R_{101} and R_{102} have an equal value of resistance of about 50 Kohms.

15 Therefore, the operational amplifier circuit 24 produces at its output a signal voltage of an inverted phase to the input voltage V_{IN} and of the same amplitude as the latter.

20 A resistor R'_{100} is connected between the output of the operational amplifier circuit 24 and the inverting input terminal (-) of the second gain control section VCA' and has a value of resistance value equal to that of the resistor R_{100} .

Therefore, the input current i'_{in} flowing through the second gain control section VCA' has an

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inverse phase to the input current i_{in} flowing through the first gain control section VCA and of the same amplitude as the latter.

5 Meanwhile, the output current i_{out} from the first gain control section VCA has a waveform of a high distortion factor, due to discordance of the parameter between the NPN transistor and the PNP transistor, as shown in Figure 4(a).

10 The voltage waveform V'_{T1} and V'_{T3} at the junction points T_1' and T_3' of the second gain control section VCA' have inverse phases to the waveforms V_{T1} and V_{T3} at the junction points T_1 and T_3 of the first gain control section VCA, and amplitudes equal to those of the latter.

15 Therefore, in the second gain control section VCA', the NPN transistor Q'_3 increases its conductivity in the period of negative half cycle of the waveform V'_{T3} to permit the collector current i'_3 to flow therethrough, while the PNP transistor Q'_4 increases
20 its conductivity in the period of positive half cycle of the voltage waveform V'_{T1} to permit the collector current i'_4 to flow therethrough.

The output current i'_{out} from the second gain control section VCA' has an inverse phase relation to the

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output current i_{out} from the first output control section VCA. The characteristic parameters of the NPN transistors Q'_1 and Q'_3 of the second gain control section VCA' are materially identical to the characteristic parameters of the NPN transistors Q_1 and Q_3 in the first gain control section VCA. Also, the characteristic parameters of the PNP transistors Q'_2 and Q'_4 of the second gain control section VCA' are materially identical to those of the PNP transistors Q_2 and Q_4 of the first gain control section VCA. Therefore, the collector current i'_3 in the NPN transistor is in inverse phase relation to the collector current i_3 of the NPN transistor and has an amplitude equal to the latter, while the collector current i'_4 in the PNP transistor Q'_4 is in inverse phase relation to the collector current i_4 in the PNP transistor Q_4 and has the same amplitude as the latter.

In consequence, the output current i'_{out} from the second gain control section VCA' has a waveform as shown in Figure 4(b).

This output current i'_{out} is applied to an inverting input terminal (-) of an operational amplifier circuit 25 in a current subtraction circuit CSC. A feedback resistor R_{103} is connected between the output and

the inverting input (-) of the operational amplifier circuit 25. The output voltage V_{25} of this operational amplifier circuit 25 is given by the following equation:-

$$V_{25} = R_{103} \cdot i'_{out} \quad \dots\dots\dots (4)$$

A resistor R_{104} is connected between the output of the operational amplifier circuit 25 and the inverting input terminal (-) of an operational amplifier circuit 26. The signal current i''_{out} flowing through the resistor R_{104} is determined by the following equation:-

$$i''_{out} = \frac{V_{25}}{R_{104}} = \frac{R_{103}}{R_{104}} \cdot i'_{out} \quad \dots\dots\dots (5)$$

Since the value of resistance of the resistor R_{104} is selected to be equal to the value of resistance of the resistor R_{103} , the value of the signal current i''_{out} is in inverse relation to the output current i'_{out} from the second gain control section VCA', as shown in Figure 4(c).

A signal current I_{OUT} which is the sum of the output current i_{out} from the first gain control section VCA and the signal current i''_{out} in the resistor R_{104} flows through the terminal T_5 of the inverting input (-)

of the operational amplifier circuit 26 of a current voltage conversion circuit CVC.

The current of the positive half cycle of this signal current I_{OUT} is the sum of the collector current i'_3 of the NPN transistor Q_3' and the collector current i_4 of the PNP transistor Q_4 , whilst the current of the negative cycle is the sum of the collector current i_3 of the NPN transistor Q_3 and the collector current i'_4 of the PNP transistor Q'_4 .

As has already been described, the amplitudes of the collector currents i_3 and i'_3 are substantially equal to each other, and the amplitudes of the collector currents i_4 and i'_4 are also substantially equal to each other. Therefore, the amplitudes of positive and negative half cycles of the signal current I_{OUT} are substantially equal to each other as shown in Figure 4(d), so that it is possible to obtain the signal current I_{OUT} having a small distortion factor.

An output voltage given by the following equation is obtained at the output terminal T_{OUT} of the circuit, because of the presence of a resistor R_{105} connected between the output terminal and the inverting input terminal (-) of the operational amplifier circuit

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$$V_{OUT} = R_{105} \cdot I_{OUT} \quad \dots\dots\dots(6)$$

A frequency characteristic which is flat over a wide frequency range can be obtained by connecting capacitors C_{103} and C_{105} each having a value of capacitance of about 30 pF (at least 2 pF) in parallel with the resistors R_{103} and R_{105} . A peaking will be generated at a high frequency range unless these capacitors are provided in the circuit. This peaking is attributable to the leakage of high frequency current flowing through the resistors R_{103} and R_{105} via a stray capacitance C_s (not greater than 1pF) between the collector electrodes of the input transistors Q_1 and Q_2 (Q_1' and Q_2') and the output transistors Q_3 and Q_4 (Q_3' and Q_4') of each gain control section. Since the compensation capacitors C_{103} and C_{105} provide bypass paths for the high-frequency currents, the peaking is eliminated to permit the frequency characteristic to become flat.

Instead of applying the control voltage V_c , it is possible to apply a voltage $-V_c$ of the reverse polarity to the base electrodes of the transistors Q_2 and Q_3 and Q_2' and Q_3' .

5 Figure 6 illustrates an embodiment of the present invention applied to a monolithic semiconductor integrated circuit. All of the elements shown within the broken line IC are formed on a silicon chip. In particular, the NPN transistors and the PNP transistors
10 are formed so as to have known vertical and lateral type constructions. In Figure 6, the same reference numerals are used to denote the same circuits or circuit elements to those shown in Figure 3. Reference numerals within circles show the terminal Nos. of the integrated
15 circuit.

In this embodiment, the circuit network outside the integrated circuit is connected in a first configuration of connection, in order to obtain a small distortion factor.

20 An operational amplifier circuit 21 is connected in the first signal line l_1 between the input and output terminals T_{IN} and T_{OUT} . The operational

amplifier circuit 21 is constituted by differential pair transistors Q_{10} and Q_{11} , a constant current transistor Q_{12} , current mirror transistors Q_{13} and Q_{14} , transistors Q_{15} and Q_{16} connected in Darlington configuration, a
5 constant current transistor Q_{17} and a level shift resistor R_1 . The base electrodes of the constant current transistors Q_{12} and Q_{17} are controlled by a bias voltage generated by a constant voltage and current regulator 27.

The regulator 27 is constituted by transistors
10 $Q_{18} - Q_{25}$ and resistors R_2, R_3 and operates to adjust various biasing voltages and biasing currents in the integrated circuit.

The base electrode of the transistor Q_{10} is connected to one end of the resistor R_{100} through a
15 terminal 1 as the inverting input terminal (-) of the operational amplifier circuit 21, as well as to the collector electrodes of the transistors Q_1 and Q_2 of the first gain control section VCA. The base electrode of the transistor Q_{11} is connected to earth through the
20 terminal 2 as the non-inverting input terminal (+) of the operational amplifier circuit 21. Since a constant current flows in the collector of the constant current transistor Q_{17} , two voltage signals V_{T1} and V_{T3} of the same phase but different levels are generated at respective

ends of the level shift resistor R_1 , and are transmitted to the junction points T_1 and T_3 of the first gain control section VCA.

As in the case of the known circuit, the first gain control section VCA has four bridge transistors Q_1 , Q_2 , Q_3 and Q_4 connected between the four junction points of the circuit.

Series connected diodes $Q_{29} - Q_{31}$, $Q_{32} - Q_{34}$, $Q_{35} - Q_{37}$ and $Q_{38} - Q_{40}$ are connected to the emitter electrodes of the four transistors $Q_1 - Q_4$. Since the A.C. resistance of these series connected diodes suppress the voltage gain for the noise voltages generated at the base electrodes of the four transistors $Q_1 - Q_4$, it is possible to obtain a high signal-to-noise ratio.

Each group of series connected diodes together with its associated transistor make up a chain of four transistors containing three NPN transistors and one PNP transistor, so that it is possible to obtain a good matching of voltage-current characteristics in the forward direction between the groups, irrespective of the dispersion of characteristic parameters of the NPN transistors and PNP transistors in the integrated circuit.

The distortion factor of the output is further

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reduced by this matching.

In general, when an equivalent diode constituted by N pieces of NPN transistors is connected in series to each of emitter electrodes of the PNP transistors, an equivalent diode constituted by (N-1) pieces of NPN transistors and one PNP transistor should be connected to the emitter electrode of each NPN transistor Q_1 and Q_3 .

The base electrodes of the transistors Q_1 and Q_4 are not directly connected to the junction point T_4 , and the base electrodes of the transistors Q_2 and Q_3 are not directly connected to the junction point T_2 . Level shift transistors $Q_{41} - Q_{48}$ are connected to the base electrodes of the transistors $Q_1 - Q_4$. Without these level shift transistors there is a danger that the gain control is not achieved completely.

If these level shift transistors are omitted and that the equivalent diodes constituted by N pieces of transistors are connected to the emitter of each bridge transistor $Q_1 - Q_4$, the control voltage V_c necessary for obtaining a -10dB change of gain between input and output sides is given by the following equation:-

$$V_c = \frac{KT}{q} \times (N + 1) \log_e 10 \frac{10}{20}$$

Suppose that the number N of transistors is four, the above-mentioned control voltage is about 150 mV/10dB, so that the control voltage has to be changed within the range of between 1.8 and 2.1. volts for obtaining a change of gain over +120 and -140 dB. On the other hand, the D.C. potentials of the collector electrodes of each of the bridge transistors $Q_1 - Q_4$ are substantially equal to earth potential, so that the transistor Q_1 is driven to the saturation region by such a large control voltage and, in some cases, a comparatively large current flows through the base junction of the transistor Q_1 .

Assume that such a level shift transistor is omitted, a positive control voltage V_c of about 1.8 volts, which is more than twice of the forward voltage of the collector-base junction, is applied to the base electrode of the transistor Q_1 , so that the base-collector junction of the transistor Q_1 and the collector-base junction of the transistor Q_2 are biased in the forward direction. Due to the forward biasing of the base-collector junction of each of the transistors Q_1 and Q_2 , a comparatively large D.C. current flows from the junction point T_4 to earth via the junction point T_2 , and the base-collector junctions of these transistors Q_1 and Q_2 .

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Similarly, if a negative control voltage of about -1.8 volts is applied, comparatively large D.C. currents flow through base-collector junctions of the transistors Q_3 and Q_4 . The terminal voltage at the junction point T_4 is clamped at a voltage level of 1.8 volts or -1.8 volts due to the flow of such comparatively large D.C. current, so that it becomes impossible to achieve a further gain control.

The level shift transistors $Q_{41} - Q_{48}$ conveniently enhance the clamp voltage which limits the controllable range of the gain, so that the difference between the maximum gain and minimum gain can be increased.

A comparatively large constant current of about $50\mu A$ flows, since constant current transistors $Q_{49}, Q_{50}, Q_{51}, Q_{52}$ are connected to the level shift transistors $Q_{41}, Q_{42}, Q_{43}, Q_{44}, Q_{45}, Q_{46}, Q_{47}$ and Q_{48} . The constant current flowing through these constant current transistors $Q_{49} - Q_{52}$ can be set by the bias current flowing in the transistors Q_{53} and Q_{54} . Thus, by permitting a comparatively large constant current through the level shift transistors $Q_{41} - Q_{48}$, noise produced by the four bridge transistors can be further suppressed. In this case, the control voltage V_c is

(40)

applied to the base electrodes of the transistors Q_{42} and Q_{48} through the terminal 3 of the integrated circuit and a resistance circuit network $R_4 - R_7$.

5 The inverter circuit INV arranged in the second signal line 1_2 is constituted by an operation amplifier circuit 24, an input resistor R_{101} and a feedback resistor R_{102} . The operation amplifier circuit 24 is constituted by differential pair transistors Q_{55} and Q_{56} , a constant current transistor Q_{57} , current mirror transistors Q_{58} and Q_{59} , transistors Q_{60} and Q_{61} connected in Darlington configuration, idling current adjusting diodes Q_{62} and Q_{63} , a constant current transistor Q_{64} and push-pull output transistors Q_{65} and Q_{66} .

15 The base electrode of the transistor Q_{56} is connected to earth through the terminal 2 of the integrated circuit as the non-inverting input terminal (+) of the operational amplifier circuit 24. The output from the operational amplifier circuit 24 is connected to the junction between the resistors R'_{100} and R_{102} through the terminal 5.

20 The other end of the resistor R'_{100} is connected through the terminal 6 of the integrated circuit to the base electrode of the transistor Q'_{10}

which constitutes the inverting input terminal (-) of the operational amplifier circuit 21' in the second gain control section VCA'. The operational amplifier circuit 21' is equivalent to the operational amplifier circuit 21 which has been described above, and the second gain control section VCA' is equivalent to the first gain control section VCA which has been described above, so further explanation is unnecessary.

The output signal i'_{out} from the second gain control section VCA' is applied to the base electrode of a transistor Q_{67} as the inverting input terminal (-) of the operational amplifier circuit 25 in the current subtraction circuit CSC. The terminals 7 and 8 of the integrated circuit constitute the inverting input terminal and the output terminal of the operational amplifier circuit 25, respectively. A detailed description of the operational amplifier circuit 25 is omitted because the latter has a construction similar to that of the operational amplifier circuit 24 in the inverter circuit INV.

As has been previously described, the terminal 9 of the integrated circuit, i.e. the terminal T_5 of the inverting input (-) of the operational amplifier circuit 26 in the current voltage conversion circuit CVC receives

the signal current I_{OUT} which is the sum of the output
 signal i_{out} from the first gain control section VCA and
 the signal current i''_{out} in the resistor R_{104} . The
 operational amplifier circuit 26 of the current voltage
 conversion circuit CVC produces at its output terminal
 10, an output voltage V_{OUT} expressed by the above
 equation (6) having a small distortion factor. The
 operational amplifier circuit 26 is not described in
 detail, because it has the same construction as the
 operational amplifier circuits 24 and 25 described above.

The terminals 11, 12 of the integrated circuit
 receive positive and negative voltages $+V_{cc}$ and $-V_{cc}$,
 respectively from a power source (not shown).

As will be clearly understood from the above
 description, the distortion attributable to the
 transmission characteristic between the input signal
 and output signal of the first gain control section VCA
 can be cancelled in the signal subtraction circuit CSC,
 by the distortion produced by the second gain control
 section VCA' having a transmission characteristic
 materially identical to that between the input and output
 of the inverter circuit INV and first gain control section
 VCA, so that a signal transmission characteristic of
 small distortion can be obtained.

On the other hand, it is also possible to improve the noise characteristic for the following reason.

The following equation for the maximum voltage gain $G'V$ is derived from equations (3) and (6). This maximum gain is twice as large as the maximum gain GV ($= R_{105}/R_{100}$).

$$\begin{aligned} G'V &= \frac{|V_{OUT}|}{|V_{IN}|} = \frac{|I_{OUT} \times R_{105}|}{|i_{in} \times R_{100}|} \\ &= \frac{|(i_{in} + i_{in}'') \times R_{105}|}{|i_{in} \times R_{100}|} \\ &= \frac{|2i_{in} \times R_{105}|}{|i_{in} \times R_{100}|} = 2 \times \frac{R_{105}}{R_{100}} \dots\dots (7) \end{aligned}$$

In contrast, the total noise voltage V_{NT} is given by the following equation in which the noise voltages produced by the first and second gain control sections VCA and VCA' are represented by V_{N1} and V_{N2} , respectively. Thus, the total noise voltage V_{NT} is only $\sqrt{2}$ times as large as the noise voltage of a single gain control section.

$$V_{NT} = \sqrt{V_{N1}^2 + V_{N2}^2} \div \sqrt{2} \cdot V_N \dots\dots\dots (8)$$

$$(\because V_N \div V_{N1} \div V_{N2})$$

Thus, the signal-to-noise ratio can be reduced to $1/\sqrt{2}$ of the compared one in order to improve the noise characteristic.

As has been described above, it is possible to obtain a signal transmission circuit of low distortion factor and low noise level, by using the integrated voltage controlled variable gain circuit and connecting an external circuit network in a first connection configuration.

It is also possible to obtain a signal transmission circuit capable of effecting independent gain controls of two input signals by using the integrated voltage controlled variable gain circuit and connecting the external circuit network in a second connection configuration.

A voltage control variable gain circuit shown in Figure 6 in the form of a monolithic semiconductor integrated circuit can be used as a variable gain circuit for stereophonic instruments.

As shown in Figure 7, two channel signals

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V_{IN}, V'_{IN} representing the left and right signals of the stereophonic instrument are applied to two input terminals T_{IN}, T'_{IN} . The channel signal V_{IN} applied to the input terminal T_{IN} is transmitted to the output terminal T_{OUT} through the terminal 1 of the integrated circuit, the operational amplifier circuit 21, the first gain control section VCA, the operational amplifier circuit 26 and the terminal 10 of the integrated circuit, as one V_{OUT} of the left and right output signals of the stereophonic instrument. The other channel signal V'_{IN} applied to the input terminal T'_{IN} is transmitted to the output terminal T'_{OUT} , through the terminal 6 of the integrated circuit, the operational amplifier circuit 21', the second gain control section VCA', the operational amplifier circuit 25 and the terminal 8 of the integrated circuit, as the other V'_{OUT} of the right and left output signals of the stereophonic instrument.

The gains of the first and second gain control sections VCA and VCA' are independently controlled by means of the control voltages V_C and V'_C applied to the respective terminals 3 and 3' of the integrated circuit.

The monolithic semiconductor integrated circuit shown in Figure 6 can provide a variable gain

circuit having a low distortion factor and high signal-to-noise ratio, by connecting the external peripheral circuit in the manner shown in Figure 6. On the other hand, by connecting the external peripheral circuit in the form as shown in Figure 7, it is possible to obtain a two-channel variable gain circuit having a reduced cost of manufacture.

Accordingly, the monolithic semiconductor circuit shown in Figure 6 has a high practicality because it can be used in two different ways by changing the connection configuration of the external peripheral circuit.

The change of the external peripheral circuit can be made in a comparatively simple way. The integrated voltage control variable gain circuit has a high utility also from this point of view.

The first and second gain control sections need not be always composed of four bridge transistors. For instance, it is possible to use a gain control section of differential current switching type gain control section, as shown in Figures 8 and 9.

Figures 8 and 9 show modifications of the basic circuit in which each have a differential input amplifier circuit DIFF. The differential input amplifier

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circuit DIFF comprises a constant current source CS_1 or CS_2 , differential transistors Q_{100} , Q_{101} or Q_{109} , Q_{110} , and load means Q_{102} , Q_{103} or R_{12} , R_{13} and delivers to the first signal line l_1 a signal voltage of the same phase as the input voltage V_{IN} applied to the input terminal T_{IN} . At the same time, a signal voltage of the opposite phase is delivered to the second signal line l_2 by this differential input amplifier circuit DIFF. The amplitudes of the two signal voltages of opposite phases on the first and second signal lines l_1 and l_2 have to be equal to each other.

In the modification of Figure 8, signal current flows in the collector electrodes of the transistors Q_{104} and Q'_{104} , as these two signal voltages are applied to the base electrode of the transistor Q_{104} of the first gain control section VCA and the base electrode of the transistor Q'_{104} of the second gain control section VCA'. The ratio of distribution of signal current to the differential transistors is changed by means of the control voltage V_c applied between the control terminals T_{C1} and T_{C2} to control the magnitudes of the signal voltages generated across the resistors R_{10} and R'_{10} .

In the modification shown in Figure 9, two

signal voltages of different phases on the first and second signal lines l_1 and l_2 are applied to the base electrodes of respective transistors Q_{111} and Q'_{111} of the first and second gain control sections VCA and VCA', so that signal currents flow in the collector electrodes of the transistors Q_{111} and Q'_{111} . The ratio of distribution of signal current to differential transistors is controlled by the control voltage V_c applied between control terminals T_{C1} and T_{C2} so that the magnitudes of the voltages generated across the resistors R_{17} and R'_{17} are controlled.

In the differential current switching type gain control section in which the ratio of current distribution to the differential transistors is controllable, the distortion of output signal is extremely small when the control voltage V_c applied between the control terminals T_{C1} and T_{C2} is substantially zero, because the characteristics of the differential pair transistors coincide with each other. However, as the control voltage V_c is increased to cause a large change of distribution ratio to the differential transistors, the output signal contains distortion components of even higher harmonics, due to the influence of the base spreading resistance and the emitter series resistance.

The modifications shown in Figures 8 and 9 incorporate a voltage subtraction circuit VSC containing differential pair transistors Q_{107} , Q_{108} or Q_{118} , Q_{119} . The voltage subtraction circuit VSC cancels the distortions generated in the first and second gain control sections VCA and VCA' with each other. It is, therefore, possible to obtain an output signal V_{OUT} of a small distortion factor at the output terminal T_{OUT} .

According to another modification shown in Figure 10, the gains in the first and second gain control sections VCA, VCA' can be controlled discontinuously by the control voltage V_c . The first and the second gain control sections VCA and VCA' are constituted by analog switches including N channel MOSFETs T_3 and T'_3 and P channel MOSFETs T_4 and T'_4 . In each CMOS analog switch, the sources (S) and drains (D) of the N channel and P channel MOSFETs are commonly connected such that the source-drain path of the N channel MOSFET and the source-drain path of the P channel MOSFET extend in parallel with each other along the first signal line l_1 or the second signal line l_2 . The gates of the N channel MOSFETs T_3 and T'_3 and the gates of the P channel MOSFETs T_4 and T'_4 are connected to each other through an inverter IN2, and the gates of the P channel MOSFETs T_4 and T'_4 are

connected also to the control terminal T_c through an inverter IN_1 .

The differential input amplifier circuit DIFF is constituted by a source resistor R_{20} , N channel differential MOSFETs T_1 and T_2 and load resistors R_{21} and R_{22} , and is arranged to deliver to the first signal line l_1 a signal voltage of the same phase as the input voltage V_{IN} applied to the input terminal T_{IN} . The circuit DIFF also delivers a signal voltage of an opposite phase as the input voltage V_{IN} to the second signal line l_2 .

By selecting the values of resistance of the load resistors R_{21} and R_{22} to be equal to each other, it is possible to set the amplitudes of signal voltages of opposite phases on the first and second signal lines l_1 and l_2 substantially equal to each other.

When a control voltage V_c of high level is applied to the control terminal T_c , the P channel MOSFETs T_4 and T'_4 are turned on by the output from the inverter IN_1 of low level, while the output from the inverter IN_2 of high level turns the N channel MOSFETs T_3 and T'_3 on. In consequence, the first and second gain control sections VCA and VCA' permit the signal transmission between the input and output sides to produce

at the output terminal T_{OUT} an output signal V_{OUT} in response to the input signal V_{IN} . When the control voltage V_c of low level is applied to the control terminal T_c , N channel MOSFETs T_3 and T'_3 are turned off, as well as P channel MOSFETs T_4 and T'_4 , so as to prohibit the delivery of the output signal V_{OUT} to the output terminal T_{OUT} .

However, when the N and P channel MOSFETs of the CMOS analog switch are turned on to permit the signal transmission from the input terminal T_{IN} to the output terminal T_{OUT} , a distorted waveform having even higher harmonics, particularly a large second harmonic, is produced.

The voltage subtraction circuit VSC, including the source resistor R_{23} and N channel differential MOSFETs T_5 and T'_6 , act to permit the distorting components of the output voltages of the first and second gain control sections VCA and VCA' , which are generated across the resistors R_{24} and R'_{24} , to cancel each other.



CLAIMS.

1. A voltage controlled variable gain circuit constructed as a semiconductor integrated circuit including:

(a) a first operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal leading out of said semiconductor integrated circuit to act as a first input terminal of said semiconductor integrated circuit, said non-inverting input terminal being connected to a reference potential outside said semiconductor integrated circuit;

(b) a second operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal leading out of said semiconductor integrated circuit to act as a second input terminal of said semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said semiconductor integrated circuit;

(c) a first gain control section connected to the output terminal of the second operational amplifier circuit within said semiconductor integrated circuit and having an input terminal, a control input terminal and an output terminal, said input terminal being electrically connected to said inverting input terminal of said first operational amplifier circuit within said semiconductor integrated circuit, said control input terminal being provided for connection to circuits



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outside said semiconductor integrated circuit to act as a first control input terminal of said semiconductor integrated circuit;

(d) a second gain control section connected to the
5 output terminal of the second operational amplifier circuit within said semiconductor integrated circuit and having an input terminal, a control input terminal and an output terminal, said input terminal being electrically connected to said inverting input terminal
10 of said second operational amplifier circuit within said semiconductor integrated circuit, said control input terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a second control input terminal of said semiconductor
15 integrated circuit;

(e) a third operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal being electrically connected to said output terminal
20 of said first gain control section within said semiconductor integrated circuit and being provided for connection to circuits outside said semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside
25 said semiconductor integrated circuit and said output terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a first output terminal of said semiconductor integrated



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circuit;

(f) a fourth operational amplifier circuit having an inverting terminal, a non-inverting terminal and an output terminal, said inverting input terminal being electrically
5 connected to said output terminal of said "second" gain control section within said semiconductor integrated circuit and leading to the outside of said semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said
10 semiconductor integrated circuit and said output terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as a second output terminal of said semiconductor integrated circuit; and

15 (g) a fifth operational amplifier circuit having an inverting input terminal, a non-inverting input terminal and an output terminal, said inverting input terminal being provided for connection to circuits outside said semiconductor integrated circuit to act as an optional
20 input terminal for the semiconductor integrated circuit, said non-inverting input terminal being connected to said reference potential outside said semiconductor integrated circuit, and said output terminal providing an external terminal to permit either the connection
25 or disconnection of said fifth operational amplifier circuit to the inverting input terminal of the second operational amplifier circuit.



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2. A signal transmission circuit incorporating the voltage controlled variable gain circuit according to Claim 1, comprising:

- 5 (h) a signal input terminal located outside said semiconductor integrated circuit and arranged to receive an input signal;
- (i) a first input resistor located outside said semiconductor integrated circuit and connected between
10 said signal input terminal and said inverting input terminal of said first operational amplifier circuit;
- (j) a second input resistor located outside said semiconductor integrated circuit and connected between said signal input terminal and said inverting input
terminal of said fifth operational amplifier circuit;
- 15 (k) a first feedback resistor located outside said semiconductor integrated circuit and connected between said output terminal of said fifth operational amplifier circuit and said inverting input terminal of the same;
- (l) a third input resistor located outside said
20 semiconductor integrated circuit and connected between said output terminal of said fifth operational amplifier circuit and said inverting input terminal of said second operational amplifier circuit;
- (m) a second feedback resistor located outside said
25 semiconductor integrated circuit and connected between



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said output terminal of said third operational amplifier circuit and said inverting input terminal of the same;

(n) a third feedback resistor located outside said semiconductor integrated circuit and connected between
5 said output terminal of said fourth operational amplifier circuit and said inverting input terminal of the same; and
(o) a fourth input resistor located outside said semiconductor integrated circuit and connected between
said output terminal of said fourth operational amplifier
10 circuit and said inverting input terminal of said third operational amplifier circuit.

3. A signal transmission circuit according to Claim 2, wherein said second input resistor and said first feedback resistor have values of resistance
15 substantially equal to each other, said first input resistor and said third input resistor have values of resistances substantially equal to each other and said third feedback resistor and said fourth input resistor have values of resistance which are substantially equal
20 to each other.

4. A signal transmission circuit according to Claim 3, further comprising:

(p) a first compensation capacitor connected in parallel with said second feedback resistor outside said
25 semiconductor integrated circuit; and



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(q) a second compensation capacitor connected in parallel with said third feedback resistor outside said semiconductor integrated circuit.

5. A signal transmission circuit incorporating the
5 voltage controlled variable gain circuit according to Claim 1, comprising:

(h) a first signal input terminal located outside said semiconductor integrated circuit for receiving a first input signal;

10 (i) a second signal input terminal located outside said semiconductor integrated circuit for receiving a second input signal;

(j) a first input resistor located outside said semiconductor integrated circuit and connected between
15 said first signal input terminal and said inverting input terminal of said first operational amplifier circuit;

(k) a second input resistor located outside said semiconductor integrated circuit and connected between said second signal input terminal and said inverting
20 input terminal of said second operational amplifier circuit;

(l) a first feedback resistor located outside said semiconductor integrated circuit and connected between said output terminal of said third operational amplifier
25 circuit and said inverting input terminal of the same; and



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(m) a second feedback resistor located outside said semiconductor integrated circuit and connected between said output terminal of said fourth operational amplifier circuit and said inverting terminal of the same.

5 6. A signal transmission circuit according to Claim 5, further comprising:

(n) a first compensation capacitor connected in parallel with said first feedback resistor and located outside said semiconductor integrated circuit, and

10 (o) a second compensation capacitor connected in parallel with said second feedback resistance and located outside said semiconductor integrated circuit.

7. A signal transmission circuit according to Claim 6, wherein said first and second input signals are
15 left and right channel signals for a stereophonic instrument, whereby the left and right channel output signals are derived from said first and second output terminals of said semiconductor integrated circuit.

8. A voltage controlled variable gain circuit
20 according to Claim 1, wherein each of said first and second gain control sections includes at least a first junction point, a second junction point, a third junction point, a fourth junction point, a first transistor a second transistor, a third transistor and
25 a fourth transistor, the emitter electrodes of said



second and fourth transistors being connected to said first junction point, the base electrodes of said second and third transistors being connected to said second junction point, the emitter electrodes of said third and first transistors being connected to said third junction point, the base electrodes of said first and fourth transistors being connected to said fourth junction point, the collector electrodes of said first and second transistors being connected to each other within said semiconductor integrated circuit and further electrically connected within said semiconductor integrated circuit, as said input terminal of said first gain control section or said second gain control section, to said inverting input terminal of said first operational amplifier circuit or said second operational amplifier circuit, the collector electrodes of said third and fourth transistors being connected to each other within said semiconductor integrated circuit and further electrically connected within said semiconductor integrated circuit, as said output terminal of said first gain control section or second gain control section, to said inverting input terminal of said third operational amplifier circuit or said fourth operational amplifier circuit, said output terminal of said first



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operational amplifier circuit or said second operational amplifier circuit being connected to said first and third junction points electrically within said semiconductor integrated circuit, said second junction point leading to the outside of said semiconductor integrated circuit, said fourth junction point leading to the outside of said semiconductor integrated circuit to act as said control input terminal of said first gain control section or said second gain control section.

9. A voltage controlled variable gain circuit according to Claim 8, wherein each of said first and second gain control section further includes:

(h) a first level shift element connected between the emitter electrode of said first transistor and said

third junction point;

(i) a second level shift element connected between the emitter electrode of said second transistor and said first junction point;

(j) a third level shift element connected between the emitter electrode of said third transistor and said third junction point;

(k) a fourth level shift element connected between the emitter electrode of said fourth transistor and said first junction point;



- (1) a fifth level shift element connected between the base electrode of said first transistor and said fourth junction point;
- (m) a sixth level shift element connected between the base electrode of said second transistor and said second junction point;
- (n) a seventh level shift element connected between the base electrode of said third transistor and said second junction point; and
- (o) an eighth level shift element connected between the base electrode of said fourth transistor and said fourth junction point.

10. A voltage controlled variable gain circuit according to Claim 8, wherein said first and third transistors are NPN transistors, whilst said second and fourth transistors are PNP transistors.

11. A signal transmission circuit incorporating a voltage controlled variable gain circuit constructed substantially as herein described with reference to and illustrated in Figure 3, or Figure 6, or Figure 7, or Figure 8, or Figure 9 or Figure 10 of the accompanying drawings.

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