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ELECTRO-OPTIC INTEGRATED CIRCUIT

High speed logic circuits are being manufactured in larger and more complicated semiconductor chips.

5 Presently, these semiconductor chips are constructed entirely of electronic devices. If these chips continue to be completely electronic, the speed with which they can manipulate external signals will be limited by the time required to send electrical signals from one part

10 of the chip to another. The RC time constant of the driving device and the relatively long connecting conductor on the chip will be the primary factors in determining the speed of the chip. A large scale high speed integrated circuit can be made to operate much

15 faster if the signals on the chip were transmitted by way of an optical signal. In essence the conductor can be replaced by an optical waveguide with an optical source or emitter at one end of the waveguide and a detector at the other end.

20 According to the present invention there is provided an electro-optic integrated circuit wherein light is generated, guided and detected including a substrate having a plurality of epitaxial layers grown thereon, the epitaxial layers including a first primary

25 layer having a bandgap suitable for optical detection, a second primary layer having a wider bandgap suitable for the generation of light that can be detected by the

28 first primary layer, a third primary layer having a

bandgap that is larger than the bandgap of the second primary layer for the transmission of the light, and at least one layer between each pair of adjacent primary layers with a bandgap greater than the bandgap of each of the adjacent primary layers.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawings of which:-

FIG. 1 is a pictorial top view of a multilayered optical integrated circuit according to the present invention,

FIG. 2 is a sectional view of a multilayered optical integrated circuit according to the present invention,

FIG. 3 is a top view of part of the integrated circuit shown in FIG. 2,

FIG. 4 is a schematic diagram of the integrated circuit shown in FIGS. 2 and 3,

FIG. 5 is a table of semiconductor layers shown in FIG. 2 giving the composition of each of these layers, and

FIG. 6 is a cross-sectional diagram of the waveguide portion of the integrated circuit shown in FIGS. 2 and 3.

A semiconductor chip 10 on which a large scale integrated electronic circuit 11 has been fabricated is shown in FIG. 1. As indicated in FIG. 1, a field effect transistor 15 can be used to electrically couple a signal on the chip to a light emitting device 16 which in turn converts this electrical signal into an optical signal. The optical signal is coupled by way of an optical waveguide 17 to a photodetector 18 which, in turn, provides an electrical signal to the gate of a field effect transistor 19. In this way, an electrical signal from the lower left-hand portion of the semiconductor chip 10 may be rapidly coupled to the lower right-hand portion of the semiconductor chip. The technical area comprising the combination of optical and electronic

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circuitry on a single semiconductor device has already been labeled "photonics" by those skilled in the art. Similar electro-optical couplings of one part of the chip to another can be provided by other sources,

5 waveguides and detectors in other areas of the semiconductor chip 10.

A schematic diagram of the type of circuit that is provided by elements 15-19 in FIG. 1 is illustrated in FIG. 4. As indicated in FIG. 4 an electrical signal
10 is connected to the gate of the field effect transistor whose source is biased and drain is connected by way of a conductor to a light emitting diode 16. The light generated by diode 16 is transmitted by way of waveguide 17 to a photodetector 18 which couples an electrical
15 signal to the gate of a second field effect transistor 19. The train of FET 19 is biased and its source provides the output signal that may be used in the second area of the semiconductor chip.

The functions illustrated in FIG. 4 are provided
20 by way of a multilayered optical integrated circuit illustrated in FIG. 2. The fabrication of the device shown in FIG. 2 is accomplished in accordance with the table set forth in FIG. 5 using procedures to be described hereinafter. Briefly, the primary layer 207
25 is fabricated with a bandgap that is suitable for the generation of optical energy. Due to the tapered shape of the primary layer 210 and cladding layer 211 above it in the device shown in FIG. 2, some of the optical energy from layer 207 is coupled into layer 210 which in
30 turn serves as a waveguide between two sections of the multilayered optical integrated circuit. At the remote end of primary layer 210, a similar taper in layer 210 and cladding layer 211 is used to reflect the guided optical energy down through the layers of the
35 device in FIG. 2 to a primary layer 205 which is fabricated to have a bandgap that is lower than either of the other two bandgaps and, therefore, can serve as a
38 detector of the optical energy. As indicated in FIG. 5,

the primary layers that provide emission, detection and guidance are surrounded by secondary layers having higher bandgap energies and therefore lower refractive indices.

5 Fabrication of the device begins by growing the epitaxial layers 202-211 shown in FIG. 2 and specified in FIG. 5 on an indium phosphide substrate 201. The doping thickness and composition of each of the layers are set forth in FIG. 5. This growth may be performed by using liquid phase epitaxy using standard semiconductor growth techniques. As indicated in FIG. 5, the wafer which results
10 consists of alternating p-type and n-type layers and groups of layers with varying thickness and varying chemical compositions to achieve the different bandgap energies. The two layers 202,203 adjacent to the substrate 201 have doping characteristics suitable for the fabrication of electrical devices 15,19.

15 In one embodiment disclosed the regions of the device which are to be used for optical emission and detection are then isolated by diffusing zinc through a mask to create regions of n-type layers that are completely surrounded by p-type material. These regions are illustrated in FIG. 2 as regions 220 and 221. The structure of
20 these regions is further illustrated in FIG. 3 which is a top view of the device shown in FIG. 2. As indicated in FIG. 3, the zinc doped regions are essentially annular and are diffused to the depth of buffer layer 203 as indicated in FIG. 2.

To understand the necessity for the next steps in the
25 processing of the semiconductor chip, it is helpful to understand first the method employed for guiding the light waves from one area of the chip to another. This method involves a ridge-loaded waveguide structure of the type shown in FIG. 6. As indicated in FIG. 6, layer 210 is of limited width relative to layer 209 and the
30 light is guided in layer 210 only in the region that is loaded by the top cladding layer 211. To confine the guided light to a singly mode, the thickness, t , of layer 210 is chosen in the present embodiment to be equal to 0.5 micrometres. In the present embodiment where layers 209 and 211 are fabricated of indium

phosphide, the index of refraction of these layers is approximately equal to 1.35. Using equations from the slab mode theory of waveguided propagation, the index of refraction for layer 210 can be computed and this index determines the composition of layer 210 set forth in FIG. 5. Using the equations from the paper by H.W. Kogelnik in the book entitled Integrated Optics by T. Tamir, Springer-Verlag, 1975, pages 23-24, the minimum value of thickness which will support single mode propagation in this type of waveguide can be computed. In the present instance where the layers have the composition set forth in FIG. 5, this minimum value of thickness is approximately equal to 0.3 micrometres. The value for the width, w , of the ridge-loading cladding layer 211 which will limit propagation to a single mode, can best be determined by experimentation, but theory predicts that this width will fall in the range of 2-5 micrometres.

With the parameters set forth for layers 209, 210 and 211, the light can be deflected out of the waveguide to a lower level on the semiconductor chip by etching a taper as shown in FIG. 2 down through the layers 210 and 211. If the taper is cut entirely through layer 210, the light will be reflected by total internal reflection. It should be noted, however, that the taper need only cut down through layer 211 and at least into layer 210 to a thickness that is approximately equal to one half of the thickness necessary to support single mode propagation. Layer 210 need only be wide enough to give a region on each side of layer 211 equal to about the width of layer 211.

After growth of the semiconductor layers shown in FIG. 2 and implantation of the zinc doped regions 220 and 221, processing of the semiconductor chip can then continue by forming layers 210 and 211 into the ridge-type structures shown in FIG. 6. These ridge-waveguide stripes for layers 210 and 211 are then fabricated by using photolithography to mask the stripe areas, and then

using a combination of reactive-ion plasma etching or chemical etching to etch through layers 210 and 211. Another photolithography step is then used to mask all of the wafer except areas near the tips of the light guide stripes. A chemical etch is then used which produces a tapered end on layers 210 and 211 and therefore provides optical coupling between the tips of the light guide and the source and detector layers beneath.

- 10 Because of the bandgap differences of the various layers it is possible to use selective etchants that etch quickly through one type of layer and slow down appreciably when the next layer is reached. There are several references that can guide the fabricator of the device
- 15 in the performance of these steps. See, for example, J. Electrochem. Soc.: Solid-State Science and Technology, Vol. 126, No. 2, February 1979, "Material-Selective Chemical Etching in the System InGaAsP/InP," by S.B. Phatak et al, pp. 287-292; Japanese Journal
- 20 of Applied Physics, Vol. 19, No. 1, January 1980, "Chemical Etching of InP and GaInAsP For Fabricating Laser Diodes and Integrated Optical Circuits," by T. Kambayash et al, pp. 79-85; J. Electrochem. Soc.: Solid State Science, Vol. 118, No. 5, May 1971,
- 25 "Selective Etching of Gallium Arsenide Crystals in $H_2SO_4-H_2O_2-H_2O$ System," by S. Lida, pp. 768-771.

A photolithographic mask is then used to cover all areas except those where the next layer, 209 in FIG. 2, is to be removed. Layers 209, 210 and 211 are then removed where they are exposed. A new photolithographic mask is then used to cover all areas except where the next layer, 208 in FIG. 2, is to be removed, and layer 208 is then etched away where exposed.

- 35 This process is repeated for the remaining layers, 207 to 202 in FIG. 2.

An insulating dielectric film 231 such as 3000Å of SiO is then deposited over the wafer and is

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covered by a photolithographic mask except where holes are desired for making electrical contact to the semiconductor layers at points exposed by the previous etching steps. These holes are etched in the dielectric, and metal conducting films 212 and 213 (a composite of 1000Å of chromium and 4000Å of gold) are evaporated over the wafer. A photolithographic mask is then used to cover the metal stripes used for electrical interconnection and the metal outside these stripes is etched away.

The wafer is then heat-treated (alloyed) to improve the ohmic contact between metal and semiconductor. The individual chips are finally separated and mounted in packages.

What has been described hereinabove is merely an illustrative embodiment of the present invention. Numerous departures may be made by those skilled in the art without departing from the scope of the present invention. For example, the top cladding layer 211 may be entirely absent especially in those cases where the primary guiding layer 210 is expected to guide more than a single mode. In those cases, primary layer 210 may be exposed to the air or covered by the oxide film 231.

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CLAIMS

1. An electro-optic integrated circuit wherein light is generated, guided and detected including a substrate having a plurality of epitaxial
5 layers grown thereon, the epitaxial layers including a first primary layer having a bandgap suitable for optical detection, a second primary layer having a wider bandgap suitable for the generation of light that can be detected by the first primary layer, a
10 third primary layer having a bandgap that is larger than the bandgap of the second primary layer for the transmission of the light, and at least one layer between each pair of adjacent primary layers with a bandgap greater than the bandgap of each of the
15 adjacent primary layers.
2. An electro-optic integrated circuit as claimed in claim 1 wherein the first primary layer is the closest primary layer to the substrate, and the third primary layer is the primary layer that is
20 furthest removed from the substrate.
3. An electro-optic integrated circuit as claimed in claim 2 wherein the epitaxial layers include a narrow stripe layer formed as a ridge over the third primary layer.
- 25 4. An electro-optic integrated circuit as claimed in claim 3 wherein the stripe layer has at least one termination in the form of a taper which extends into the third primary layer so as to optically couple the third primary layer with the first or second
30 primary layer.
5. An electro-optic integrated circuit as claimed in any of the preceding claims wherein the substrate is composed primarily of indium and phosphorus, and the epitaxial layers are composed primarily of
35 indium, phosphorus, gallium and arsenic.
6. An electro-optic integrated circuit as claimed in any of the preceding claims wherein the
38 epitaxial layers include at least two epitaxial layers



adjacent to the substrate having doping characteristics that are suitable for the fabrication of electrical devices.

7. An electro-optic integrated circuit substantially as herein described with reference to the accompanying drawings.

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