

## Description

Title of Invention: DIRECT AC POWER CONVERTER

### Technical Field

5 [0001] The present invention relates to a direct AC power converter, and particularly, to a configuration including a rectifying circuit, an inverter, and a boost chopper.

### Background Art

[0002] Patent Documents 1 and 2 and Non-Patent Document 1 introduce direct AC power converters. In each of these direct AC power converters, a boost chopper is used  
10 and receives an electric power from a rectifying circuit and supplies the electric power to an inverter so that pulsation of an instantaneous power is reduced.

### Prior Art Documents

#### Patent Documents

[0003] Patent Document 1: Japanese Patent Application Laid-Open No. 2011-193678  
15 Patent Document 2: Japanese Patent Application Laid-Open No. 2012-135184  
Patent Document 3: Japanese Patent Application Laid-Open No. 2014-82926

#### Non-Patent Document

[0004] Non-Patent Document 1: Ohnuma, Itoh, "Experimental Verification of Single Phase to Three Phase Converter Using an Active Buffer circuit with a Charge Circuit",  
20 IEEJ 2010 Industry Applications Society Conference 1-124, pp. I-587-590 (2010)

### Summary of Invention

#### Problems to be Solved by the Invention

[0005] In the techniques introduced in Patent Documents 1 and 2 and Non-Patent Document 1, however, a period of charge from the rectifying circuit to the capacitor and a  
25 period of discharge from the capacitor to the inverter are set alternately in each 1/4 of a

cycle of an input AC voltage. The magnitude of an output voltage thus remains at  $1/\sqrt{2}$  times a crest value of the input AC voltage.

[0006] Also in the technique described in Patent Document 3, a capacitor is unnecessarily charged and discharged in view of the operation of an inverter, so that a  
5 boost chopper is likely to require an increased power capacity.

[0007] The present invention therefore has an object to provide a technique of reducing a power capacity required for a boost chopper while increasing a voltage output from a direct AC power converter more than in a conventional technique.

#### Means to Solve the Problems

10 [0008] A direct AC power converter according to the present invention includes a DC link (7), a first rectifying circuit (5, 51), a boost chopper (3), and a switch (41).

[0009] The DC link has a first power supply line (L1) and a second power supply line (L2) to which a potential lower than a potential of the first power supply line is applied.

[0010] The first rectifying circuit has a plurality of input terminals that receive an input  
15 of an AC voltage, and a pair of output terminals (51c, 51d) each connected to the DC link.

[0011] The inverter converts a voltage applied to the DC link into another multi-phase AC voltage.

[0012] The boost chopper has a capacitor (34) at its output stage.

[0013] The switch switches a discharge and non-discharge from the capacitor to the  
20 DC link.

[0014] In a first aspect of the direct AC power converter according to the present invention, in the boost chopper, the capacitor is charged at least during a first period being a part of a period during which a discharge duty (dc) is greater than 0.

[0015] The discharge duty is a time ratio at which the switch is conductive.

25 [0016] A virtual DC link voltage (Vdc) is greater than or equal to a first value (V1) and

smaller than or equal to a second value (V2). The virtual DC link voltage is expressed as a sum of a product ( $d_c \cdot V_c$ ) of the discharge duty and a voltage between both ends ( $V_c$ ) of the capacitor and a product ( $d_r \cdot V_{rec}$ ) of a rectifying duty ( $d_r$ ) and a rectified voltage ( $V_{rec}$ ) of the AC voltage.

5 [0017] The rectifying duty takes a value obtained by subtracting a sum of the discharge duty and a zero voltage duty ( $d_z$ ) from 1.

[0018] The zero voltage duty is a time ratio at which the inverter (6) adopts a zero voltage vector irrespective of magnitude of a voltage output from the inverter (6).

[0019] The first value is a maximum value ( $\max(|V_{uv}|, |V_{vw}|, |V_{wu}|)$ ) among absolute  
10 values of respective line-to-line voltages of the multi-phase AC voltage.

[0020] The second value is a maximum value that the absolute values can take.

[0020a] The rectified voltage is applied to an input side of the boost chopper.

[0020b] A second aspect of the direct AC power converter according to the present invention, further includes a second rectifying circuit (52) that inputs the rectified voltage  
15 ( $V_{rec}$ ) to the boost chopper (3).

[0020c] In a third aspect of the direct AC power converter according to the present invention, said pair of output terminals of said first rectifying circuit are connected to an input side of said boost chopper.

[0021] In a fourth aspect of the direct AC power converter according to the present  
20 invention, in any one of the first to third aspects, the capacitor is charged in the boost chopper during the first period and a part or whole of a period at which the discharge duty is 0.

[0022] In a fifth aspect of the direct AC power converter according to the present invention, in the first to fourth aspects, the capacitor (34) is charged with a charge power ( $P_{ci}$ ) and discharged with a discharge power ( $P_{co}$ ) during the first period. The first  
5 period has a period during which the charge power is greater than the discharge power and a period during which the discharge power is greater than the charge power.

[0023] In a sixth aspect of the direct AC power converter according to the present invention, in any one of the first to fifth aspects, a period during which the virtual DC link voltage ( $V_{dc}$ ) takes the first value ( $V_1$ ) is present.

10 [0024] In a seventh aspect of the direct AC power converter according to the present invention, in any one of the first to sixth aspects, the discharge duty at which the zero voltage duty ( $d_z$ ) is minimum is set based on a command value ( $i_{rec}^*$ ) of a rectified

current ( $i_{rec}$ ) being a sum of a current ( $i_b$ ) flowing in the boost chopper (3) and a current ( $i_{direct}$ ) flowing from the first rectifying circuit to the inverter (6), a command value ( $V_{dc}^*$ ) of the virtual DC link voltage ( $V_{dc}$ ), a voltage between both ends ( $V_c$ ) of the capacitor, the rectified voltage ( $V_{rec}$ ), and a current ( $i_{dc}$ ) input to the inverter (6).

5 [0025] In a eighth aspect of the direct AC power converter according to the present invention, in the seventh aspect, when the virtual DC link voltage ( $V_{dc}$ ) is greater than the rectified voltage ( $V_{rec}$ ) and the command value ( $i_{rec}^*$ ) of the rectified current ( $i_{rec}$ ) is greater than or equal to a product of a predetermined value ( $dr\_max$ ) and a current ( $i_{dc}$ ) input to the inverter (6), the rectifying duty ( $dr$ ) takes the predetermined value, and the  
10 discharge duty ( $dc$ ) takes a value obtained by subtracting the predetermined value from 1.

[0026] The predetermined value is a value  $((V_{dc}^* - V_c)/(V_{rec} - V_c))$  obtained by dividing a value obtained by subtracting the voltage between both ends ( $V_c$ ) of the capacitor from the command value ( $V_{dc}^*$ ) of the virtual DC link voltage ( $V_{dc}$ ) by a value obtained by subtracting the voltage between both ends ( $V_c$ ) from the rectified voltage

15 ( $V_{rec}$ ).

[0027]

[0028]

[0029] In a ninth aspect of the direct AC power converter according to the present invention, in the first aspect or any one of the third and fifth to eighth aspects, the  
20 discharge duty ( $dc$ ) is always positive.

[0030] A tenth aspect of the direct AC power converter according to the present

invention, in any one of the first to ninth aspects, further includes a diode connected in parallel with the switch (41). A forward direction of the diode is a direction in which the capacitor (34) is charged from the DC link (7).

#### Effects of the Invention

5 [0031] The capacitor is charged in the boost chopper at least during a part of the period in which the discharge duty is greater than 0, so that an average value of maximum values of voltages that can be output from the inverter in a cycle of control of switching of the inverter can exceed  $1/\sqrt{2}$  times a crest value of the AC voltage.

[0032] A small discharge duty can be selected, and thus, the average value or the  
10 effective value of the current flowing in the inductor of the boost chopper can be reduced more than in the conventional technique.

[0033] These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### 15 Brief Description of Drawings

[0034] FIG. 1 is a circuit diagram illustrating a configuration of a direct AC power converter according to an embodiment;

FIG. 2 is a circuit diagram illustrating another configuration of the direct AC power converter according to the embodiment;

20 FIG. 3 is a circuit diagram of an equivalent circuit of the direct AC power converter according to the embodiment;

FIG. 4 is a block diagram illustrating a configuration of a controller of the direct AC power converter according to the embodiment;

FIG. 5 is a flowchart summarizing steps of obtaining a rectifying duty, a zero

voltage duty, a discharge duty, and a current command value;

FIGS. 6 and 7 are graphs showing waveforms of specifications of Example 1;

FIGS. 8 and 9 are graphs showing waveforms of specifications of Example 2;

FIG. 10 is a graph showing a relationship between a command value of a virtual

5 DC link voltage and a command value of an inverter;

FIG. 11 is a graph showing a relationship between a command value of the virtual DC link voltage and a command value of the inverter;

FIGS. 12 and 13 are graphs showing waveforms of specifications of Example 3;

FIG. 14 is a graph showing waveforms of currents flowing in inductors of  
10 Examples 2 and 3;

FIG. 15 is a graph showing waveforms of currents flowing through capacitors of Examples 2 and 3;

FIG. 16 is a graph showing an operation of an inverter of Example 2; and

FIG. 17 is a graph showing an operation of an inverter of Example 3.

## 15 Description of Embodiments

[0035] FIG. 1 is a circuit diagram illustrating a configuration of a direct AC power converter according to an embodiment.

[0036] The direct AC power converter includes a DC link 7, rectifying circuits 51 and 52, a boost chopper 3, a switch 41, and an inverter 6.

20 [0037] The DC link 7 has power supply lines L1 and L2. A potential lower than the potential of the power supply line L1 is applied to the power supply line L2.

[0038] The rectifying circuit 51 has input terminals 51a and 51b that receive an AC voltage  $V_{in}$  and a pair of output terminals 51c and 51d respectively connected to the power supply lines L1 and L2. The rectifying circuit 51 is of a full-wave rectification type. Illustrated herein is a case in which the rectifying circuit 51 is formed by a diode bridge.

[0039] FIG. 1 illustrates a state in which the AC voltage  $V_{in}$  is supplied to the rectifying circuit 51 from a single-phase AC power supply via a filter circuit 2. The filter circuit 2, however, is provided to cut off a harmonic noise, and thus, a cutoff frequency of the harmonic noise is higher than the frequency of the AC voltage  $V_{in}$ .

The function of the filter circuit 2 has hardly any influence on the operations of the respective sections described below, and accordingly, description will be given below without consideration of the operation of the filter circuit 2.

[0040] An operation of the switch 41 and switching operations of the boost chopper 3 and the inverter 6 are controlled by a controller 9. The controller 9 can be regarded as being included in the direct AC power converter as well.

[0041] The inverter 6 converts the voltage applied to the DC link 7 into another multi-phase AC voltage. Illustrated herein is a configuration in which the inverter 6 outputs a three-phase AC voltage to a permanent-magnet synchronous motor PMSM that serves as an inductive load. The inverter 6 is a voltage-source inverter that operates under instantaneous spatial vector control, and may have a publicly known configuration. The inverter 6 outputs a three-phase current  $I_{inv}$  to the permanent-magnet synchronous motor PMSM.

[0042] The boost chopper 3 has a capacitor 34 at its output stage. More specifically, a rectified voltage  $V_{rec}$  of the AC voltage  $V_{in}$  is applied to the boost chopper 3. The rectified voltage  $V_{rec}$  is generated by the rectifying circuit 52 of full-wave rectification type.

Illustrated herein is a case in which the rectifying circuit 52 is formed by a diode bridge.

[0043] The boost chopper 3 has an inductor 32, a switch 31, and a diode 33 in addition to the capacitor 34. The rectified voltage  $V_{rec}$  is applied between one end of the inductor 32 and one end of the switch 31. The other end of the inductor 32, the other  
5 end of the switch 31, and an anode of the diode 33 are connected to each other. The capacitor 34 is connected between a cathode of the diode 33 and the one end of the switch 31. For example, the switch 31 is an insulated gate bipolar transistor.

[0044] Such a configuration is publicly known as the boost chopper, and thus, detailed operation thereof will be omitted.

10 [0045] It is noted here that the switch 31 is conductive/non-conductive in accordance with activity/non-activity of a control signal  $S_b$  and that a boost duty  $db$  that is a time ratio at which the switch 31 is conductive is determined by a command value  $ib^*$  (described below) of a current  $ib$  flowing in the inductor 32, a capacitor voltage (voltage between both ends of the capacitor 34)  $V_c$  to be applied to the capacitor 34, and the  
15 rectified voltage  $V_{rec}$ .

[0046] The switch 41 performs discharge/non-discharge from the capacitor 34 to the DC link 7 in accordance with activity/non-activity of a control signal  $S_c$ . More specifically, the switch 41 is connected between the power supply lines L1 and L2 in series with the capacitor 34.

20 [0047] Normally, the boost chopper 3 operates to make the voltage between both ends of a capacitor (hereinbelow referred to as a "capacitor voltage")  $V_c$  higher than the rectified voltage  $V_{rec}$ . The switch 41 thus has a switch device for controlling whether to flow a current from the boost chopper 3 (more specifically, from the capacitor 34) toward the power supply line L1. For example, such a switch device is an insulated gate bipolar  
25 transistor.

[0048] A diode, a forward direction of which is the direction from the DC link 7 toward the boost chopper 3 (more specifically, from the power supply line L1 toward the capacitor 34), is desirably provided to charge the capacitor 34 with a regenerative current from the inverter 6.

5 [0049] The controller 9 receives an AC voltage  $V_{in}$  (more accurately, a signal indicating its waveform: the same applies to the following), a current  $I_{inv}$  output from the inverter 6, and a capacitor voltage  $V_c$ , and outputs control signals  $S_b$ ,  $S_c$ , and  $S_g$ . The control signal  $S_g$  is a signal for controlling switching of the inverter 6. Since illustrated herein is a case in which the inverter 6 outputs a three-phase voltage, the control signal  $S_g$  is a group composed of 6 ( $= 3 \times 2$ ) signals.

[0050] FIG. 2 is a circuit diagram illustrating another configuration of the direct AC power converter according to the embodiment. In comparison with the configuration shown in FIG. 1, the rectifying circuit 51 also serves as the rectifying circuit 52. That is to say, the pair of output terminals 51c and 51d of the rectifying circuit 5 are connected to an input side of the boost chopper 3. In this case, a rectified voltage  $V_{rec}$  is not always applied to the boost chopper 3, unlike the configuration shown in FIG. 1. This is because the other end of the inductor 32 is connected via the power supply line L1 to the switch 41, and depending on an operating status of the switch 41, the capacitor voltage  $V_c$  is applied to the boost chopper 3.

20 [0051] However, FIGs. 1 and 2 can be treated equivalently in an equivalent circuit described below, and thus, a control method described below is common. The equivalent circuit will be described first.

[0052] FIG. 3 is a circuit diagram of the equivalent circuit of each of the direct AC power converters shown in FIGs. 1 and 2. The rectified voltage  $V_{rec}$  is expressed as a voltage source, and accordingly, a switch  $G_{rec}$  indicates whether the rectifying circuit 51

is conductive. The switches 31 and 41 are respectively indicated by switches Gb and Gc. However, the regenerative current from the inverter 6 is not taken into consideration, and the diode of the switch 41 is not taken into consideration.

[0053] The inverter 6 and its load are expressed as a current source for flowing a DC current  $i_{dc}$  into the inverter 6. With the switch Gz conductive, the inverter 6 operates with a so-called zero voltage vector. When the inverter 6 operates with the zero voltage vector, the inverter 6 short-circuits with respect to an inductive load with any one of the power supply lines L1 and L2, and thus does not receive a current from the DC link 7.

[0054] The inverter 6 is allowed to operate with any vectors other than the zero voltage vector when the inverter 6 receives a current from the DC link 7. The inverter 6 thus operates with any vectors other than the zero voltage vector when the switch Gz is not conductive.

[0055] When the capacitor voltage  $V_c$  higher than the rectified voltage  $V_{rec}$  is applied to the DC link 7, no current flows in the DC link 7 from the rectifying circuit 51. That is to say, the switch G<sub>rec</sub> is not conductive when the switch Gc is conductive.

[0056] As described in Patent Documents 1 and 2 above, when time ratios at which the switches G<sub>rec</sub>, Gc, and Gz are conductive are respectively a rectifying duty  $d_r$ , a discharge duty  $d_c$ , and a zero voltage duty  $d_z$ , a sum of the three time ratios is 1. That is to say, Expression (1) below holds, where these time ratios are time ratios in a cycle shorter than a cycle of the AC voltage  $V_{in}$  and are time ratios regarding a carrier cycle controlled with approximation that the AC voltage  $V_{in}$  is constant.

$$[0057] \quad d_r + d_c + d_z = 1 \dots (1)$$

[0058] The zero voltage duty  $d_z$  is a time ratio corresponding to a period during which the inverter 6 adopts the zero voltage vector irrespective of the magnitude of a voltage to be output. The discharge duty  $d_c$  is a time ratio at which the switch 41 is conductive.

[0059] The rectifying duty  $d_r$  is a time ratio at which the rectifying circuit 51 is conductive. Expression (1) reveals that the rectifying duty  $d_r$  takes a value obtained by subtracting a sum of the discharge duty  $d_c$  and the zero voltage duty  $d_z$  from 1.

[0060] As the DC voltage applied to the DC link 7, the capacitor voltage  $V_c$  is adopted when the switch 41 is conductive and the rectified voltage  $V_{rec}$  is adopted when the switch 41 is not conductive. Here, a virtual voltage (referred to as a "virtual DC link voltage" in this application)  $V_{dc}$  is determined according to Expression (2) below.

$$[0061] \quad V_{dc} = d_r \cdot V_{rec} + d_c \cdot V_c \dots (2)$$

[0062] That is to say, the virtual DC link voltage  $V_{dc}$  is expressed as a sum of a product ( $d_c \cdot V_c$ ) of the discharge duty  $d_c$  and the capacitor voltage  $V_c$  and a product ( $d_r \cdot V_{rec}$ ) of the rectifying duty  $d_r$  and the rectified voltage  $V_{rec}$ . This can also be understood as an average of maximum values of voltages that the inverter 6 is capable of output in a cycle of control of switching of the switch 41 and the inverter 6. FIG. 3 shows the virtual DC link voltage  $V_{dc}$  as a voltage generated between both ends of the current source  $i_{dc}$  (this flows the DC current  $i_{dc}$ ) representing the inverter 6 and its load.

[0063] The virtual DC link voltage  $V_{dc}$  is an average value of the maximum values of a voltage that the inverter 6 is capable of output as described above, and thus, the voltage output from the inverter 6 may fall below the virtual DC link voltage  $V_{dc}$ . In such a case, the inverter 6 adopts the zero voltage vector even when the switch 41 is conductive.

This reflects a fact that as described above, the zero voltage duty  $d_z$  is a time ratio corresponding to a period during which the inverter 6 adopts the zero voltage vector irrespective of the magnitude of the voltage output from the inverter 6 but is not a time ratio corresponding to all the periods during which the inverter 6 adopts the zero voltage vector.

[0064] In such an equivalent circuit, a current  $i_{rec}$  from the voltage source indicating

the rectified voltage  $V_{rec}$  (referred to as a "rectified current" in this application) is understood as a sum of the current  $i_b$  flowing in the inductor 32 (of the boost chopper 3) and a current  $i_{direct}$  flowing from the rectifying circuit 51 into the inverter 6 in an actual configuration.

5 [0065] In the configuration shown in FIG. 1, the rectified current  $i_{rec}$  is not directly indicated. With reference to FIG. 1, the current  $i_{direct}$  is a current flowing from the rectifying circuit 51 into the DC link 7, and the current  $i_b$  is a current flowing from the rectifying circuit 52 into the boost chopper 3.

[0066] In the configuration shown in FIG. 2, the rectified current  $i_{rec}$  is output from  
10 the output terminal 51c, and a portion thereof that flows into the inductor 32 is the current  $i_b$ .

[0067] Since the switch  $G_{rec}$  indicates the conductivity/non-conductivity of the rectifying circuit 51, the rectifying duty  $d_r$  that is a time ratio at which the rectifying circuit 51 is conductive is expressed as a value obtained by dividing the current  $i_{direct}$  by  
15 the DC current  $i_{dc}$ . Thus, Expression (3) below holds.

$$[0068] \quad i_{rec} = d_r \cdot i_{dc} + i_b \dots (3)$$

[0069] In Patent Documents 1 and 2 and Non-Patent Document 1 above, a period during which the current  $i_b$  is allowed to flow is excluded from a period (providing period) during which the capacitor 34 provides electric power to the DC link 7.  
20 Furthermore, the providing period and a period (receiving period) during which the capacitor 34 receives electric power from the DC link 7 are set alternately in each 1/4 of the cycle of the AC voltage  $V_{in}$ . For this reason, the virtual DC link voltage  $V_{dc}$  does not exceed  $1/\sqrt{2}$  times a crest value of the AC voltage.

[0070] However, the capacitor 34 is not always discharged and is conductive at the  
25 discharge duty  $d_c$  even during the providing period. Therefore, even the providing

period includes a period during which the capacitor 34 can be charged. In contrast, the providing period is necessary in a period during which the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$ . This is because, even with  $dc = 0$ , as is clear from Expression (2), the virtual DC link voltage  $V_{dc}$  can be determined only by the rectified voltage  $V_{rec}$ , the rectifying duty  $d_r$ , and the zero voltage duty  $d_z$  when the  
 5 virtual DC link voltage  $V_{dc}$  is smaller than the rectified voltage  $V_{rec}$ .

[0071] In other words, at least during a part of the period during which the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$  ( $dc > 0$  during this period: a reason for this will be described below), the capacitor 34 is charged in the boost chopper  
 10 3 so that the capacitor 34 is supplemented with an electric power. As a result, the virtual DC link voltage  $V_{dc}$  can exceed  $1/\sqrt{2}$  times the crest value of the AC voltage  $V_{in}$ . Needless to say, the capacitor 34 can be charged during a part or whole of the period during which  $dc = 0$ .

[0072] Alternatively, the period during which the capacitor 34 is charged can be set to  
 15 be longer than in a conventional technique even when the virtual DC link voltage  $V_{dc}$  does not exceed  $1/\sqrt{2}$  times the crest value of the AC voltage  $V_{in}$ , thus reducing an average value or an effective value of the current  $i_b$  flowing in the inductor 32 more than in a conventional technique.

[0073] More detailed description will be given below. The discharge duty  $dc$  is  
 20 desirably set to be small in order to reduce a loss in the boost chopper 3 and a rated current required for the inductor 32.

[0074] Considered first is the case in which the rectified current  $i_{rec}$  is greater than the current  $i_{direct}$ . According to Expression (3), this is the case in which there is a margin for flowing the current  $i_b$  in the boost chopper 3, and the magnitude of the rectifying duty  
 25  $d_r$  is not limited by the rectified current  $i_{rec}$ . In this case, the case in which the virtual

DC link voltage  $V_{dc}$  is made to be smaller than or equal to the rectified voltage  $V_{rec}$  is considered as a first case. In the first case,  $dc = 0$  and  $dz > 0$  as described above. Specifically, setting is made such that  $dc = 0$  in Expressions (1) and (2), so that the rectifying duty  $dr$  and the zero voltage duty  $dz$  in the first case are determined by

5 Expression (4) below. At this time, the capacitor 34 is not discharged via the switch 41.

[0075]  $dr = V_{dc}/V_{rec}, dz = 1 - V_{dc}/V_{rec} \dots (4)$

[0076] In other words, it is revealed that when a command value  $V_{dc}^*$  of the virtual DC link voltage  $V_{dc}$  is set, the rectifying duty  $dr$  should be set to a ratio ( $V_{dc}^*/V_{rec}$ ) of the command value  $V_{dc}^*$  to the rectified voltage  $V_{rec}$ , and the zero voltage duty  $dz$

10 should be set to a value obtained by subtracting the ratio from 1 in order to cause the virtual DC link voltage  $V_{dc}$  to follow the command value  $V_{dc}^*$  with the discharge duty  $dc$  being zero in the first case.

[0077] It is also revealed that the zero voltage duty  $dz$  is minimum in this case. This is because, according to Expression (2), the zero voltage duty  $dz$  needs to be increased in

15 order to match the virtual DC link voltage  $V_{dc}$  with the command value  $V_{dc}^*$  even when the discharge duty  $dc$  increases.

[0078] In other words, in the first case, setting the rectifying duty  $dr$  to the ratio ( $V_{dc}^*/V_{rec}$ ) can be regarded as setting a discharge duty  $dc$  for making the zero voltage duty  $dz$  minimum and setting a value of the discharge duty  $dc$  to 0.

20 [0079] When the control above is performed in the first case, the capacitor 34 is not discharged.

[0080] The case in which the rectified current  $i_{rec}$  is greater than the current  $i_{direct}$  and the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$  is considered as a second case. In this case, it is obvious from Expression (2) that the discharge from the

25 capacitor 34 to the DC link 7 needs to be performed. That is to say, the discharge duty

dc is positive. It is also obvious from Expression (2) that the virtual DC link voltage  $V_{dc}$  should be smaller than or equal to the capacitor voltage  $V_c$ .

[0081] A zero voltage duty  $d_z$  that does not contribute to a rise in the virtual DC link voltage  $V_{dc}$  needs to be reduced in order to reduce the discharge duty  $d_c$  for reduced loss  
5 or rated current. In the second case, the magnitude of the rectifying duty  $d_r$  is not limited by the rectified current  $i_{rec}$  as in the first case, and thus, the DC current  $i_{dc}$  can be fed by the rectified current  $i_{rec}$ . The zero voltage duty  $d_z$  can therefore be reduced to zero.

[0082] According to the above and Expression (1), Expression (2) can be transformed  
10 into Expression (5) below.

$$\begin{aligned} [0083] \quad V_{dc} &= d_r \cdot V_{rec} + (1 - d_r) \cdot V_c \\ \therefore d_r &= (V_{dc} - V_c) / (V_{rec} - V_c) \dots (5) \end{aligned}$$

[0084] In other words, it is found that in order to cause the virtual DC link voltage  $V_{dc}$  to follow the command value  $V_{dc}^*$  in the second case, the rectifying duty  $d_r$  should be set  
15 to a ratio  $(V_{dc}^* - V_c) / (V_{rec} - V_c)$ , and the discharge duty  $d_c$  should be set to a value obtained by subtracting the ratio from 1.

[0085] In the second case, setting the rectifying duty  $d_r$  as described above can be regarded as setting the discharge duty  $d_c$  to make the zero voltage duty  $d_z$  minimum and setting a value of the discharge duty  $d_c$  to  $(1 - d_r)$ . This is because the zero voltage duty  
20  $d_z$  reduces to zero also in this case.

[0086] It can be regarded that the control of each duty means setting the discharge duty  $d_c$  for making the zero voltage duty  $d_z$  minimum based on two viewpoints. The first viewpoint is whether the rectified current  $i_{rec}$  is greater than the current  $i_{direct}$ , that is, whether the command value  $i_{rec}^*$  of the rectified current  $i_{rec}$  is set to be greater than the  
25 current  $i_{direct}$ . The second viewpoint is whether the virtual DC link voltage  $V_{dc}$  is

greater than the rectified voltage  $V_{rec}$ , that is, whether the command value  $V_{dc}^*$  is greater than the rectified voltage  $V_{rec}$ .

[0087] The circuit shown in FIG. 1 can afford to flow the current  $i_b$  from the rectifying circuit 52, and the circuit shown in FIG. 2 can afford to flow the current  $i_b$  from the rectifying circuit 51. Therefore, when the DC current  $i_{dc}$  is estimated, the use of an estimated value  $i_{dc}^{\wedge}$  thereof allows the command value  $i_b^*$  of the current  $i_b$  to be set according to Expression (6) below in consideration of Expression (3).

$$[0088] \quad i_b^* = i_{rec}^* - dr_{max} \cdot i_{dc}^{\wedge} \dots (6)$$

[0089] Herein,  $dr_{max}$  is a rectifying duty  $dr$  represented by Expression (4) in the first case and by Expression (5) in the second case.

[0090] In particular, when the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$  as in the second case, a providing period appears during which discharge is performed from the capacitor 34 to the DC link 7 at the discharge duty  $dc$ . During this providing period, the current  $i_b$  flows in accordance with the command value  $i_b^*$  represented by Expression (6), and thus, not only the discharge but also the charge of the capacitor 34 is performed.

[0091] In this application, therefore, the period corresponding to the second case is referred to as a "charge and discharge zone". In contrast, the period corresponding to the first case is referred to as a "charge zone" in this application because the capacitor 34 is not discharged but is only charged.

[0092] A known approach can be employed for a switching operation to be performed by a switch  $G_b$  (switch 31) using the current  $i_b$  flowing in the boost chopper 3 to charge the capacitor 34 to the capacitor voltage  $V_c$ . This approach may be of a so-called discontinuous current mode, a critical mode, or a continuous current mode.

[0093] The case in which the rectified current  $i_{rec}$  is smaller than or equal to the

current  $i_{direct}$  is then considered as a third case. This is the case in which there is no margin for flowing the current  $i_b$  with reference to Expression (3). Alternatively, this is the case in which  $i_b^* < 0$  with reference to Expression (6), that is, the case in which Expression (7) below holds.

5 [0094]  $i_{rec}^* < d_{r\_max} \cdot i_{dc}^{\wedge} \dots (7)$

[0095] The current  $i_b$  does not actually take a negative value, and thus, the rectifying duty  $d_r$  that takes a value smaller than  $d_{r\_max}$  is adopted under the condition of Expression (7) so that Expression (3) is established under conditions where  $i_{rec} \geq 0$ ,  $d_r \geq 0$ ,  $i_{dc} > 0$ , and  $i_b \geq 0$ .

10 [0096] The command value  $i_b^*$  of the current  $i_b$  is set to 0 so as to always satisfy  $i_b \geq 0$ . That is to say, the capacitor 34 is not charged during a period during which Expression (7) holds, and the capacitor 34 is discharged at a discharge duty  $d_c$  determined below. In this application, therefore, the period during which Expression (7) holds is referred to as a "discharge zone".

15 [0097] The rectifying duty  $d_r$  is determined according to Expression (8) below with the use of the command value  $i_{rec}^*$  and the estimated value  $i_{dc}^{\wedge}$ , in consideration of Expression (7).

[0098]  $d_r = i_{rec}^* / i_{dc}^{\wedge} \dots (8)$

[0099] That is to say, in order to cause the virtual DC link voltage  $V_{dc}$  to follow the  
20 command value  $V_{dc}^*$ , the rectifying duty  $d_r$  is set to a ratio ( $i_{rec}^* / i_{dc}^{\wedge}$ ) of the command value  $i_{rec}^*$  to the estimated value  $i_{dc}^{\wedge}$ .

[0100] Expression (9) below needs to hold in consideration of Expression (2) in order to cause the virtual DC link voltage  $V_{dc}$  to follow the command value  $V_{dc}^*$ .

[0101]  $V_{dc}^* = d_r \cdot V_{rec} + d_c \cdot V_c \dots (9)$

25 [0102] Herein, the rectifying duty  $d_r$  is set to a value set by Expression (8), and the

capacitor voltage  $V_c$  is substantially fixed. Thus, parameters that can be selected to make the right side of Expression (9) equal to the given command value  $V_{dc}^*$  are the zero voltage duty  $d_z$  and the discharge duty  $d_c$ .

[0103] The discharge duty  $d_c$  is determined according to Expression (10) below  
5 directly led from Expression (9).

$$[0104] \quad d_c = (V_{dc}^* - d_r \cdot V_{rec}) / V_c \dots (10)$$

[0105] It is noted that the capacitor voltage  $V_c$  technically reduces during the period during which Expression (7) holds ("discharge zone"). This is because the command value  $i_b^*$  is set to 0 as described above. However, appropriately setting the command  
10 value  $i_{rec}^*$  reduces the discharge zone to such an extent that a reduction in the capacitor voltage  $V_c$  can be ignored.

[0106] In Patent Documents 1 and 2 and Non-Patent 1 described above, the rectified current  $i_{rec}$  has a waveform of full-wave rectification, and thus, such selection of the command value  $i_{rec}^*$  was not considered. However, in this embodiment, since the  
15 rectified current  $i_{rec}$  is not limited to the waveform of full-wave rectification, the discharge zone is shortened, and the discharge duty  $d_c$  can be set with Expression (10) where the capacitor voltage  $V_c$  is constant.

[0107] Due to the restricting condition of Expression (1), the zero voltage duty  $d_z$  is obtained by Expression (11) below.

$$20 \quad [0108] \quad d_z = 1 - d_r - d_c \dots (11)$$

[0109] As described above, during the discharge zone, the rectifying duty  $d_r$  is determined according to Expression (8) when the command value  $i_{rec}^*$  and the estimated value  $i_{dc}^{\wedge}$  are obtained, and further, the discharge duty  $d_c$  and the zero voltage duty  $d_z$  are uniquely determined according to Expressions (10) and (11), respectively.

25 [0110] That is to say, the zero voltage duty  $d_z$  is not allowed to take a value greater

than or equal to a value determined by Expression (11), and is thus considered to be set to a minimum value thereof. That is to say, it can be regarded that the discharge duty  $d_c$  to make the zero voltage duty  $d_z$  minimum is set also in the discharge zone as in the charge zone and the charge and discharge zone.

5 [0111] When the rectifying duty  $d_r$ , the zero voltage duty  $d_z$ , the discharge duty  $d_c$ , and the command value  $i_b^*$  are determined in the manner above, the control signals  $S_b$ ,  $S_c$ , and  $S_g$  can be generated using a known technique.

[0112] FIG. 4 is a block diagram illustrating a configuration of the controller 9. The controller 9 is roughly divided into a current command generator 91, a DC current ( $i_{dc}$ ) estimator 92, a duty divider 93, a pulse width modulation (PWM) signal generator 94, and  
10 a chopper signal generator 95.

[0113] The current command generator 91 generates the command value  $i_{rec}^*$  of the rectified current  $i_{rec}$ . Although FIG. 4 illustrates a configuration in which the command value  $i_{rec}^*$  has an absolute value of a sinusoidal waveform as described below, the  
15 command value  $i_{rec}^*$  is not always limited to providing such a waveform.

[0114] The DC current estimator 92 obtains the estimated value  $i_{dc}^{\wedge}$  of the DC current  $i_{dc}$ . As is understood from the equivalent circuit of FIG. 3, an actual circuit has no portion that can actually measure the DC current  $i_{dc}$ . Therefore, the estimated value  $i_{dc}^{\wedge}$  is adopted in the computations represented by Expressions (6) and (8).

20 [0115] An electric power to be output from the inverter 6 can be obtained in the equivalent circuit from the DC current  $i_{dc}$  and the virtual DC link voltage  $V_{dc}$ . In contrast, an electric power to be output from the inverter 6 in an actual circuit is obtained from a three-phase current  $i_{inv}$  and a three-phase voltage  $V_{inv}$  to be output from the inverter 6. Therefore, theoretically, the estimated value  $i_{dc}^{\wedge}$  can be obtained from the  
25 virtual DC link voltage  $V_{dc}$ , the current  $i_{inv}$ , and the voltage  $V_{inv}$ .

[0116] It is noted that the voltage  $V_{inv}$  to be output from the inverter 6 is controlled by the pulse width modulation signal generator 94 to follow its command value  $V_{inv}^*$ . The virtual DC link voltage  $V_{dc}$  cannot be measured per se, but is controlled by the duty divider 93 to follow the command value  $V_{dc}^*$ . The current  $i_{inv}$  can be measured from  
 5 wire connection between the inverter 6 and the permanent-magnet synchronous motor PMSM. In this embodiment, therefore, the estimated value  $\hat{i}_{dc}$  is obtained from the command values  $V_{dc}^*$  and  $V_{inv}^*$  and the current  $i_{inv}$ . Needless to say, the estimated value  $\hat{i}_{dc}$  may be obtained by another method.

[0117] The duty divider 93 determines the rectifying duty  $d_r$ , the zero voltage duty  $d_z$ ,  
 10 the discharge duty  $d_c$ , and the command value  $i_b^*$  in accordance with the methods described in the first to third cases on the basis of the command values  $V_{dc}^*$  and  $i_{rec}^*$ , the capacitor voltage  $V_c$ , the rectified voltage  $V_{rec}$ , and the estimated value  $\hat{i}_{dc}$ . The expression "duty 'divider'" is given here because as represented by Expression (2), a value 1 is divided by the rectifying duty  $d_r$ , the zero voltage duty  $d_z$ , and the discharge duty  $d_c$ .

15 [0118] The pulse width modulation signal generator 94 generates the control signals  $S_c$  and  $S_g$  on the basis of the rectifying duty  $d_r$ , the zero voltage duty  $d_z$ , the discharge duty  $d_c$ , and the command values  $V_{inv}^*$  and  $V_{dc}^*$ . For example, these duties and respective phase portions of the command value  $V_{inv}^*$  are operated to generate signal waves, and the signal waves can be compared to a triangular carrier to generate the control signals  $S_c$   
 20 and  $S_g$ . Since such a method is publicly known and is described in, for example, Patent Documents 1 and 2, detailed description thereof will be omitted.

[0119] The chopper signal generator 95 has a boost chopper duty arithmetic unit 951 and a pulse width modulation (PWM) signal generator 952. The boost chopper duty arithmetic unit 951 determines the boost duty  $d_b$  on the basis of the command value  $i_b^*$ ,  
 25 the capacitor voltage  $V_c$ , and the rectified voltage  $V_{rec}$ .

[0120] A method for determining the boost duty  $db$  differs depending on a mode in which the boost chopper 3 operates. The method may be a normal method for determining the discharge duty of a boost chopper, and thus, detailed description thereof will be omitted.

5 [0121] The pulse width modulation signal generator 952 can also generate the control signal  $S_b$  from the boost duty  $db$  by a known modulation method.

[0122] A configuration of the current command generator 91 will now be described.

The current command generator 91 has an output power ( $P_{out}$ ) estimator 911, a trigonometric function value generator 912, a capacitor voltage controller 913, an adder  
10 914, a multiplier 915, and a divider 916.

[0123] The output power estimator 911 obtains an estimated value  $P_{out}^{\wedge}$  of an output power  $P_{out}$  based on the command value  $V_{inv}^*$  and the current  $i_{inv}$ . The DC current estimator 92, which obtains the estimated value  $idc^{\wedge}$  as described above, may receive  
15 inputs of the estimated value  $P_{out}^{\wedge}$  obtained from the output power estimator 911 and the command value  $V_{dc}^*$  so as to obtain the estimated value  $idc^{\wedge}$ .

[0124] The capacitor voltage controller 913 obtains a deviation  $V_c^* - V_c$  between the capacitor voltage  $V_c$  and its command value  $V_c^*$  and performs at least proportional control on the deviation  $V_c^* - V_c$ , then outputting the deviation  $V_c^* - V_c$  to the adder  
914.

20 [0125] The adder 914 adds an output from the capacitor voltage controller 913 to the estimated value  $P_{out}^{\wedge}$ . This is a process for suitably setting a command value  $P_{in}^*$  of the input power by correcting the estimated value  $P_{out}^{\wedge}$  to be greater/smaller when the capacitor voltage  $V_c$  becomes smaller/greater than the command value  $V_c^*$ , thus reducing the deviation. For stability of the deviation, the capacitor voltage controller  
25 913 desirably adopts not mere proportional control itself but proportional-integral control

or proportional-integral-derivative control.

[0126] Assumed here is a case in which the command value  $i_{rec}^*$  of the rectified current  $i_{rec}$  takes an absolute value of the sinusoidal waveform. The rectified voltage  $V_{rec}$  takes the absolute value of the sinusoidal waveform, and thus, an output from the adder 914 is multiplied by a trigonometric function value  $2 \cdot \sin^2 \theta$ , thus obtaining the command value  $P_{in}^*$ .

[0127] The trigonometric function value generator 912 generates the trigonometric function value  $2 \cdot \sin^2 \theta$  based on a phase angle  $\theta$  of the power-supply voltage. The multiplier 915 multiplies an addition result of the adder 914 and the trigonometric function value  $2 \cdot \sin^2 \theta$  to obtain the command value  $P_{in}^*$ .

[0128] Since an input power  $P_{in}$  is a product of the rectified voltage  $V_{rec}$  and the rectified current  $i_{rec}$ , the command value  $i_{rec}^*$  of the rectified current  $i_{rec}$  is obtained by dividing the command value  $P_{in}^*$  by the rectified voltage  $V_{rec}$ .

[0129] The phase angle  $\theta$  is estimated from, for example, the measured AC voltage  $V_{in}$  by a power-supply phase estimator 96. The power-supply phase estimator 96 can be constituted by, for example, a phase locked loop. The rectified voltage  $V_{rec}$  can be obtained, for example, in such a manner that an absolute value circuit 97 obtains an absolute value of the measured AC voltage  $V_{in}$ . Since specific configurations of the power-supply phase estimator 96 and the absolute value circuit 97 are publicly known techniques, which will not be described here in detail.

[0130] The command value  $V_{dc}^*$  is set by a virtual DC link voltage command value generator 98 on the basis of the command value  $V_{inv}^*$  according to the expression below. It is noted that the command value  $V_{dc}^*$  is a maximum value of the voltage  $V_{inv}$  (which is, here, an average in a cycle of controlling switching) of the inverter 6 as described above, and thus, setting the command value  $V_{dc}^*$  below the command value  $V_{inv}^*$  is not

appropriate. In other words, the command value  $V_{dc}^*$  needs to be increased in order to increase a maximum value of the command value  $V_{inv}^*$ . In a conventional direct power converter, the command value  $V_{dc}^*$  is smaller than or equal to  $1/\sqrt{2}$  times the AC voltage  $V_{in}$ .

5 [0131] FIG. 5 is a flowchart summarizing steps of obtaining the rectifying duty  $d_r$ , the zero voltage duty  $d_z$ , the discharge duty  $d_c$ , and the command value  $i_b^*$ . It is grasped that this flowchart shows an operation of the duty divider 93.

[0132] Step S101 corresponds to a determination whether the operation of the direct AC power converter corresponds to the first case or the second case on the assumption  
10 that the operation does not correspond to the third case. It is determined in Step S101 whether the command value  $V_{dc}^*$  of the virtual DC link voltage  $V_{dc}$  is smaller than or equal to the rectified voltage  $V_{rec}$ . The process proceeds to Steps S102 and S104 if the determination is affirmative or proceeds to Steps S103 and S105 if the determination is negative.

15 [0133] Steps S102 and S104 are processes for determining whether the operation of the direct AC power converter corresponds to the first case or the third case. In Step S102,  $d_{r\_max} = V_{dc}^*/V_{rec}$  is obtained in consideration of Expression (4). It is determined in Step S104 whether the command value  $i_{rec}^*$  is greater than or equal to a value  $d_{r\_max} \cdot i_{dc}^*$  in consideration of Expression (7). If the determination in Step S104 is affirmative,  
20 the operation of the direct AC power converter corresponds to the first case, and the process proceeds to Steps S106 and S109. If the determination in Step S104 is negative, the operation of the direct AC power converter corresponds to the third case, and the process proceeds to Steps S108 and S110.

[0134] Steps S103 and S105 are processes for determining whether the operation of the  
25 direct AC power converter corresponds to the second case or the third case. In Step

S103,  $dr\_max = (V_{dc}^* - V_c)/(V_{rec} - V_c)$  is obtained in consideration of Expression (5).

In Step S105, whether the command value  $i_{rec}^*$  is greater than or equal to the value  $dr\_max \cdot i_{dc}^*$  is determined in consideration of Expression (7) as in Step S104. If the

determination of Step S105 is affirmative, the operation of the direct AC power converter

5 corresponds to the second case, and the process proceeds to Steps S107 and S109. If the determination is negative in Step S105, the operation of the direct AC power converter corresponds to the third case, and the process proceeds to Steps S108 and S110.

[0135] Steps S106, S107, and S108 are setting of duties respectively corresponding to the first case, the second case, and the third case. Step S109 is the setting of the

10 command value  $i_b^*$  according to the first case and the second case, and Step S110 is the setting of the command value  $i_b^*$  according to the third case. These setting contents are as described above.

[0136] If  $V_{dc} > V_{rec}$ , Step S107 or S108 is performed according to the determination result of Step S101. When Step S107 is performed, the discharge duty  $dc$  takes a value

15  $(1 - dr)$ . In this case, the rectifying duty  $dr$  is represented by Expression (5) and is smaller than 1. In this case, therefore, the discharge duty  $dc$  is greater than 0.

[0137] When Step S108 is performed, the discharge duty  $dc$  takes a value represented by Expression (10). If  $V_{dc} > V_{rec}$ , a numerator of the right side of Expression (10) is greater than 0 irrespective of the value of the rectifying duty  $dr$ . Also in this case,

20 therefore, the discharge duty  $dc$  is greater than 0.

[0138] That is to say, when  $V_{dc} > V_{rec}$ , setting is always made such that  $dc > 0$ .

[0139] The controller 9 can be implemented by, for example, a microcomputer and a storage device. The microcomputer executes the respective steps (in other words, the procedure) described in a program. The storage device can be configured by, for

25 example, one or a plurality of various storage devices such as a ROM (Read Only

Memory), a RAM (Random Access Memory), a rewritable non-volatile memory (such as EPROM (Erasable Programmable ROM)), and a hard disc device. The storage device stores various information, data, and the like, stores a program to be executed by the microcomputer, and provides a work area for executing the program. It can be grasped  
 5 that the microcomputer functions as various means corresponding to the respective processing steps described in the program or implements various functions corresponding to the respective steps. Further, the controller 9 is not limited to this, and some or all of various procedures (such as obtaining respective measured values and executing Steps S101 to S110) to be executed by the controller 9, or respective elements or various  
 10 functions of the controller 9 may be implemented by hardware.

[0140] Examples

Examples describing the effects of the use of the above methods will be described below.

[0141] Two examples of the case in which the command value  $V_{dc}^*$  takes a constant  
 15 value will be described first, and then, an example of a desirable value of the command value  $V_{dc}^*$  will be described.

[0142] Example 1

FIGs. 6 and 7 are graphs showing waveforms of specifications obtained by simulation. It is noted that the virtual DC link voltage  $V_{dc}$  is set to  $1/\sqrt{2}$  (212 V) of a  
 20 crest value (300 V) of the rectified voltage  $V_{rec}$ . The capacitor voltage  $V_c$  is higher than the rectified voltage  $V_{rec}$  and is constant (400 V) (the same applies to the following).

[0143] A first tier of FIG. 6 shows waveforms of the capacitor voltage  $V_c$ , the rectified voltage  $V_{rec}$ , and the virtual DC link voltage  $V_{dc}$  (this is assumed to accurately follow its  
 25 command value  $V_{dc}^*$ : the same applies to the following).

[0144] A second tier of FIG. 6 shows waveforms of the rectified current  $i_{rec}$  (this is assumed to accurately follow its command value  $i_{rec}^*$ : the same applies to the following) and the DC current  $i_{dc}$  (this is assumed to accurately estimated by the estimated value  $i_{dc}^{\wedge}$ : the same applies to the following). The DC current  $i_{dc}$  set to a constant value, in cooperation with the virtual DC link voltage  $V_{dc}$  that takes a constant value, makes the output power  $P_{out}$  constant.

[0145] A third tier of FIG. 6 shows waveforms of the rectified current  $i_{rec}$ , the current  $i_{direct}$  (this is obtained by a product of the rectifying duty  $d_r$  and the estimated value  $i_{dc}^{\wedge}$ : the same applies to the following), and the current  $i_b$  (this is assumed to accurately follow the command value  $i_b^*$ : the same applies to the following).

[0146] A fourth tier of FIG. 6 shows waveforms of the rectifying duty  $d_r$ , the discharge duty  $d_c$ , and the zero voltage duty  $d_z$ .

[0147] A fifth tier of FIG. 6 shows waveforms of the DC current  $i_{dc}$ , the current  $i_{direct}$ , the current  $i_c$  flowing from the capacitor 34 to the DC link 7 (this is obtained by a product of the discharge duty  $d_c$  and the estimated value  $i_{dc}^{\wedge}$ : the same applies to the following), and a zero-phase current  $i_z$  (this is obtained by a product of the zero voltage duty  $d_z$  and the estimated value  $i_{dc}^{\wedge}$ : the same applies to the following).

[0148] A first tier of FIG. 7 shows waveforms of an output power  $P_{out}$  to be output from the inverter 6 (this is assumed to be accurately estimated by its estimated value  $P_{out}^{\wedge}$ : the same applies to the following), an electric power  $P_{direct}$  to be determined based on the rectified voltage  $V_{rec}$  and the current  $i_{direct}$ , an electric power (discharge power)  $P_{co}$  to be discharged from the capacitor 34, and an electric power  $P_c$  to be input/output to/from the capacitor 34. The electric power  $P_c$  takes a negative value because it reduces the output power  $P_{out}$  in charging.

[0149] A second tier of FIG. 7 shows waveforms of the input power  $P_{in}$  (this is

assumed to accurately follow the command value  $P_{in}^*$ : the same applies to the following), the electric power  $P_{direct}$ , an electric power (charge power)  $P_{ci}$  with which the capacitor 34 is charged, and the electric power  $P_c$ .

[0150] A third tier of FIG. 7 is a graph summarizing electric powers  $P_c$ ,  $P_{ci}$ , and  $P_{co}$  related to the capacitor 34, which are extracted from the first and second tiers of FIG. 7.

[0151] The capacitor 34 is charged but is not discharged during "charge" periods in FIGs. 6 and 7 ( $P_{ci} > 0$ ,  $P_{co} = 0$ ). Specifically, the "charge" period is a period during which the virtual DC link voltage  $V_{dc}$  is smaller than or equal to the rectified voltage  $V_{rec}$  and  $i_c = 0$  (that is,  $dc = 0$ ), and Steps S106 and S109 of FIG. 5 are performed.

10 [0152] The capacitor 34 is discharged but is not charged during the "discharge" period ( $P_{co} > 0$ ,  $P_{ci} = 0$ ). Specifically, the "discharge" period is a period during which the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$  and  $i_z > 0$  (that is,  $dz > 0$ ), and Steps S108 and S110 of FIG. 5 are performed.

[0153] The "charge and discharge" period is a period during which the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$  and  $i_z = 0$  (that is,  $dz = 0$ ), and Steps S107 and S109 of FIG. 5 are performed. The "charge and discharge" period includes a period during which the electric power  $P_{ci}$  with which the capacitor 34 is charged is greater than the electric power  $P_{co}$  to be discharged from the capacitor 34 (that is, a period during which  $P_c < 0$ : this is adjacent to the "charge" period and is separate from the "discharge" period) and a period during which the electric power  $P_{co}$  to be discharged from the capacitor 34 is greater than the electric power  $P_{ci}$  with which the capacitor 34 is charged (that is, the period during which  $P_c > 0$ : this is adjacent to the "discharge" period and is separate from the "charge" period).

[0154] The "charge and discharge" period is provided and the capacitor 34 is charged also in this period as described above, so that the average value or the effective value of

the current  $i_b$  can be reduced more than in the conventional technique in which a capacitor is charged only during the "charge" period. This contributes to a reduction in the rated current required for the inductor 32, and accordingly, a reduction in the power capacity required for the boost chopper 3.

5 [0155] It is noted that in the case shown in FIGs. 6 and 7, the virtual DC link voltage  $V_{dc}$  is set to  $1/\sqrt{2}$  times the crest value of the rectified voltage  $V_{rec}$ . Therefore, the following will be described: while the rectified current  $i_{rec}$  has a sinusoidal waveform, the virtual DC link voltage  $V_{dc}$  can be set to be higher than  $1/\sqrt{2}$  times the crest value of the rectified voltage  $V_{rec}$ .

10 [0156] Example 2

FIGs. 8 and 9 are graphs showing waveforms of specifications obtained by simulation through control in accordance with the method of this embodiment. FIG. 8 shows the waveforms of the specifications corresponding to FIG. 6. FIG. 9 shows the waveforms of the specifications corresponding to FIG. 7 except for the graph shown in  
15 the lowest tier. FIGs. 8 and 9 show the case in which the crest value of the rectified voltage  $V_{rec}$  is set to 300 V as in FIGs. 6 and 7, the virtual DC link voltage  $V_{dc}$  is set to be equal to the crest value of the rectified voltage  $V_{rec}$ , and the waveform of the rectified current  $i_{rec}$  is the absolute value of the sinusoidal wave.

[0157] When the virtual DC link voltage  $V_{dc}$  is equal to the crest value of the rectified  
20 voltage  $V_{rec}$  as described above,  $dc = 0$  holds only at a phase of  $90^\circ$  or  $270^\circ$ . FIGs. 8 and 9 therefore show no "charge" period.

[0158] Further, when the virtual DC link voltage  $V_{dc}$  is smaller than the capacitor voltage  $V_c$ , control can be performed to always make the virtual DC link voltage  $V_{dc}$  greater than the rectified voltage  $V_{rec}$ . In this case,  $dc > 0$  always holds, and Step S106  
25 is performed in no case as shown in the flowchart of FIG. 5. Needless to say, since

Expression (1) holds,  $d_r < 1$ .

[0159] Examples 1 and 2 reveal that the virtual DC link voltage  $V_{dc}$  can be set to be greater than or equal to  $1/\sqrt{2}$  times the crest value of the rectified voltage  $V_{rec}$ .

[0160] In particular, Example 2 reveals that the waveform of the rectified current  $i_{rec}$  can be the absolute value of a sinusoidal wave. This contributes to the restriction of the power line harmonics.

[0161] Example 3

As described in Example 1, when the virtual DC link voltage  $V_{dc}$  is greater than the rectified voltage  $V_{rec}$ , there is a "charge and discharge" period during which  $dz =$   
 10 0. The voltage  $V_{inv}$  output from the inverter 6 during this period is not a DC voltage but an AC voltage. When the virtual DC link voltage  $V_{dc}$  takes a constant value, therefore, the inverter 6 operates with a zero voltage vector for the voltage  $V_{inv}$  to be AC if  $dz = 0$ .

[0162] This means that the virtual DC link voltage  $V_{dc}$  is excessive with respect to the  
 15 voltage  $V_{inv}$ , and the capacitor 34 is charged and discharged unnecessarily.

[0163] Description will now be given of the virtual DC link voltage  $V_{dc}$  for reducing the unnecessary charge and discharge of the capacitor 34 and reducing the power capacity of the boost chopper 3.

[0164] Both FIGs. 10 and 11 show, in an upper tier, command values  $V_u^*$ ,  $V_v^*$ , and  
 20  $V_w^*$  of three phases as the command value  $V_{inv}^*$  of the inverter 6 and the virtual DC link voltage  $V_{dc}$  and show, in a lower tier, line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  obtained by the inverter 6 outputting the voltage  $V_{inv}$  based on the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$ . In the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$ , a minimum-phase voltage (minimum value) of them is zero. The horizontal axis common to FIGs. 10 and 11 is the  
 25 phase of the AC voltage  $V_{in}$ , and illustrated herein is the case in which the cycle of the

AC voltage  $V_{in}$  is twice the cycles of the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$ .

[0165] FIG. 10 shows the case in which the virtual DC link voltage  $V_{dc}$  takes a constant value. The constant value is a maximum value that the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  can take with respect to a minimum-phase voltage of the command values of three phases (hereinbelow, this value is a value  $V_2$ ).

[0166] It is revealed that with a phase of  $(15 + 30 \cdot n)$  degrees ( $n$  is an integer) and therearound, the virtual DC link voltage  $V_{dc}$  is greater than the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  and is thus a value greater than or equal to a voltage required for the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$ . In such a case, even when  $dz = 0$ , the inverter 6 adopts the zero voltage vector in order to output a voltage lower than the virtual DC link voltage  $V_{dc}$ .

[0167] That is to say, at a phase of  $(15 + 30 \cdot n)$  degrees ( $n$  is an integer) and therearound, the virtual DC link voltage  $V_{dc}$  is set to be unnecessarily high in view of the operation of the inverter 6. This results in unnecessary discharge for obtaining such an unnecessarily high virtual DC link voltage  $V_{dc}$ .

[0168] When the command value  $V_{dc}^*$  of the virtual DC link voltage  $V_{dc}$  is set without being unnecessarily increased with respect to the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$ , an unnecessary discharge of the capacitor 34 is reduced, and accordingly, an unnecessary charge of the capacitor 34 is reduced.

[0169] This will be described with reference to the flowchart of FIG. 5. Since an improvement in the case in which  $dz = 0$  is considered here, Step S103 that leads to Step S107 of setting  $dz = 0$  is considered. Normally,  $V_c > V_{rec}$  and  $V_c > V_{dc}^*$ , and thus,  $dr\_max$  becomes greater as the command value  $V_{dc}^*$  is smaller. As the command value  $V_{dc}^*$  is smaller, thus, the rectifying duty  $dr$  set in Step S107 is greater and the discharge duty  $dc$  is smaller. Since the capacitor voltage  $V_c$  can be considered to be constant, a

smaller discharge duty means a smaller current  $i_c$ .

[0170] Further, Step S109 processed after Step S107 will also be considered. As described above, the rectifying duty  $d_r$  becomes greater as the command value  $V_{dc}^*$  is smaller. The output power  $P_{out}$  is made constant, and accordingly, the pulsation of the command value  $V_{dc}^*$  causes the DC current  $i_{dc}$  to pulsate. Specifically, the DC current  $i_{dc}$  becomes greater as the command value  $V_{dc}^*$  is smaller. Thus, both the rectifying duty  $d_r$  and the DC current  $i_{dc}$  are greater as the command value  $V_{dc}^*$  is smaller, and the rectified current  $i_{rec}$  does not depend on the command value  $V_{dc}^*$  as a sinusoidal wave, and accordingly, the current  $i_b$  is small.

[0171] Such reductions in the currents  $i_b$  and  $i_c$  contribute to a reduction in the power capacities required for the inductor 32 and the capacitor 34, and accordingly, miniaturization of the inductor 32 and the capacitor 34, cost reduction, and an improvement in efficiency owing to a reduced calorific value, and further contribute to a reduction in the power capacity required for the boost chopper 3.

[0172] Specifically, the command value  $V_{dc}^*$  may be the greatest command value among the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  with respect to a minimum phase. This is because while the inverter 6 cannot output a large voltage exceeding the virtual DC link voltage  $V_{dc}$ , it suffices that the virtual DC link voltage  $V_{dc}$  is the greatest command value among the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  with respect to a minimum phase.

[0173] That is to say, the command value  $V_{dc}^*$  may have  $V_1 = \max(V_u^*, V_v^*, V_w^*) - \min(V_u^*, V_v^*, V_w^*)$ , where a symbol " $\max()$ " represents the greatest one among the elements within a parenthesis, and a symbol " $\min()$ " represents the smallest one among the elements within a parenthesis.

[0174] Under normal control, phase voltages  $V_u$ ,  $V_v$ , and  $V_w$  output from the inverter 6 respectively match the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$ , and thus, the value  $V_1$  can be obtained

as  $V1 = \max(V_u, V_v, V_w) - \min(V_u, V_v, V_w)$ . This can be obtained as  $V1 = \max(|V_{uv}|, |V_{vw}|, |V_{wu}|)$  using line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$ .

[0175] Similarly, the value  $V2$  can be obtained as a maximum value that the phase voltages  $V_u$ ,  $V_v$ , and  $V_w$  output from the inverter 6 can take with respect to a minimum phase among them. This means that the value  $V2$  can be obtained as a maximum value that the respective absolute values  $|V_{uv}|$ ,  $|V_{vw}|$ , and  $|V_{wu}|$  of the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  can take.

[0176] FIG. 11 illustrates a case in which the command value  $V_{dc}^*$  takes the value  $V1$ . Also in this case, the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  can take the same values as those of FIG. 10, and thus, the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  also do not differ between FIGs. 10 and 11.

[0177] Needless to say, the command value  $V_{dc}^*$  may take a value greater than the value  $V1$ . In the case shown in FIG. 10, the command value  $V_{dc}^*$  takes the value  $V2$  greater than the value  $V1$ , and thus, it suffices that  $V1 \leq V_{dc}^* \leq V2$ .

[0178] More accurately, it is desirable that  $V_{dc}^* = V2$  at a phase (with reference to FIGs. 10 and 11,  $(30 \cdot n)$  degrees) at which the command values  $V_u^*$ ,  $V_v^*$ , and  $V_w^*$  are maximum with respect to a minimum phase and that  $V1 \leq V_{dc}^* < V2$  at the other phases.

[0179] The command value  $V_{dc}^*$  can be set as described above in the virtual DC link voltage command value generator 98 shown in FIG. 4.

[0180] FIG. 12 shows waveforms of the specifications corresponding to FIG. 8 in Example 3. FIG. 13 shows the specifications corresponding to FIG. 9 and waveforms of line-to-line voltages. For brevity of the drawings, the cycles of the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  are set to a half of the cycle of the AC voltage  $V_{in}$ , and the amplitudes of the line-to-line voltages  $V_{uv}$ ,  $V_{vw}$ , and  $V_{wu}$  are set to be equal to the amplitude of the AC voltage  $V_{in}$ .

[0181] It is revealed that while the DC current  $i_{dc}$  fluctuates correspondingly to the variation of the command value  $V_{dc}^*$ , the waveform of the rectified current  $i_{rec}$  can take an absolute value of a sinusoidal wave. As described with reference to FIG. 5, the currents  $i_b$  and  $i_c$  also reduce at phases at which the command value  $V_{dc}^*$  reduces.

5 [0182] FIG. 14 is a graph in which the current  $i_b$  is compared between Examples 2 and 3. The current  $i_b$  in Example 2 is indicated by the current  $i_{b1}$ , and the current  $i_b$  in Example 3 is indicated by the current  $i_{b2}$ . It is understood that the current  $i_{b2}$  is always smaller than or equal to the current  $i_{b1}$  and that the effective value and the average value of the current  $i_{b2}$  are smaller than the effective value and the average value of the current  
10  $i_{b1}$ .

[0183] FIG. 15 is a graph in which the current  $i_c$  is compared between Examples 2 and 3. The current  $i_c$  in Example 2 is indicated by the current  $i_{c1}$ , and the current  $i_c$  in Example 3 is indicated by the current  $i_{c2}$ . It is understood that the current  $i_{c2}$  is always smaller than or equal to the current  $i_{c1}$  and that the effective value and the average value  
15 of the current  $i_{c2}$  are smaller than the effective value and the average value of the current  $i_{c1}$ .

[0184] It is revealed that both the currents  $i_{b2}$  and  $i_{c2}$  reduce at a phase  $(15 + 30 \cdot n)$  degrees at which the command value  $V_{dc}^*$  reduces and therearound.

[0185] Next, the operation of the inverter 6 in the period in which  $d_z = 0$  will be  
20 described.

[0186] FIGs. 16 and 17 are graphs showing a carrier  $CY$  and a signal wave to be compared with the carrier  $CY$ , an operation of the switch  $G_c$ , a DC current  $i_{dc}$  and an instantaneous value  $V_{link}$  between DC link voltages, an output power  $P_{out}$ , and switching states of respective phases that will be described below. Herein, a minimum  
25 value of the carrier  $CY$  is 0, and a maximum value of the carrier  $CY$  is 1. Values  $du^*$ ,

$dv^*$ , and  $dw^*$  are adopted to generate a signal wave and are set based on the command values  $Vu^*$ ,  $Vv^*$ , and  $Vw^*$  of the inverter 6 by the known technique. Specifically,  $du^* = Vu^*/V_{dc}^*$ ,  $dv^* = Vv^*/V_{dc}^*$ , and  $dw^* = Vw^*/V_{dc}^*$ .

[0187] Both FIGs. 16 and 17 show an operation in areas in which a U-phase voltage output from the inverter 6 is a minimum phase, a W-phase voltage output from the inverter 6 is a maximum phase,  $Vu^* < Vv^* < Vw^*$  holds, and none of the command values  $Vv^*$  and  $Vw^*$  peaks (zones of 135 degrees or more and less than 150 degrees, more than 150 degrees and 165 degrees or less, 315 degrees or more and less than 330, and more than 330 degrees and 345 degrees or less in terms of phases: see FIG. 10). In such a case,  $Vu^* = 0$ , and  $dz = 0$  (see also FIG. 12).

[0188] A period  $t_c$  is a period in which the switch  $G_c$  turns on. In the period  $t_c$ , accordingly, the capacitor 34 is discharged, the instantaneous value  $V_{link}$  is the capacitor voltage  $V_c$ , and the electric power  $P_{co}$  provides the output power  $P_{out}$ . A period  $t_r$  is a period in which the switch  $G_c$  turns off. In the period  $t_r$ , accordingly, the instantaneous value  $V_{link}$  provides the rectified voltage  $V_{rec}$ , and the electric power  $P_{direct}$  is the output power  $P_{out}$ .

[0189] The control signal  $S_g$  is determined through the comparison between the carrier  $CY$  and the signal wave, and accordingly, the switching operation of the inverter 6 is determined. Specifically, for example, the inverter 6 is a three-phase voltage-source inverter and has a current path (leg) per phase. Each leg has a series connection between an upper arm and a lower arm, and switches are used as the upper arm and the lower arm that are conductive exclusively (see FIG. 1).

[0190] More specifically, in the U-phase leg, the upper arm is conductive and the lower arm is not conductive when the carrier  $CY$  is smaller than or equal to the signal wave  $dr \cdot du^*$  or is greater than or equal to the signal wave  $dr + dc \cdot (1 - du^*)$ . In the other case, the

lower arm is conductive and the upper arm is not conductive. The same applies to the V-phase leg and the W-phase leg.

[0191] Such a control signal  $S_g$  that determines conductivity/non-conductivity is generated in the pulse width modulation signal generator 94. The carrier  $CY$  is  
5 generated in, for example, the pulse width modulation signal generator 94.

[0192] The lowest three rows of each of FIGs. 16 and 17 indicate the switching states in the U-phase, the V-phase, and the W-phase of the inverter 6. In these three lines, a symbol "H" indicates the state in which the upper arm is conductive and the lower arm is not conductive, and a symbol "L" indicates the state in which the lower arm is conductive  
10 and the upper arm is not conductive.

[0193] In the areas of the phases described above,  $V_u^* = 0$  and signal wave  $dr \cdot du^* = 0$ ,  $dr + dc \cdot (1 - du^*) = 1$  ( $\therefore dz = 0$ ), and thus, the case in which the lower arm is kept conductive is illustrated for the U-phase. That is to say, switching does not occur at the U-phase leg in this area.

15 [0194] In such a case, when  $V_{dc}^* > V_w^*$  as shown in FIG. 10, as shown in FIG. 16, a signal wave has a relationship  $dr + dc \cdot (1 - dw^*) < dr < dr \cdot dw^*$ , where  $dz = 0$  is taken into consideration. This results in the presence of a zone  $t_0$  with a width corresponding to a difference  $(1 - dw^*)$  between the command values  $dr + dc \cdot (1 - dw^*)$  and  $dr \cdot dw^*$ . The zone  $t_0$  is a period in which although  $dz = 0$ , the inverter 6 adopts a zero voltage  
20 vector.

[0195] In the zone  $t_0$ , the inverter 6 adopts the zero voltage vector, so that the DC current  $i_{dc}$  is 0 and the instantaneous value of the output power  $P_{out}$  is also 0. Nevertheless, the zone  $t_0$  includes a period in which the switch  $G_c$  is conductive and the instantaneous value  $V_{link}$  increases, and a discharge of the capacitor 34 during this period  
25 is an unnecessary discharge in view of the operation of the inverter 6.

[0196] When the command values are equal between the case shown in FIG. 16 and the case shown in FIG. 17, a period in which the instantaneous value  $V_{link}$  takes the capacitor voltage  $V_c$  is shortened by setting  $V_{dc}^* = V_w^*$  as shown in FIG. 11. That is to say, the period  $t_c$  is shortened. This results from a reduction in the discharge duty  $d_c$  described above.

[0197] Setting  $V_{dc}^* = V_w^*$ , the upper arm is always conductive in the W-phase leg in the area of the phase described above. That is to say, no switching operation is required in the W-phase leg, that is, not only switching based on a minimum one (herein, command value  $V_u^*$ ) among the command values is not required, but also switching based on a maximum one (herein, command value  $V_w^*$ ) among the command values is not required. Unlike FIG. 16, there is accordingly no zone  $t_0$  as shown in FIG. 17.

[0198] Since  $dz = 0$ , a shorter period  $t_c$  results in a longer period  $t_r$ , a greater output power  $P_{out}$  (that is to say, electric power  $P_{direct}$ ) in the period  $t_r$ , and a smaller output power  $P_{out}$  (that is to say, electric power  $P_{co}$ ) in the period  $t_c$ . The average of the output power  $P_{out}$ , however, can be maintained even when the command value  $V_{dc}^*$  is reduced.

[0199] The effect of reducing the period  $t_c$  for a reduced period  $t_r$  is obtained by reducing the duration of a zone  $t_0$  even in the presence of such a zone  $t_0$ . The effect is thus obtained if  $V_{dc}^* = V_1$  ( $V_w^*$  in the example above) does not always hold.

[0200] Through setting of the command value  $V_{dc}^*$  to be greater than or equal to the value  $V_1$  and smaller than or equal to the value  $V_2$ , the discharge duty  $d_c$  can be reduced, the currents  $i_c$  and  $i_b$  can be reduced, and the power capacities required for the boost chopper and the capacitor 34 and the inductor 32, which are components of the boost chopper, can be reduced while the output voltage from the direct AC power converter is increased more than in the conventional case. The virtual DC link voltage  $V_{dc}$  takes the

command value  $V_{dc}^*$  in the normal control, and thus, the effect described above can be obtained when the virtual DC link voltage  $V_{dc}$  is greater than or equal to the value  $V1$  and smaller than or equal to the value  $V2$ .

[0201] In particular, setting the command value  $V_{dc}^*$  to the value  $V1$  eliminates the  
5 need for the switching operations of two phases among the legs of the three phases of the inverter 6. This is desirable not only in that the generation of a control signal  $S_g$  for substantially two phases is omitted but also in that a switching loss of the inverter 6 is reduced.

[0202] Needless to say, even when the command value  $V_{dc}^*$  is not always set to the  
10 value  $V1$ , a switching loss of the inverter 6 is reduced during a period during which the command value  $V_{dc}^*$  is set to the value  $V1$ . In other words, the presence of the period during which the command value  $V_{dc}^*$  is set to the value  $V1$  contributes to a reduction in the switching loss of the inverter 6.

[0203] The virtual DC link voltage  $V_{dc}$  takes the command value  $V_{dc}^*$  in normal  
15 control. Therefore, the presence of the period during which the virtual DC link voltage  $V_{dc}$  takes the value  $V1$  reduces a switching loss of the inverter 6.

[0204] While the invention has been shown and described in detail, the foregoing  
description is in all aspects illustrative and not restrictive. It is therefore understood that  
numerous modifications and variations can be devised without departing from the scope  
20 of the invention.

## CLAIMS

1. A direct AC power converter comprising:

a DC link having

5 a first power supply line, and

a second power supply line to which a potential lower than a potential  
of said first power supply line is applied;

a first rectifying circuit having

a plurality of input terminals that receive an input of an AC voltage,

10 and

a pair of output terminals each connected to said DC link;

an inverter that converts a voltage applied to said DC link into another  
multi-phase AC voltage;

a boost chopper having a capacitor in an output stage thereof; and

15 a switch that switches a discharge and non-discharge from said capacitor to said  
DC link,

wherein

in said boost chopper, said capacitor is charged at least during a first period  
being a part of a period during which a discharge duty is greater than 0, said discharge  
20 duty being a time ratio at which said switch is conductive,

a virtual DC link voltage is greater than or equal to a first value and smaller  
than or equal to a second value, said virtual DC link voltage being expressed as a sum of a  
product of said discharge duty and a voltage between both ends of said capacitor and a  
product of a rectifying duty and a rectified voltage of said AC voltage,

25 said rectifying duty takes a value obtained by subtracting a sum of said

discharge duty and a zero voltage duty from 1,

said zero voltage duty is a time ratio at which said inverter adopts a zero voltage vector irrespective of magnitude of a voltage output from said inverter,

said first value is a maximum value among absolute values of respective  
 5 line-to-line voltages of said multi-phase AC voltage,

said second value is a maximum value that said absolute values are capable of taking, and

said rectified voltage is applied to an input side of said boost chopper.

10 2. The direct AC power converter according to claim 1, further comprising

a second rectifying circuit that inputs said rectified voltage to said boost chopper.

3. A direct AC power converter, comprising:

15 a DC link having

a first power supply line, and

a second power supply line to which a potential lower than a potential of said first power supply line is applied;

a first rectifying circuit having

20 a plurality of input terminals that receive an input of an AC voltage,  
 and

a pair of output terminals each connected to said DC link;

an inverter that converts a voltage applied to said DC link into another multi-phase AC voltage;

25 a boost chopper having a capacitor in an output stage thereof; and

a switch that switches a discharge and non-discharge from said capacitor to said DC link,

wherein

in said boost chopper, said capacitor is charged at least during a first period being a part of a period during which a discharge duty is greater than 0, said discharge duty being a time ratio at which said switch is conductive,

5           a virtual DC link voltage is greater than or equal to a first value and smaller than or equal to a second value, said virtual DC link voltage being expressed as a sum of a product of said discharge duty and a voltage between both ends of said capacitor and a product of a rectifying duty and a rectified voltage of said AC voltage,

10           said rectifying duty takes a value obtained by subtracting a sum of said discharge duty and a zero voltage duty from 1,

          said zero voltage duty is a time ratio at which said inverter adopts a zero voltage vector irrespective of magnitude of a voltage output from said inverter,

          said first value is a maximum value among absolute values of respective line-to-line voltages of said multi-phase AC voltage,

15           said second value is a maximum value that said absolute values are capable of taking,

          said pair of output terminals of said first rectifying circuit are connected to an input side of said boost chopper.

20           4. The direct AC power converter according to any one of preceding claims, wherein said capacitor is charged in said boost chopper during said first period and a part or whole of a period at which said discharge duty is 0.

          5. The direct AC power converter according to any one of preceding claim, wherein

25           said capacitor is charged with a charge power and discharged with a discharge power during said first period, and

          said first period has a period during which said charge power is greater than said discharge power and a period during which said discharge power is greater than said charge power.

6. The direct AC power converter according to any one of preceding claims ,  
wherein a period during which said virtual DC link voltage takes said first value is  
present.

7. The direct AC power converter according to any one of preceding claim,  
5 wherein said discharge duty at which said zero voltage duty is minimum is set based

on a command value of a rectified current being a sum of a current flowing in said boost chopper and a current flowing from said first rectifying circuit to said inverter, a command value of said virtual DC link voltage, a voltage between both ends of said capacitor, said rectified voltage, and a current input to said inverter.

5

8. The direct AC power converter according to claim 7, wherein

when said virtual DC link voltage is greater than said rectified voltage and said command value of said rectified current is greater than or equal to a product of a  
10 predetermined value and a current input to said inverter, said rectifying duty takes said predetermined value, and said discharge duty takes a value obtained by subtracting said predetermined value from 1, and

said predetermined value is a value obtained by dividing a value obtained by subtracting said voltage between both ends of said capacitor from said command value of  
15 said virtual DC link voltage by a value obtained by subtracting said voltage between both ends from said rectified voltage.

9. The direct AC power converter according to claim 1 or any one of claims 3 and 5 to 8, wherein said discharge duty is always positive.

10. The direct AC power converter according to any one of claims 1 to 9,  
5 further comprising

a diode connected in parallel with said switch, a forward direction of said diode is a direction in which said capacitor is charged from said DC link.