

Description

Background of the Invention

5 The present invention relates, in general, to the field of data processors and methods. More particularly, the present invention relates to an output compare system and method for automatically controlling multiple outputs in a microprocessor (MPU) or microcomputer (MCU) in which a single output compare function may directly control multiple output pins by means of mask and data registers.

10 By "output compare" is meant the provision of an output signal upon the occurrence of a comparison signal indicating that two values are equal. In former MPU and MCU systems, there have been provided output compare functions to generate a timed output signal from the device. See for example Electronic Design, May 24, 1980 pages 75-81. Such output signals could be used to either (1) set the output, (2) clear the output, (3) toggle the output, or (4) indicate no change to the output. In certain prior art MCU devices, such as the MC6801 available from Motorola, Inc., assignee of the present invention, there was only one
15 output compare function provided. In the MC6801U4, likewise available from Motorola, Inc., three output compare functions were provided each of which operated as a separate independent entity. In this latter instance, were an output pin not being used for a compare function, control of that pin could not be picked up by one of the other output compare functions. Such a system is disclosed in US-A-4,161,787.

20 With such independent prior art output compare functions, the best pulse width available on a given output compare pin was on the order of approximately 30 MCU cycles. This relatively long pulse width is due to the fact that after an output compare occurred on a given pin, an interrupt routine would be executed to write a new higher value to the compare register. Because of this, it was not possible to achieve a one-MCU-cycle wide pulse positioned with one cycle resolution.

25 Certain other prior art devices, such as the Intel 8096, utilize a content addressable memory. Such content addressable memories are similar to the above-described output compare registers except that they have a circular FIFO configuration in which a value placed therein is sequentially compared against each one of the compare registers in the device to a timer count. Upon achieving a match with the compare register and timer count, a command word associated with the compare value generates an appropriate output signal. By use of this circular FIFO system, the device can set several of its compare registers to the
30 same value and utilize the appropriate command word to cause an action on separate pins so that several of the device pins can change state during the same cycle. However, in utilizing a system of this sort, more than one compare register must be utilized. Still further, such a system is not efficient in effectuating a one-cycle pulse width nor allowing the utilization of any unused output pins on the timer port as timed output pins controlled by a separate output compare register.

35 It is therefore an object of the present invention to provide an improved timer system according to claim 1 and method according to claim 3.

The foregoing object is achieved in the present invention wherein there is provided a timer system comprising:

- 40 a first counter for counting pulses of a first input signal;
- a first compare register for selectively storing a first compare value therein;
- a first comparator, coupled to the output of the first counter and to the output of the first compare register, for comparing the first counter value to the first compare value, and for providing a first compare signal when said values are the same;
- characterised by a data register for selectively storing first and second data bits therein;
- 45 a mask register for selectively storing first and second mask bits therein; and
- logic means connected to said first comparator to receive the first compare signal, for providing a first output signal on a first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a first predetermined state, and to provide a second output signal on a second timer output pin indicative of the state of the second data bit in response to the first
50 compare signal only if the second mask bit is in a predetermined state, whereby the first compare signal is capable of causing output signals to be provided via more than one timer output pin under control of the mask register.

Brief Description of the Drawings

55 The present invention will become more apparent and will be best understood by reference to the following description of an embodiment of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified timing diagram illustrative of the programming necessary to implement the output compare function and software instructions to a prior art microcomputer; and
 FIG. 2 is a simplified logic flow diagram of a data processor system in accordance with the present invention for automatically controlling multiple outputs by means of mask and data registers used in conjunction with an output compare function.

Description of a Preferred Embodiment

With reference to FIG. 1, the timing involved in an instruction sequence in a software implementation of an immediate output compare function in a prior art microcomputer, such as an MC6801 available from Motorola, Inc., assignee of the present invention, is shown. The following three instructions were used to generate an immediate output compare:

```
LDD $9 /GET COUNTER REGISTER VALUE
ADDD #10 /ADD AN OFFSET
STD $B /UPDATE OUTPUT COMPARE
```

If it were undesirable to disturb the A accumulator, the following four-instruction sequence could also be used:

```
LDAB #9 /COUNTER OFFSET TO ACCB
LDX $9 /READ COUNTER REGISTER
ABX /ADD OFFSET
STX $B /UPDATE OUTPUT COMPARE
```

In either instance, valuable program space was necessary to force an output compare function in addition to the latency to the desired output action attendant the program execution.

With reference now to FIG. 2, a simplified logic flow diagram of a data processor system in accordance with the present invention for implementation of an output compare function by means of an output compare register 10 or timer compare force register (CFORC) 22 is shown. This portion of the data processor system is the subject matter of United States Patent Application No. SC05067A filed concurrently herewith by James M. Sibigtroth and assigned to the assignee of the present invention. Timing input to the system is supplied from the data processor E clock for input through prescaler 20 to 16-bit free running counter 12. Prescaler 20 and free running counter 12 are the subject matter of United States patent application number SC05060 filed on November 2, 1983 by James M. Sibigtroth and David Rivera and assigned to the assignee of the present invention.

Output from free running counter 12 is applied as input to output compare registers 10 by means of a 16-bit timer bus. The output of output compare registers 10 is supplied through timer interrupt flag register (TFLG 1) 14 for input to a like number of OR gates 30. An additional input to OR gates 30 is supplied from the output of timer compare force register (CFORC) 22. Output of main timer interrupt mask register 1 (TMSK 1) 28 in conjunction with the output of timer interrupt flag register 14 supply interrupt requests through a like number of AND gates 32.

The output of OR gates 30 corresponding to output compares 2, 3, 4 and 5 are supplied as input to TCTL 1 control register 16. The output of OR gate 30 corresponding to an output compare 1 function is supplied directly to output compare 1 mask register (OC1M) 24 and output compare 1 data register (OC1D) 26. As shown, the output of TCTL 1 control register 16 is likewise applied to output compare pin logic comprising output compare 1 mask register (OC1M) 24 and output compare 1 data register (OC1D) 26, the output of which is applied to port A 18.

Normal Output Compare Functions

The Output Compare Registers 10 are 16-bit read/write registers which are initialized to SFFFF by Reset and can be used for several purposes. Two possible applications include controlling an output waveform and indicating when a period of time has elapsed. The five Output Compare Registers 10 are

unique in that all bits are readable and writable and are not altered by the timer hardware (except during Reset). If an output compare function is not utilized, the unused registers may be used simply as storage locations.

All Output Compare Registers 10 have a separate dedicated comparator for comparing against the free running counter 12. If a match is found, the corresponding Output Compare flag (OCxF) bit is set in the Timer Interrupt Flag Register 14 and a specified action is automatically taken. For output compare functions 2 thru 5 the automatic action is controlled by pairs of bits in the TCTL1 control register 16. Each pair of control bits is encoded to specify the output action to be taken as a result of a successful OCx compare. Output compare functions 2 thru 5 are always associated with Port A 18 bits 6 thru 3 respectively.

OMx	OLx	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

In some cases the values in the Output Compare Register 10 and the output action control bits must be changed after each successful comparison to control an output waveform or establish a new elapsed timeout.

An interrupt can also accompany a successful output compare provided that the corresponding interrupt enable bit (OCx1) is set.

Due to the prescaler 20, the counter may not change value on each cycle of the E-clock and the comparison may be true for several consecutive E-cycles. In order to avoid multiple output actions, the output action is only permitted to occur during the E-low time immediately following the cycle where the match first became true.

After an MPU write cycle to the register most significant byte, the output compare function is inhibited for one E-cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double byte write instruction should be used in order to take advantage of the compare inhibit feature.

MPU writes can be made to either byte of the Output Compare Register 10 without affecting the other byte. When a compare occurs, the output action is taken regardless of whether or not the Output Compare Flag (OCxF) of Timer Interrupt Flag Register 14 was previously set.

In the MC6801 timer system, the only way to force a timer compare action was to write a 16-bit value slightly larger than the present counter value into the output compare register 10. This was a cumbersome procedure so the present invention includes a write only register to allow forced compares. Five of the bit positions in the CFORC register 22 correspond to the five output compare functions. To force a compare or compares a write is done to CFORC register 22 with the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there were a match between the OCx register and the free running counter 12 except the corresponding interrupt flag status bits of Timer Interrupt Flag Register 14 are not set.

Unlike the other four compare functions Output Compare 1 can automatically affect any or all of the five output pins (bits 3-7) in Port A 18 as a result of a successful compare between the OC1 register and the 16-bit free running counter 12. Two 5-bit registers are used in conjunction with this function, the Output Compare 1 Mask register (OC1M) 24 and the Output Compare 1 Data register (OC1D) 26.

OC1M 24 is used to specify the bits of Port A 18 (I/O and Timer Port) which are to be affected as a result of a successful OC1 compare. The bits of OC1M 24 correspond bit-for-bit with the bits of Port A 18 (bits 3-7). For each bit that is to be affected by the successful compare, the corresponding bit in OC1M 24 should be set to one. OC1D 26 is used to specify the data which is to be stored to the affected bits of Port A 18 as the result of a successful OC1 compare. The bits of OC1D 26 correspond bit-for-bit with the bits of Port A 18 (bits 3-7). When a successful OC1 compare occurs, for each bit that is set in OC1M 24, the corresponding data bit in OC1D 26 is stored to the corresponding bit of Port A 18. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E-cycle, and both attempt to alter the same Port A 18 bit, the OC1 action will override.

One reason this function is provided is to allow control of multiple I/O pins automatically with a single output compare function. In a case where the output compare 2 and the output compare 3 functions were being used for internal timing functions, the associated Port A 18 pins would be free to use for other purposes. These two pins can be controlled simultaneously as high speed timed outputs using the output

compare 1 function. For the two bits which are to be affected, the corresponding bits in the OC1M 24 register would be set to one. Since the OC1M 24 bits corresponding to the other Port A 18 pins would be zero a successful compare with OC1 would not affect any of those pins.

Another intended use for the special I/O pin control on the output compare 1 function is to allow more than one output compare function to control a single I/O pin. In a case where the output compare 1 function is configured to affect only bit-3 of Port A 18 (by setting OC1M 24 = S08), both output compare 1 and output compare 5 are associated with the same Port A 18 bit. The OC5 function can set Port A 18 bit-3 high and the OC1 function can set it low on the very next count of the free running counter 12. This will permit shorter duration pulses than were previously possible.

CFORC Timer Compare Force Register 22

The Compare Force (CFORC) Register 22 is used to force early Output Compare actions. A shortcoming of the previous output compare operation was the difficulty in forcing an output compare action which involved reading the Timer Count Register, adding a constant, and writing to the Output Compare Register 10. The CFORC register 22 is an 8-bit write only register except that bits 2, 1, and 0 are not implemented. Reads of this location have no meaning or effect and always return logic zeros (S00). The following Table 1 and paragraphs describe the function of each of the bits.

B7	B6	B5	B4	B3	B2	B1	B0
FOC1	FOC2	FOC3	FOC4	FOC5	-	-	-

Table 1: Timer Compare Force Register (CFORC) 22

Bit-7 FOC1 - Force Output Compare 1 Action

Reads of this bit have no meaning and will always return a logic zero value. A write to this bit with the corresponding data bit clear has no effect on the system. A write to this bit with the corresponding data bit set causes the action which is programmed for output compare 1 to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OC1 register except the OC1 interrupt flag of Timer Interrupt Flag Register 14 does not get set.

Bit-6 FOC2 - Force Output Compare 2 Action

Reads of this bit have no meaning and will always return a logic zero value. A write to this bit with the corresponding data bit clear has no effect on the system. A write to this bit with the corresponding data bit set causes the action which is programmed for output compare 2 to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OC2 register except the OC2 interrupt flag of Timer Interrupt Flag Register 14 does not get set. This function is not recommended when using the toggle output feature of OC2.

Bit-5 FOC3 - Force Output Compare 3 Action

Reads of this bit have no meaning and will always return a logic zero value. A write to this bit with the corresponding data bit clear has no effect on the system. A write to this bit with the corresponding data bit set causes the action which is programmed for output compare 3 to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OC3 register except the OC3 interrupt flag of Timer Interrupt Flag Register 14 does not get set. This function is not recommended when using the toggle output feature of OC3.

Bit-4 FOC4 - Force Output Compare 4 Action

Reads of this bit have no meaning and will always return a logic zero value. A write to this bit with the

corresponding data bit clear has no effect on the system. A write to this bit with the corresponding data bit set causes the action which is programmed for output compare 4 to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OC4 register except the OC4 interrupt flag of Timer Interrupt Flag Register 14 does not get set. This function is not recommended when using the toggle output feature of OC4.

Bit-3 FOC 5 - Force Output Compare 5 Action

Reads of this bit have no meaning and will always return a logic zero value. A write to this bit with the corresponding data bit clear has no effect on the system. A write to this bit with the corresponding data bit set causes the action which is programmed for output compare 5 to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OC5 register except the OC5 interrupt flag of Timer Interrupt Flag Register 14 does not get set. This function is not recommended when using the toggle output feature of OC5.

Bit-2 not implemented

This bit is not implemented and writes have no meaning or effect on it. Reads of this bit will always return a logic zero value.

Bit-1 not implemented

This bit is not implemented and writes have no meaning or effect on it. Reads of this bit will always return a logic zero value.

Bit-0 not implemented

This bit is not implemented and writes have no meaning or effect on it. Reads of this bit will always return a logic zero value.

OC1M Output Compare 1 Mask Register 24

This 8-bit read/write register is cleared by reset and is used in conjunction with the Output Compare 1 function to specify the bits of Port A 18 (I/O and Timer Port) which are to be affected as a result of a successful OC1 compare. The following Table 2 and paragraphs describe the function of each of the bits.

B7	B6	B5	B4	B3	B2	B1	B0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	-	-	-

Table 2: Output Compare 1 Mask Register (OC1M) 24

The bits of OC1M correspond bit-for-bit with the bits of Port A 18 (bits 7 thru 3 only). For each bit that is to be affected by the successful compare, the corresponding bit in OC1M 24 should be set to one.

OC1D Output Compare 1 Data Register 26

This 8-bit read/write register is used in conjunction with the Output Compare 1 function to specify the data which is to be stored to the affected bits of Port A 18 as the result of a successful OC1 compare. This register is not affected by reset. The following Table 3 and paragraphs describe the function of each of the bits.

B7	B6	B5	B4	B3	B2	B1	B0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	-	-	-

Table 3: Output Compare 1 Data Register (OC1D) 26

The bits of OC1D 26 correspond bit-for-bit with the bits of Port A 18 (bits 7 thru 3 only). When a successful OC1 compare occurs, for each bit that is set in OC1M 24, the corresponding data bit in OC1D 26 is stored to the corresponding bit of Port A 18. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E-cycle, and both attempt to alter the same Port A 18 bit, the OC1 action will override.

TCNT 16-bit Timer Count Register

The key element in the timer system is a 16-bit free running counter 12, or Timer Counter Register, with its associated prescaler 20. The timer counter is incremented to higher values each time the prescaler 20 times out (rollover from SFFFF to S0000 is permitted). Software can read the counter 12 at any time without affecting its value because the counter 12 is clocked and read during opposite half cycles of the MPU E-cycle clock.

A full counter 12 read should first address the most significant byte. An MPU read of this address causes the least significant byte to be latched into a buffer for the next CPU cycle so that a double byte read will return the full 16-bit state of the counter 12 at the time of the most significant byte read cycle. For double byte read instructions, these two accesses occur on consecutive bus cycles. This buffer is normally transparent and is accessed when reading the counter 12 least significant byte.

Because its width is 16 bits, the value in the free running counter 12 repeats every 65,536 counts (prescaler 20 timeouts). When the count changes from SFFFF to S0000 the Timer Overflow Flag (TOF) bit is set. An interrupt can also be enabled when counter overflow occurs by setting its interrupt enable bit, TOI.

TOC1 Timer Output Compare 1 Register

The Output Compare Registers 10 are 16-bit read/write registers that are initialized to SFFFF during reset and are used to control timer output events. After an MPU write to the register most significant byte, the output compare function is inhibited for one E-clock cycle in order to allow both bytes of the 16-bit register to be written before the next comparison is made. If both bytes of the register are to be changed, a double byte write instruction should be used in order to take advantage of this inhibit feature. Either byte may be written separately without affecting the other byte and timer hardware does not affect these registers except during reset so registers associated with unused timer functions may be used as normal RAM type locations. The timer Output Compare 1 function uses the OC1M 24 and OC1D 26 registers to directly control up to five Port A 18 I/O pins as previously described.

TOC2 Timer Output Compare 2 Register

The Output Compare Registers 10 are 16-bit read/write registers that are initialized to SFFFF during reset and are used to control timer output events. After an MPU write to the register most significant byte, the output compare function is inhibited for one E-clock cycle in order to allow both bytes of the 16-bit register to be written before the next comparison is made. If both bytes of the register are to be changed, a double byte write instruction should be used in order to take advantage of this inhibit feature. Either byte may be written separately without affecting the other byte and timer hardware does not affect these registers except during reset so registers associated with unused timer functions may be used as normal RAM type locations as previously described.

TOC3 Timer Output Compare-3 Register

See TOC2 explanation above.

TOC4 Timer Output Compare 4 Register

5 See TOC2 explanation above.

TOC5 Timer Output Compare 5 Register

See TOC2 explanation above.

10

TCTL1 Timer Control Register 1 16

15 The Timer Control Register 1 (TCTL 1) 16 is an 8-bit read/write register. All bits in this register are cleared to zero during reset so that all Output Compare functions (2 thru 5) are disconnected from their corresponding Port A 18 output pins. The following Table 4 and paragraphs describe the function of each of the bits.

20 B7 B6 B5 B4 B3 B2 B1 B0

OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
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25 Bit-7 OM2 Output Mode

Bit-6 OL2 Output Level

30 These two control bits are encoded to specify the output action to be taken as a result of a successful OC2 compare.

OM2	OL2	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle disconnected from output pin logic
1	0	Clear OC2 output line to zero
1	1	Set OC2 output line to one

40 Bit-5 OM3 Output Mode

Bit-4 OL3 Output Level

45 These two control bits are encoded to specify the output action to be taken as a result of a successful OC3 compare.

OM3	OL3	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OC3 output line
1	0	Clear OC3 output line to zero
1	1	Set OC3 output line to one

55

Bit-3 OM4 Output Mode

Bit-2 OL4 Output Level

These two control bits are encoded to specify the output action to be taken as a result of a successful OC4 compare.

OM4	OL4	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OC4 output line
1	0	Clear OC4 output line to zero
1	1	Set OC4 output line to one

Bit-1 OM5 Output Mode

Bit-0 OL5 Output Level

These two control bits are encoded to specify the output action to be taken as a result of a successful OC5 compare.

OM4	OL5	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OC5 output line
1	0	Clear OC5 output line to zero
1	1	Set OC5 output line to one

Main Timer Interrupt Mask Register 1 28

The I-interrupt mask in the CC-register is a class interrupt inhibit and no timer interrupt requests are honored while it is set to one. The Timer System Mask Register 1 (TMSK1) 28 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in the Timer Flag Register 1 (TFLG1) 14. For each bit in the Timer Flag Register 1 (TFLG1) 14 there is a corresponding bit in the Timer Mask Register 1 (TMSK1) 28 in the same bit position. If and only if the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence will be requested as well as the flag bit being set.

The Timer Interrupt Mask Register is a read/write register and the bits are described in the following Table 5 and paragraphs.

B7	B6	B5	B4	B3	B2	B1	B0
OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I

Table 5: Timer Interrupt Mask Register 1 (TMSK1) 28

Bit-7 OC1I Output Compare 1 Interrupt

If the OC1I mask bit is set when the OC1F flag bit is set, a hardware interrupt sequence will also be requested.

Bit-6 OC2I Output Compare 2 Interrupt

If the OC2I mask bit is set when the OC2F flag bit is set, a hardware interrupt sequence will also be requested.

Bit-5 OC3I Output Compare 3 Interrupt

If the OC3I mask bit is set when the OC3F flag bit is set, a hardware interrupt sequence will also be requested.

Bit-4 OC4I Output Compare 4 Interrupt

If the OC4I mask bit is set when the OC4F flag bit is set, a hardware interrupt sequence will also be requested.

Bit-3 OC5I Output Compare 5 Interrupt

If the OC5I mask bit is set when the OC5F flag bit is set, a hardware interrupt sequence will also be requested.

Main Timer Interrupt Flag Register 1 TFLG1 14

The Timer Flag Register 1 (TFLG1) 14 is used to indicate the occurrence of timer system events and together with the TMSK1 register 28 allows the timer sub-system to operate in a polled or interrupt driven system. For each bit in the Timer Interrupt Flag Register 1 (TFLG1) 14 there is a corresponding bit in the Timer Mask Register 1 (TMSK1) 28 in the same bit position. If and only if the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence will be requested as well as the flag bit being set.

The Status Register indicates when interrupt conditions have occurred. The on-chip hardware sets these bits as a result of the occurrence of the corresponding condition. To clear a bit or bits in the Timer Interrupt Flag Register (TFLG1) 14, a write operation must be performed to the register where the status bits to be cleared by the write are set to ones. In this way the programmer is not likely to clear a status bit before it has been recognized.

B7	B6	B5	B4	B3	B2	B1	B0
OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F

Table 6: Timer Interrupt Flag Register 1 (TFLG1) 14

Bit-7 OC1F Output Compare 1 Flag

This flag bit is set each time the timer counter matches the output compare register 1 value.

A write operation to this bit with the corresponding data bit equal zero will not affect the state of this bit. A write operation to this bit with the corresponding data bit equal one will cause this bit to be cleared.

Bit-6 OC2F Output Compare 2 Flag

This flag bit is set each time there is a successful compare with the output compare register 2 value.

A write operation to this bit with the corresponding data bit equal zero will not affect the state of this bit. A write operation to this bit with the corresponding data bit equal one will cause this bit to be cleared.

Bit-5 OC3F Output Compare 3 Flag

This flag bit is set each time the timer counter matches the output compare register 3 value.

A write operation to this bit with the corresponding data bit equal zero will not affect the state of this bit. A write operation to this bit with the corresponding data bit equal one will cause this bit to be cleared.

Bit-4 OC4F Output Compare 4 Flag

This flag bit is set each time the timer counter matches the output compare register 4 value.

A write operation to this bit with the corresponding data bit equal zero will not affect the state of this bit.
A write operation to this bit with the corresponding data bit equal one will cause this bit to be cleared.

5 Bit-3 OC5F Output Compare 5 Flag

This flag bit is set each time the timer counter matches the output compare register 5 value.

A write operation to this bit with the corresponding data bit equal zero will not affect the state of this bit.
A write operation to this bit equal one will cause this bit to be cleared.

10

PORTA Port A 18 Data Register

	B7	B6	B5	B4	B3	B2	B1	B0	
15	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
	PIN	PA7/	PA6/	PA5/	PA4/	PA3/	PA2/	PA1/	PA0/
	FUNCTION	PAI/	OC2/	OC3/	OC4/	OC5/	IC1	IC2	IC3
	AND/OR	OC1	OC1	OC1	OC1	OC1			
20									

Table 7: Port A 18 Data Register

- 25 READ: any time (inputs return pin level; outputs return pin driver input level)
- WRITE: data stored in an internal latch (drives pins only if configured for output)
- 30 RESET: causes Port A 18 bits 0,1,2, and 7 to be configured as general purpose inputs, bits 3,4,5, and 6 become general purpose outputs (all zeros).

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CFORC Timer Compare Force Register 22

40	FOC1	FOC2	FOC3	FOC4	FOC5			CFORC
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Table 8: CFORC Timer Compare Force Register 22

45

READ: any time but will always return \$00 (1 state is transient)

WRITE: any time

50

FOC1 - FOC5 Force Output Compare "x" Action

55 A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare "x" to occur at the next timer count transition. The action taken is the same as if a successful comparison had just taken place with the OCx register except the associated interrupt flag does not get set.

OC1M Output Compare 1 Mask Register 24

OC1M7	OC1M6	OC1M5	OC1M4	OC1M3			OC1M
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Table 9: OC1M Output Compare 1 Mask Register 24

READ: any time WRITE: any time

RESET: \$00 (OC1 disconnected from Port A logic)

The bits of OC1M 24 correspond bit-for-bit with the bits of Port A 18. For each bit that is to be affected by the successful OC1 compare, the corresponding bit in OC1M 24 should be set to one.

OC1D Output Compare 1 Data Register 26

OC1D7	OC1D6	OC1D5	OC1D4	OC1D3			OC1D
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Table 10: OC1D Output Compare 1 Data Register 26

RESET: indeterminate

The bits of OC1D 26 correspond bit-for-bit with the bits of Port A 18. When a successful OC1 compare occurs, for each bit that is set in OC1M 24, the corresponding data bit in OC1D 26 is stored to the corresponding bit of Port A 18.

TCNT 16-Bit Timer Count Register

CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8	TCNT (HI)
CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0	TCNT (LO)

TABLE 11: TCNT 16-Bit Timer Count Register

READ: any time WRITE: has no meaning or effect

RESET: \$0000

A full counter 12 read should first address the most significant byte. An MPU read of this address causes the least significant byte to be latched into a buffer for the next CPU cycle so that a double byte read will return the full 16-bit state of the counter 12 at the time of the most significant byte read cycle. This buffer is normally transparent and is accessed when reading the counter least significant byte.

TOC1 - TOC5 Timer Output Compare Registers 10

	B7	B6	B5	B4	B3	B2	B1	B0	
5	OC115	OC114	OC113	OC112	OC111	OC110	OC19	OC18	TOC1 (HI)
	OC17	OC16	OC15	OC14	OC13	OC12	OC11	OC10	TOC1 (LO)
10	OC215	OC214	OC213	OC212	OC211	OC210	OC29	OC28	TOC2 (HI)
	OC27	OC26	OC25	OC24	OC23	OC22	OC21	OC20	TOC2 (LO)
15	OC315	OC314	OC313	OC312	OC311	OC310	OC39	OC38	TOC3 (HI)
	OC37	OC36	OC35	OC34	OC33	OC32	OC31	OC30	TOC3 (LO)
20	OC415	OC414	OC413	OC412	OC411	OC410	OC49	OC48	TOC4 (HI)
	OC47	OC46	OC45	OC44	OC43	OC42	OC41	OC40	TOC4 (LO)
25	OC515	OC514	OC513	OC512	OC511	OC510	OC59	OC58	TOC5 (HI)
	OC57	OC56	OC55	OC54	OC53	OC52	OC51	OC50	TOC5 (LO)
	B7	B6	B5	B4	B3	B2	B1	B0	

Table 12: TOC1-TOC5 Timer Output Compare Registers 10

READ: any time WRITE: any time

RESET: \$FFFF.

A write to a High order byte inhibits the compare for the next E-cycle. When the TOCx register matches the TCNT register, the OCxF bit in the TFLG1 register 14 is set and the specified output action takes place.

Timer Control Register 1 TCTL1 16

	B7	B6	B5	B4	B3	B2	B1	B0	
45	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
50	RESET	0	0	0	0	0	0	0	

TABLE 13: Timer Control Register 1 TCTL1 16

READ: any time WRITE: any time

OMx Output ModeOLx Output Level

- 5 These four pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare.

OMx	OLx	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero

15 Main Timer Interrupt Mask Register 1 TMSK1 28

The bits in TMSK1 28 correspond bit-for-bit with the bits in the TFLG1 14 status register. A zero disables the corresponding flag from causing a hardware interrupt. A one enables the corresponding flag to cause a hardware interrupt.

B7	B6	B5	B4	B3	B2	B1	B0	
OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
RESET	0	0	0	0	0	0	0	

25 **TABLE 14: Main Timer Interrupt Mask Register IMSK1 28**

30 **READ: any time WRITE: any time**

35 OC1I - OC5I Output Compare "x" Interrupt enable

IC1I - IC3I Input Capture "x" Interrupt enable

40 Main Timer Interrupt Flag Register 1 TFLG1 14

The Timer Interrupt Flag Register 14 indicates when interrupt conditions have occurred. On-chip hardware sets these bits as a result of the occurrence of the corresponding condition. To clear a bit or bits in the Timer Interrupt Flag Register. 14, a write operation must be performed to the TFLG1 register 14 where the bits to be cleared by the write are set to ones.

B7	B6	B5	B4	B3	B2	B1	B0	
OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
RESET	0	0	0	0	0	0	0	

55 **TABLE 15: Main Timer Interrupt Flag Register 1 TFLG1 14**

READ: any time

WRITE: used in clearing mechanism (bits set clear
corresponding bits)

OC1F - OC5F Output Compare "x" Flag

10 IC1F - IC3F Input Capture "x" Flag

What has been provided therefore is an improved output compare system and method for automatically controlling multiple outputs in a data processor which provides an efficient means for providing hardware control of any timer output pins which are not used by other output compare functions. The output compare system and method of the present invention allows for efficient implementation of high resolution, positioning to a specific processor cycle, control of unused timer output pins which are not used by other output compare functions and allows for simultaneous utilization of another output compare function to achieve one cycle wide pulses on a timer output pin.

20 Claims

1. A timer system comprising:

- a first counter for counting pulses of a first input signal (E);
- a first compare register (10) for selectively storing a first compare value therein;
- 25 a first comparator (16-Bit Comparator), coupled to the output of the first counter (12) and to the output of the first compare register (10), for comparing the first counter value to the first compare value, and for providing a first compare signal when said values are the same;
- characterised by a data register (OC1D3 to OC1D7) for selectively storing first and second data bits therein;
- 30 a mask register (OC1M3 to OC1M7) for selectively storing first and second mask bits therein; and
- logic means (14, 22, 28, 30, 24, and 28) connected to said first comparator to receive the first compare signal, for providing a first output signal on a first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a first predetermined state, and to provide a second output signal on a second timer output pin indicative of the state of the
- 35 second data bit in response to the first compare signal only if the second mask bit is in a predetermined state, whereby the first compare signal is capable of causing output signals to be provided via more than one timer output pin under control of the mask register.

2. The timer system of claim 1 further comprising:

- 40 a second compare register (10) for selectively storing a second compare value therein; and
- a second comparator (16 Bit Comparator) coupled to the output of the first counter and to the output of the second compare register, for comparing the second counter value to the second compare value, and for providing a second compare signal when said values are the same;
- wherein the logic means (14, 22, 28, 30, 24, and 28) is responsive to both the first and second
- 45 compare signals to provide the first output signal on the first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a predetermined state, to provide the second output signal on the second timer output pin indicative of the state of the second data bit in response to said first compare signal only if the second mask bit is in a predetermined state, to provide a third output signal on the second timer output pin in response to the
- 50 second compare signal and to override said third output signal in favor of said second output signal if said first and second compare signals occur substantially simultaneously.

3. A timer method comprising the steps of:

- counting pulses of a first input signal;
- 55 selectively storing a first compare value and providing a first compare signal when said values are the same;
- characterised by the steps of:
- selectively storing a first and second data bit and a first and second mask bit; and



READ: any time

WRITE: used in clearing mechanism (bits set clear corresponding bits)

5

OC1F - OC5F Output Compare "x" Flag

10 IC1F - IC3F Input Capture "x" Flag

15 What has been provided therefore is an improved output compare system and method for automatically controlling multiple outputs in a data processor which provides an efficient means for providing hardware control of any timer output pins which are not used by other output compare functions. The output compare system and method of the present invention allows for efficient implementation of high resolution, positioning to a specific processor cycle, control of unused timer output pins which are not used by other output compare functions and allows for simultaneous utilization of another output compare function to achieve one cycle wide pulses on a timer output pin.

20 Claims

1. A timer system comprising:

25 a first counter for counting pulses of a first input signal (E);
a first compare register (10) for selectively storing a first compare value therein;
a first comparator (16-Bit Comparator), coupled to the output of the first counter (12) and to the output of the first compare register (10), for comparing the first counter value to the first compare value, and for providing a first compare signal when said values are the same;
characterised by a data register (OC1D3 to OC1D7) for selectively storing first and second data bits therein;
30 a mask register (OC1M3 to OC1M7) for selectively storing first and second mask bits therein; and
logic means (14, 22, 28, 30, 24, and 28) connected to said first comparator to receive the first compare signal, for providing a first output signal on a first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a first predetermined state, and to provide a second output signal on a second timer output pin indicative of the state of the second data bit in response to the first compare signal only if the second mask bit is in a predetermined state, whereby the first compare signal is capable of causing output signals to be provided via more than one timer output pin under control of the mask register.

2. The timer system of claim 1 further comprising:

40 a second compare register (10) for selectively storing a second compare value therein; and
a second comparator (16 Bit Comparator) coupled to the output of the first counter and to the output of the second compare register, for comparing the second counter value to the second compare value, and for providing a second compare signal when said values are the same;
wherein the logic means (14, 22, 28, 30, 24, and 28) is responsive to both the first and second compare signals to provide the first output signal on the first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a predetermined state, to provide the second output signal on the second timer output pin indicative of the state of the second data bit in response to said first compare signal only if the second mask bit is in a predetermined state, to provide a third output signal on the second timer output pin in response to the second compare signal and to override said third output signal in favor of said second output signal if said first and second compare signals occur substantially simultaneously.

3. A timer method comprising the steps of:

55 counting pulses of a first input signal;
selectively storing a first compare value and providing a first compare signal when said values are the same;
characterised by the steps of:
selectively storing a first and second data bit and a first and second mask bit; and



providing a first output signal on a first timer output pin indicative of the state of the first data bit in response to said first compare signal only if the first mask bit is in a predetermined state, and providing a second output signal on a second timer output pin indicative of the state of the second data bit in response to said first compare signal only if the second mask bit is in a predetermined state, whereby the first compare signal is capable of causing output signals to be provided via more than one timer output pin under control of the mask register.

4. The timer method of claim 3 further comprising the steps of:
- selectively storing a second compare signal; and
 - comparing the first count value to the second compare value, and providing a second compare signal when said values are the same;
- wherein the first output signal indicative of the state of the first data bit is provided on the first timer output pin in response to said first compare signal only if the first mask bit is in a predetermined state, the second output signal indicative of the state of the second data bit is provided on the second timer output pin in response to said first compare signal only if the second mask bit is in a predetermined state, a third output signal is provided on the second timer output pin in response to the second compare signal and said third output signal is overridden by said second output signal if said first and second compare signals occur substantially simultaneously.

Revendications

1. Un système de temporisateur comprenant :

- un premier compteur destiné à compter des impulsions d'un premier signal d'entrée (E);
- un premier registre de comparaison (10) destiné à enregistrer sélectivement une première valeur de comparaison;

- un premier comparateur (Comparateur à 16 Bits), connecté à la sortie du premier compteur (12) et à la sortie du premier registre de comparaison (10), pour comparer la valeur du premier compteur avec la première valeur de comparaison, et pour fournir un premier signal de comparaison lorsque ces valeurs sont les mêmes;

- caractérisé par un registre de données (OC1D3 à OC1D7) destiné à enregistrer sélectivement des premier et second bits de données;

- un registre de masque (OC1M3 à OC1M7) destiné à enregistrer sélectivement des premier et second bits de masque; et

- des moyens logiques (14, 22, 28, 30, 24 et 28) connectés au premier comparateur pour recevoir le premier signal de comparaison, pour produire un premier signal de sortie sur une première broche de sortie de temporisateur, représentatif de l'état du premier bit de données, sous l'effet du premier signal de comparaison, seulement si le premier bit de masque est dans un premier état prédéterminé, et pour fournir un second signal de sortie sur une seconde broche de sortie de temporisateur, représentatif de l'état du second bit de données, sous l'effet du premier signal de comparaison, seulement si le second bit de masque est dans un état prédéterminé, grâce à quoi le premier signal de comparaison est capable de faire apparaître des signaux de sortie sur plus d'une broche de sortie de temporisateur, sous la commande du registre de masque.

2. Le système de temporisateur de la revendication 1, comprenant en outre :

- un second registre de comparaison (10) destiné à enregistrer sélectivement une seconde valeur de comparaison; et

- un second comparateur (Comparateur à 16 Bits) connecté à la sortie du premier compteur et à la sortie du second registre de comparaison, pour comparer la valeur du second compteur avec la seconde valeur de comparaison, et pour produire un second signal de comparaison lorsque ces valeurs sont les mêmes;

- dans lequel les moyens logiques (14, 22, 28, 30, 24 et 28) réagissent aux premier et second signaux de comparaison en produisant le premier signal de sortie sur la première broche de sortie de temporisateur, représentatif de l'état du premier bit de données, sous l'effet du premier signal de comparaison, seulement si le premier bit de masque est dans un état prédéterminé, en produisant le second signal de sortie sur la seconde broche de sortie de temporisateur, représentatif de l'état du second bit de données, sous l'effet du premier signal de comparaison, seulement si le second bit de masque est dans un état prédéterminé, en produisant un troisième signal de sortie sur la seconde broche de sortie de temporisateur, sous l'effet du second signal de comparaison, et en accordant la



priorité au second signal de sortie vis-à-vis du troisième signal de sortie, si les premier et second signaux de comparaison apparaissent de façon pratiquement simultanée.

3. Un procédé de temporisation comprenant les étapes suivantes :

- 5 on compte des impulsions d'un premier signal d'entrée;
on enregistre sélectivement une première valeur de comparaison et on produit un premier signal de comparaison lorsque ces valeurs sont les mêmes;
caractérisé par les étapes suivantes :
10 on enregistre sélectivement des premier et second bits de données et des premier et second bits de masque;
et on produit un premier signal de sortie sur une première broche de sortie de temporisateur, représentatif de l'état du premier bit de données, sous l'effet du premier signal de comparaison, seulement si le premier bit de masque est dans un état prédéterminé, et on produit un second signal de sortie sur une seconde broche de sortie de temporisateur, représentatif de l'état du second bit de données, sous l'effet du premier signal de comparaison, seulement si le second bit de masque est dans un état prédéterminé, grâce à quoi le premier signal de comparaison est capable de faire apparaître des signaux de sortie sur plus d'une broche de sortie de temporisateur, sous la commande du registre de masque.

20 4. Le procédé de temporisation de la revendication 3, comprenant en outre les étapes suivantes :

- on enregistre sélectivement un second signal de comparaison; et
on compare la première valeur de comptage à la seconde valeur de comparaison, et on produit un second signal de comparaison lorsque ces valeurs sont les mêmes;
25 dans lequel le premier signal de sortie représentatif de l'état du premier bit de données est fourni sur la première broche de sortie de temporisateur, sous l'effet du premier signal de comparaison, seulement si le premier bit de masque est dans un état prédéterminé, le second signal de sortie représentatif de l'état du second bit de données est fourni sur la seconde broche de sortie de temporisateur sous l'effet du premier signal de comparaison, seulement si le second bit de masque est dans un état prédéterminé, un troisième signal de sortie est fourni sur la seconde broche de sortie de temporisateur sous l'effet du second signal de comparaison, et le second signal de sortie a priorité sur ce troisième signal de sortie si les premier et second signaux de comparaison apparaissent de façon pratiquement simultanée.

Patentansprüche

- 35 1. Zeitgebersystem mit:
einem ersten Zähler zum Zählen von Impulsen eines ersten Eingangssignals (E);
einem ersten Vergleichsregister (10) zum selektiven Speichern einer ersten Vergleichswertes darin;
einem ersten Komparator (16-Bit Komparator), der mit dem Ausgang des ersten Zählers (12) und dem Ausgang des ersten Vergleichsregisters (10) verbunden ist, zum Vergleichen des ersten Zählwertes mit dem ersten Vergleichswert und zum Erzeugen eines ersten Vergleichssignals, wenn die Werte dieselben sind;
geennzeichnet durch ein Datenregister (OC1D3 bis OC1D7) zum selektiven Speichern von ersten und zweiten Maskenbits darin; und durch
45 eine Logikvorrichtung (14, 22, 28, 30, 24 und 28), die mit dem ersten Komparator zum Erhalten des ersten Vergleichssignals verbunden ist, zum Erzeugen eines ersten Ausgangssignals auf einem ersten Zeitgeberausgabestift, das den Zustand des ersten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das erste Maskenbit in einem ersten, vorgegebenen Zustand ist, und zum Erzeugen eines zweiten Ausgangssignals auf einem zweiten Zeitgeberausgabestift, das den Zustand des zweiten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das zweite Maskenbit in einem vorgegebenen Zustand ist, wobei das erste Vergleichssignal geeignet ist, zu veranlassen, daß die Ausgangssignale über mehr als einen Zeitgeberausgangsstift unter der Kontrolle des Maskenregisters erzeugt werden.
- 50 2. Zeitgebersystem nach Anspruch 1, das außerdem umfaßt:
ein zweites Vergleichsregister (10) zum selektiven Speichern eines zweiten Vergleichswertes darin;
einen zweiten Komparator (16-Bit Komparator), der mit dem Ausgang des ersten Zählers (12) und dem Ausgang des zweiten Vergleichsregisters (10) verbunden ist, zum Vergleichen des zweiten



Zählwertes mit dem zweiten Vergleichswert und zum Erzeugen eines zweiten Vergleichssignals, wenn die Werte dieselben sind;

wobei eine Logikvorrichtung (14, 22, 28, 30, 24 und 28) sowohl auf das erste als auch auf das zweite Vergleichssignal reagiert zum Erzeugen des ersten Ausgangssignals auf dem ersten Zeitgeberausgabestift, das den Zustand des ersten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das erste Maskenbit in einem vorgegebenen Zustand ist, zum Erzeugen des zweiten Ausgangssignals auf dem zweiten Zeitgeberausgabestift, das den Zustand des zweiten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das zweite Maskenbit in einem vorgegebenen Zustand ist, und zum Erzeugen eines dritten Ausgangssignals auf dem zweiten Zeitgeberausgabestift in Abhängigkeit von dem zweiten Vergleichssignal und zum Überschreiben des dritten Ausgangssignals zu Gunsten des zweiten Ausgangssignals, wenn die ersten und zweiten Ausgangssignale im wesentlichen gleichzeitig auftreten.

3. Zeitgeberverfahren mit folgenden Verfahrensschritten:

Zählen von Impulsen eines ersten Eingabesignals; Erzeugen eines ersten Vergleichssignals, wenn die Werte dieselben sind;

gekennzeichnet durch folgende Verfahrensschritte:

Erzeugen eines ersten Ausgangssignals auf einem ersten Zeitgeberausgabestift, das den Zustand des ersten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das erste Maskenbit in einem vorgegebenen Zustand ist, und Erzeugen eines zweiten Ausgangssignals auf einem zweiten Zeitgeberausgabestift, das den Zustand des zweiten Datenbits in Abhängigkeit von dem ersten Vergleichssignal nur dann angibt, wenn das zweite Maskenbit in einem vorgegebenen Zustand ist, wobei das erste Vergleichssignal geeignet ist, zu veranlassen, daß die Ausgangssignale über mehr als einen Zeitgeberausgabestift unter der Kontrolle des Maskenregisters erzeugt werden.

4. Zeitgeberverfahren nach Anspruch 3, das außerdem folgende Verfahrensschritte umfaßt:

selektives Speichern eines zweiten Vergleichswertes; und Vergleichen des zweiten Zählwertes mit dem zweiten Vergleichswert und Erzeugen eines zweiten Vergleichssignals, wenn die Werte dieselben sind;

wobei das erste Ausgangssignal, das den Zustand des ersten Datenbits angibt, in Abhängigkeit von dem ersten Vergleichssignal auf dem ersten Zeitgeberausgabestift nur dann ausgegeben wird, wenn das erste Maskenbit in einem vorgegebenen Zustand ist, wobei das zweite Ausgangssignal, das den Zustand des zweiten Datenbits angibt, in Abhängigkeit von dem zweiten Vergleichssignal auf dem zweiten Zeitgeberausgabestift nur dann ausgegeben wird, wenn das zweite Maskenbit in einem vorgegebenen Zustand ist, wobei ein drittes Ausgangssignal auf dem zweiten Zeitgeberausgabestift in Abhängigkeit von dem zweiten Vergleichssignal ausgegeben wird und wobei das dritte Ausgangssignal zu Gunsten des zweiten Ausgangssignals überschrieben wird, wenn die ersten und zweiten Ausgangssignale im wesentlichen gleichzeitig auftreten.