

ABSOLUTE VALUE ARITHMETIC CIRCUIT

DESCRIPTION

The present invention relates to an absolute value
5 arithmetic circuit for computing the absolute value of a
difference between two digital values in a digital signal
processor (DSP), a microprocessor, a microcomputer or the
like.

10 Heretofore, technology in the above-mentioned field is
disclosed in literature "Study of Absolute Value Computing
System" issued at the 1986th national conference of the
communication branch of the Institute of Electronics
Communication Engineers, 1-46. The arrangement disclosed in
15 this literature will be explained hereinbelow.

Figs. 2a to 2d are circuit block diagrams illustrating the
conventional absolute value arithmetic circuit. Fig. 2a
shows a parallel type circuit, Fig. 2b shows a series type
20 circuit, Fig. 2c shows an input register type circuit, and
Fig. 2d shows an output feed-back type circuit.

In Fig. 2a, the parallel type absolute value computing
circuit 10 is composed of two subtracters connected in

parallel with each other, and a selector 13.

The subtracters 11 and 12 calculate differences between two input signals S_{in1} and S_{in2} , that is $(S_{in1} - S_{in2})$ and $(S_{in2} - S_{in1})$, respectively. The selector 13 selects and outputs a positive result of the calculation. In this arrangement, for example, the subtracter 11 outputs the most significant bit denoted hereinbelow as "MSB") or the sign digit bit as a control input signal S_c to control the selector 13.

The series type absolute value arithmetic circuit 20 shown in Fig. 2b is composed of a subtracter 21, a sign inverter 22 connected in series to the subtracter 21 and a selector 23. The sign inverter 22 is composed of a 2's complement circuit including an inverting circuit and an adder.

In this absolute value arithmetic circuit 20, the subtracter 21 calculates a difference between two input signals S_{in1} and S_{in2} , that is, $(S_{in1} - S_{in2})$. In accordance with a resultant signal of the computation, if the value is positive the selector 23 outputs the value as it is, but if the value is negative, it selects and delivers an output from the sign inverter 22 by which the value is inverted and is subjected to 2's complement computation by addition. In this arrangement, for example, the subtracter 21 outputs the MSB which is used as a control input signal S_c to the selector 23.

In Fig. 2c, the input register type absolute value arithmetic circuit 30 shown in Fig. 2c, is composed of registers 31 and 32, a selector 33, and a subtracter 34.

In this absolute value arithmetic circuit 30, two input signals Sin1 and Sin2 are stored in the registers 31 and 32, respectively, and the subtracter 34 calculates a difference between the two input signals Sin1 and Sin2, that is, $(\text{Sin1} - \text{Sin2})$. If the result of the calculation is a positive value, the selector 33 outputs the value as it is. However, if it is negative, the selector 33 exchanges the signals stored in the registers 31 and 32. The subtracter 34 again subtracts the thus replaced signals and delivers the result of the subtraction during the next clock cycle. In this arrangement, for example, the MSB of an output from the subtracter 34 is used as a control input signal Sc to the selector 33.

The output feed-back type absolute value arithmetic circuit 40, as shown in Fig. 2d, is composed of a subtracter 41, a register 42, and a selector 43.

In this absolute value computing circuit 40, the subtracter 43 calculates a difference between two input signals Sin1 and Sin2, that is, $(\text{Sin1} - \text{Sin2})$, and if the difference is positive, the value thereof is once stored in the register 42 and is then delivered as it is. But if it is negative, the value stored in the register 42 is selected by the selector 43 in accordance with a control input signal Sc, and then the sign thereof is inverted by the subtracter

41, then the thus obtained value being outputted.

In the conventional absolute value arithmetic circuits 10, 20, 30, and 40, when two input signals Sin1 and Sin2 are inputted, the absolute value of a difference between the two signals Sin1 and Sin2, that is, $|sin1 - sin2|$ is calculated.

However, the conventional absolute value arithmetic circuits 10, 20, 30 and 40 have the following problems:

The parallel type absolute value arithmetic circuit 10 can compute in short time, or one clock cycle, but requires two computing units 11, 12, thus leading to complicated hardware.

The series type absolute value arithmetic circuit 20 has advantages in view of the scale of the hardware in comparison with that of the absolute value arithmetic circuit 10. However, the process of addition for 2's complement calculation carried out by the sign inverter 22 causes longer computation time. The computation time is substantially twice as long as that of the absolute value computing circuit 10.

With the input register type absolute value arithmetic circuit 30, the scale of the hardware thereof is smaller than that of the absolute value arithmetic circuits 10, 20. But, the computation time requires two clock cycles.

With the output feed-back type absolute value arithmetic circuit 40, the scale of the hardware thereof can be relatively small. But two clock cycles is required for computation.

In the conventional absolute value arithmetic circuits, it has been difficult to miniaturize its circuit size and to satisfy high speed computation.

5 The present invention is devised in view of the above-mentioned problems inherent to the conventional arrangements. Accordingly, one object of the present invention is to provide a miniaturized high-speed absolute value arithmetic circuit.

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According to the present invention, there is provided an absolute value arithmetic circuit for computing an absolute value of a difference between two binary input signals, comprising: a computing circuit for computing a difference
15 signal representing the difference between said two input signals; a 1's complementor for inverting or not inverting the difference signal in accordance with the state of a sign bit of the difference signal; a priority encoder for searching for the location of the least significant zero bit
20 in the difference signal; and a bit inverting circuit, responsive to the state of said sign bit, to either invert only those bits of the difference signal from the least significant bit to the least significant zero bit located by the priority encoder or pass the difference signal un
25 modified so as to output a signal representing the absolute value of the difference between said input signals.

In an absolute value arithmetic circuit, embodying the present invention, the computing circuit obtains a difference between two binary input signals, and the 1's complementor converts the difference between two binary input signals into a 1's complement which is obtained by the computing element, with the use of the sign digit bit (for example, the most significant bit) of the difference between the two binary input signals when the difference is negative, but delivers the value of the difference as it is when the difference is positive.

The priority encoder searches the output of the 1's complementor for the position of a bit which is "0" bit at first, starting from the least significant bit (LSB), and delivers an encoder output which is a data indicating the position of this "0" bit, (bit position output).

The bit inverting circuit receives and output from the 1's complementor and an encoder output from the priority encoder, and acts upon the output from the 1's complementor to invert a bit pattern on the least significant bit side (LSB side) including the "0" bit indicated by the encoder output when the difference between the two binary input signals obtained by the computing circuit is negative.

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With this arrangement, the above-mentioned purpose of the

present invention can be achieved.

An embodiment of the present invention will now be described, by way of example, with reference to Figures 1, 3 and 4 of the accompanying drawings, in which:

Fig. 1 is a circuit diagram illustrating an absolute value arithmetic circuit in an embodiment of the present invention;

10 Fig. 2a to 2d are circuit diagrams illustrating conventional absolute value arithmetic circuits;

Fig. 3 is a circuit diagram showing a 1's complementor shown in Fig. 1; and

Fig. 4 is a circuit diagram illustrating an LSB bit
15 inverting circuit shown in Fig. 1.

The absolute arithmetic circuit 50 comprises a computing circuit 51, a 1's complementor 52, a priority encoder 53, and a bit inverting circuit 54.

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The computing circuit 51 performs subtraction

(Sin11 - Sin12) where Sin11 and Sin12 are binary data. The computing circuit 51 delivers a binary digit string Qs as a result of computation to the complementor 52. The most significant bit of the binary digit string Qs indicates a sign. For example, when the most significant bit is "0", Qs is a positive number, but if it is "1", Qs is a negative number which is indicated by a 2's complement.

The 1's complementor 52 delivers a binary digit string Qc which is equal to the inputted binary digit string Qs to the priority encoder 53 and the bit inverting circuit 54 when the most significant digit bit of the binary digit string is "0". When the most significant bit is "1", the 1's complementor 52 delivers a binary digit string Qc which is obtained by inverting all bits of the binary digit string Qs to the priority encoder 53 and the bit inverting circuit 54. In other words, the binary digit string Qc is the one which is obtained by converting the binary digit string Qs into a 1's complement. As shown in Fig. 3, the 1's complementor 52 requires an inverter 52-1 and exclusive NOR gates (denoted as Ex.NOR gate) 52-2 to 52-9 if the binary digit string Qs consists of 8 bits.

The priority encoder 53 searches the binary digit string Qc for the bit which has a value of "0". The priority encoder 53 delivers a data Qe which exhibits the position of the least significant bit "0" of the bits which have been searched. For example, if the binary digit string Qc is "00011011", Qe becomes data indicating "3". The

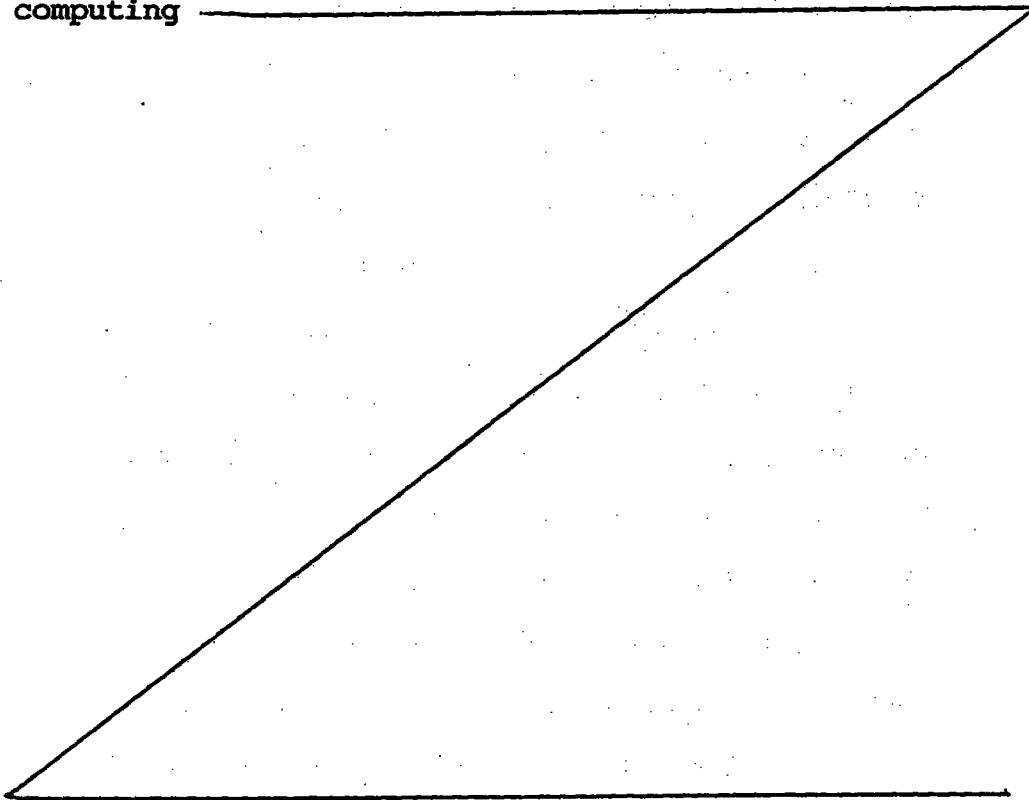
priority encoder 53 is composed of NAND gate, NOR gate and the like.

5 The bit inverting circuit 54 delivers a binary digit string which is equal to the inputted binary digit string Qc if the most significant bit of the binary digit string Qs is "0". If the most significant bit of the binary digit string Qs is "1", the bit inverting circuit 54 inverts only bits that are less than or
10 equal to the position of a bit of the binary digit string Qc, which is exhibited by the data Qe. The bit inverting circuit 54 delivers a binary digit string which is obtained by the inversion. For example, if the binary digit string Qc is "00011011" and Qe is "3",
15 the bit inverting circuit 54 delivers "00011100". As shown in Fig. 4, if the binary digit string Qs consists of 8 bits, the bit inverting circuit 54 requires inverters 54-1 to 54-8, selecting circuit portions (denoted as "SELS") 54-9 to 54-16, and a decoding unit
20 54-17. The decoding unit 54-17 converts the data Qe into inversion control signals C7 to C0. The decoding unit 54-17 is composed of a ROM converter, a

programmable logic array or the like. The inversion control signals C7 to C0 selectively control the SELs 54-9 to 54-16, respectively.

- 5 Next, explanation will be made of operation of a 8-bit absolute value arithmetic circuit.

The computing circuit 51 carries out subtraction between two binary input data Sin11, Sin12. The
10 computing



circuit 51 delivers a binary digit string Qs which is a result of the subtraction, to the 1's complementor 52. The 1's complementor 52 delivers bits I7 to I0 of the binary digit string Qs to the Ex.NOR gates 52-2 to 52-9. The 1's complementor 52 delivers the most significant bit of the binary digit string Qs to the NOR gates 52-2 to 52-9 by way of the inverter 52-1. Accordingly, if the most significant bit is "0", Ex.NOR gates 52-1 to 52-9 delivers bits 07 to 00 which are equal to the bits I7 to I0 to priority encoder 53 and the bit inverting circuit 54. If the most significant bit is "1", the Ex.NOR gates 52-1 to 52-9 deliver bits 07 to 00 which are obtained by inverting bits I7 to I0 to the priority encoder 53 and the bit inverting circuit 54. Bits 07 to 00 will be denoted hereinbelow as the binary digit string Qc.

The priority encoder 53 searches bits 07 to 00 of the binary digit string Qc for those having a value "0". The priority encoder 53 delivers a data Qe which exhibits the position of the least significant bit among searched bits having a value of "0", to the bit inverting circuit 54. It is noted that the data Qe may be binary, that is, for example, if it is "3", it may be exhibited by "11".

The bit inverting circuit 54 delivers the data Qe and the most significant bit of the binary digit string Qs to the decoding unit 54-17. If the most significant bit of Qs is a value "0", the decoding unit 54-17 neglects the data Qe. That is, the decoding portion 54-17 delivers the

inversion control data C7 to C0 which does not invert bits 07 to 00, to the SELs 54-9 to 54-16. The SELs 54-9 to 54-16 set in accordance with the inversion control data C7 to C0 so that bits 07 to 00 are
5 delivered as I7 to I0 without through the inverters 54-1 to 54-8. Accordingly, the bit inverting circuit 54 delivers bits I7 to I0 which are equal to bits 007 to 00 of the binary digit string Qc. If the most significant bit of Qs is a value "1", the decoding
10 portion 54-17 delivers to the SELs 54-19 to 54-16 the inversion control data C7 to C0 for inverting only those of bits 07 to 00 which are less than or equal to the position of the bit exhibited by the data Qe. The SELs for the lower digit bits corresponding
15 to those of the inversion control data C7 to C0 which are inversion data, set so that the inputted bits are delivered through the inverters. The upper digit bit SELs corresponding to those of the inversion control

data C7 to C0 which are non-inversion data sets so that the inputted data are delivered without through the inverters.

According, the bit inverting circuit 54 inverts those of
5 bits 07 to 00 of the binary digit string Qc that are less than or equal to the position of the bit exhibited by the data Qc but does not invert the other bits, and accordingly, delivers I7 to I0. For example, if the binary digit string Qe is "10011011" and the data Qe is "3", the output of the
10 bit inverting circuit 54 becomes "10011100" which is similar to that obtained by adding "1" to the binary digit string Qc.

As mentioned above, if the result of the subtraction

between two data S_{in11} , S_{in12} is positive, the absolute value arithmetic circuit 50 directly delivers it as it is. However, the absolute value arithmetic circuit 50 carries out 2's complement conversion without using addition for the result of the subtraction if the result of the subtraction is negative. The absolute value arithmetic circuit 50 delivers the result of subtraction which is given by 2's complement conversion. In other words, this output becomes the absolute value $|sin11 - sin12|$.

The embodiment offers the following advantages:

A single computing circuit 51 is used for the absolute value arithmetic circuit 50. The 1's complementor 52, the priority encoder 53 and the bit inverting circuit 54 are provided for computing the absolute value of the difference obtained by the computing element 51. In order to perform the absolute value computation, the 1's complementor 52 carries out 1's complement calculation, the priority encoder 53 carries out the "0" bit detection, and the bit inverting circuit 54 performs the inversion of bits lower than the "0" bit.

Accordingly, with the absolute value arithmetic circuit 50 in this embodiment, it is possible to reduce the scale of hardware and to shorten the computation time in comparison with the conventional absolute value arithmetic circuits 10, 20, 30, and 40.

It is noted here that the present invention should not be limited only to the above-mentioned embodiment, but

various changes and modification can be made thereto.

For example, the absolute value arithmetic circuit 50 can be changed in the arrangement. The computing circuit 51 is a subtracter. In this case, the hardware arrangement of the absolute value arithmetic circuit 50 can be reduced more in its scale. Further, the computing element 51 also may be constituted by an arithmetic logic unit (ALU) or the like. Accordingly, its hardware arrangement can be also used for computation other than that for the absolute value.

Further, although the 1's complementor 52 and the bit inverting circuit 54 have been used for data having a 8 bit length, the number of component elements can be changed depending upon a length of data. The logic gates may be modified in other arrangements. Further, the logic level should not be limited to that stated in the above-mentioned embodiment.

As mentioned above, the absolute value arithmetic circuit according to the present invention is composed of a computing circuit, a 1's complementor, a priority encoder and a bit inverting circuit. The computing circuit can be restrained to only one. The complement calculation in the absolute value computation process can be made by a logic inversion process and a "0" bit detection without using an addition process.

Accordingly, it is possible to realize an absolute value arithmetic circuit which has a less hardware scale and a miniature size and which performs a high speed arithmetic

operation.

As used herein the terms "1" and "0" are intended as relative terms, indicating opposite binary levels.

5 Thus as used in the description and/or the claims "1" could be replaced by "0" throughout without altering the scope of the invention.



CLAIMS

1. An absolute value arithmetic circuit for computing an absolute value of a difference between two binary input signals, comprising:
5 a computing circuit for computing a difference signal representing the difference between said two input signals;
a 1's complementor for inverting or not inverting the difference signal in accordance with the state of a sign bit
10 of the difference signal;
a priority encoder for searching for the location of the least significant zero bit in the difference signal; and
a bit inverting circuit, responsive to the state of said sign bit, to either invert only those bits of the difference
15 signal from the least significant bit to the least significant zero bit located by the priority encoder or pass the difference signal un modified so as to output a signal representing the absolute value of the difference between said input signals.
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2. An absolute value arithmetic circuit according to claim 1, wherein the computing circuit is a subtractor.
3. An absolute value arithmetic circuit according to claim
25 1, wherein the computing circuit is an arithmetic logic unit .

4. An absolute value arithmetic circuit substantially as hereinbefore described with reference to Figures 1, 3 and 4 of the accompanying drawings.
