Claims

What is claimed is:

1. A semiconductor device, comprising:

a first fin disposed on a substrate, the first fin comprising first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from a first type of extrinsic semiconductor, and

the second and fourth materials are formed from a second type of extrinsic semiconductor, the second type different from the first type; and

a second fin disposed on the substrate, laterally separated from the first fin, wherein the second fin has a material that is materially contiguous with at least one of the first, second, third or fourth materials.

2. The semiconductor device of claim 1, wherein the first type of extrinsic semiconductor is one of an N-type and a P-type, and wherein the second type of extrinsic semiconductor is an N-type if the first type of extrinsic semiconductor is a P-type, or a P-type if the first type of extrinsic semiconductor is an N-type.

3. The semiconductor device of any of claims 1-2, further comprising a first conductive contact disposed on the fourth material.

4. The semiconductor device of claim 3, wherein:

the first fin has a first portion and a second portion;

the first, second, third and fourth materials of the first fin are included in the first portion;

the second portion includes first and second materials;

the first material of the second portion is materially contiguous with the first material of the first portion;

the second material of the second portion is materially contiguous with the second material of the first portion; and

the semiconductor device further comprises a second conductive contact disposed on the second material of the second portion.

5. The semiconductor device of claim 4, wherein the first conductive contact is disposed on a first surface of the fourth material of the first portion, the second conductive contact is disposed on a second surface of the second material of the second portion, and the first and second surfaces are substantially in the same plane.

6. The semiconductor device of claim 4, wherein the fourth material of the first portion and the second material of the second portion are laterally separated by a material that is materially contiguous with the third material of the first portion.

7. The semiconductor device of claim 4, further comprising a third conductive contact disposed on the second fin.

8. The semiconductor device of any of claims 1-2, wherein the second fin is laterally separated from the first fin by an insulator.

9. The semiconductor device of any of claims 1-2, wherein the semiconductor device is a thyristor.

10. The semiconductor device of any of claims 1-2, wherein the material of the second fin is materially contiguous with the first material.

11. A method of fabricating a semiconductor device, comprising:

forming first and second fins on a substrate, the first and second fins extending away from the substrate and laterally separated; and

forming first, second, third and fourth dopant source films of first, second, third and fourth dopants, respectively, in contact with a side surface of a portion of a first fin, wherein:

the first dopant source film is disposed in contact with a side surface of a portion of the first fin, in contact with the second fin, and between the second dopant source film and the substrate,

the second dopant source film is disposed in contact with the side surface of the portion of the first fin and between the third dopant source film and the first dopant source film,

the third dopant source film is disposed in contact with the side surface of the portion of the first fin and between the fourth dopant source film and the second dopant source film,

the first and third dopant source films include a dopant for a first type of extrinsic semiconductor, and

the second and fourth dopant source films include a dopant for a second type of extrinsic semiconductor, the second type different from the first type.

12. The method of claim 11, wherein the fourth dopant source film is in contact with a top surface of the portion of the first fin.

13. The method of any of claims 11-12, further comprising:

driving dopants from the first, second, third and fourth dopant source films into the portion of the first fin to form first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from the first type of extrinsic semiconductor, and

the second and fourth materials are formed from the second type of extrinsic semiconductor.

14. The method of claim 13, further comprising:

forming a first conductive contact on the fourth material; and

forming a second conductive contact on a material that is materially contiguous with the second material.

15. The method of claim 14, further comprising:

forming a third conductive contact on a material of the second fin that is materially contiguous with the first material.

16. The method of claim 14, wherein the first, second, third and fourth materials are included in a thyristor.

17. The method of any of claims 11-12, wherein the first, second, third or fourth dopants comprise a doped glass.

18. An integrated circuit device, comprising:

a silicon substrate;

an interconnect layer comprising interconnect structures and an interlayer dielectric; and

one or more semiconductor devices, disposed between the silicon substrate and the interconnect layer, each of the one or more semiconductor devices comprising:

a first fin disposed on the silicon substrate, the first fin comprising first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the silicon substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from a first type of extrinsic semiconductor, and

the second and fourth materials are formed from a second type of extrinsic semiconductor, the second type different from the first type, and

a second fin disposed on the substrate, laterally separated from the first fin, wherein the second fin has a material that is materially contiguous with at least one of the first, second, third or fourth materials.

19. The integrated circuit device of claim 18, wherein the one or more semiconductor devices is included in electrostatic discharge protection circuitry.

20. The integrated circuit device of claim 19, wherein the electrostatic discharge protection circuitry includes a high voltage clamp.

21. The integrated circuit device of any of claims 18-20, wherein:

the one or more semiconductor devices comprises a plurality of semiconductor devices;

the arrangement of the first and second fins of an individual semiconductor device define an axis; and

the plurality of axes corresponding to the plurality of semiconductor devices are substantially parallel.

22. The integrated circuit device of any of claims 18-20, wherein at least one of the one or more semiconductor devices is a thyristor.

Claims

What is claimed is:

1. A semiconductor device, comprising:

a first fin disposed on a substrate, the first fin comprising first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from a first type of extrinsic semiconductor, and

the second and fourth materials are formed from a second type of extrinsic semiconductor, the second type different from the first type; and

a second fin disposed on the substrate, laterally separated from the first fin, wherein the second fin has a material that is materially contiguous with at least one of the first, second, third or fourth materials.

2. The semiconductor device of claim 1, wherein the first type of extrinsic semiconductor is one of an N-type and a P-type, and wherein the second type of extrinsic semiconductor is an N-type if the first type of extrinsic semiconductor is a P-type, or a P-type if the first type of extrinsic semiconductor is an N-type.

3. The semiconductor device of claim 1, further comprising a first conductive contact disposed on the fourth material.

4. The semiconductor device of claim 3, wherein:

the first fin has a first portion and a second portion;

the first, second, third and fourth materials of the first fin are included in the first portion;

the second portion includes first and second materials;

the first material of the second portion is materially contiguous with the first material of the first portion;

the second material of the second portion is materially contiguous with the second material of the first portion; and

the semiconductor device further comprises a second conductive contact disposed on the second material of the second portion.

5. The semiconductor device of claim 4, wherein the first conductive contact is disposed on a first surface of the fourth material of the first portion, the second conductive contact is disposed on a second surface of the second material of the second portion, and the first and second surfaces are substantially in the same plane.

6. The semiconductor device of claim 4, wherein the fourth material of the first portion and the second material of the second portion are laterally separated by a material that is materially contiguous with the third material of the first portion.

7. The semiconductor device of claim 4, further comprising a third conductive contact disposed on the second fin.

8. The semiconductor device of claim 1, wherein the second fin is laterally separated from the first fin by an insulator.

9. The semiconductor device of claim 1, wherein the semiconductor device is a thyristor.

10. The semiconductor device of claim 1, wherein the material of the second fin is materially contiguous with the first material.

11. A method of fabricating a semiconductor device, comprising:

forming first and second fins on a substrate, the first and second fins extending away from the substrate and laterally separated; and

forming first, second, third and fourth dopant source films of first, second, third and fourth dopants, respectively, in contact with a side surface of a portion of a first fin, wherein:

the first dopant source film is disposed in contact with a side surface of a portion of the first fin, in contact with the second fin, and between the second dopant source film and the substrate,

the second dopant source film is disposed in contact with the side surface of the portion of the first fin and between the third dopant source film and the first dopant source film,

the third dopant source film is disposed in contact with the side surface of the portion of the first fin and between the fourth dopant source film and the second dopant source film,

the first and third dopant source films include a dopant for a first type of extrinsic semiconductor, and

the second and fourth dopant source films include a dopant for a second type of extrinsic semiconductor, the second type different from the first type.

12. The method of claim 11, wherein the fourth dopant source film is in contact with a top surface of the portion of the first fin.

13. The method of claim 11, further comprising:

driving dopants from the first, second, third and fourth dopant source films into the portion of the first fin to form first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from the first type of extrinsic semiconductor, and

the second and fourth materials are formed from the second type of extrinsic semiconductor.

14. The method of claim 13, further comprising:

forming a first conductive contact on the fourth material; and

forming a second conductive contact on a material that is materially contiguous with the second material.

15. The method of claim 14, further comprising:

forming a third conductive contact on a material of the second fin that is materially contiguous with the first material.

16. The method of claim 14, wherein the first, second, third and fourth materials are included in a thyristor.

17. The method of claim 11, wherein the first, second, third or fourth dopants comprise a doped glass.

18. An integrated circuit device, comprising:

a silicon substrate;

an interconnect layer comprising interconnect structures and an interlayer dielectric; and

one or more semiconductor devices, disposed between the silicon substrate and the interconnect layer, each of the one or more semiconductor devices comprising:

a first fin disposed on the silicon substrate, the first fin comprising first, second, third and fourth materials, wherein:

the first material is disposed between the second material and the silicon substrate,

the second material is disposed between the third material and the first material,

the third material is disposed between the fourth material and the second material,

the first and third materials are formed from a first type of extrinsic semiconductor, and

the second and fourth materials are formed from a second type of extrinsic semiconductor, the second type different from the first type, and

a second fin disposed on the substrate, laterally separated from the first fin, wherein the second fin has a material that is materially contiguous with at least one of the first, second, third or fourth materials.

19. The integrated circuit device of claim 18, wherein the one or more semiconductor devices is included in electrostatic discharge protection circuitry.

20. The integrated circuit device of claim 19, wherein the electrostatic discharge protection circuitry includes a high voltage clamp.

21. The integrated circuit device of claim 18, wherein:

the one or more semiconductor devices comprises a plurality of semiconductor devices;

the arrangement of the first and second fins of an individual semiconductor device define an axis; and

the plurality of axes corresponding to the plurality of semiconductor devices are substantially parallel.

22. The integrated circuit device of claim 18, wherein at least one of the one or more semiconductor devices is a thyristor.