

1 TRIGGERED BACK-TO-BACK DIODES FOR ESD PROTECTION IN TRIPLE-
2 WELL CMOS PROCESS
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4

5 ABSTRACT

6 An embodiment is a Electro Static Discharge (ESD) protection device
7 comprising: a n-doped region and a p-doped region in a p-well in a semiconductor
8 structure. The n-doped region and the p-doped region are spaced. A n-well and a deep n-
9 well surrounding the p-well on the sides and bottom. A first I/O pad connected to the n-
10 doped region. A trigger circuit connected the first I/O pad and the p-doped region. A
11 second I/O pad connected to the n-well. A parasitic bipolar transistor is comprised of the
12 n-doped region that functions as a collector terminal, the P-well that functions as a base
13 terminal, and the deep N-well that functions as the emitter terminal. Whereby under an
14 ESD condition, the p-well is charged positive using the trigger circuit and the parasitic
15 bipolar transistor can be turned on.
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Figure 1A