

RASTER DISTORTION CORRECTION CIRCUITTHIS SHEET HAS BEEN
REPLACED

The invention relates to a deflection circuit of a video display apparatus.

5 A horizontal deflection circuit is, typically, required to be accurately phased or synchronized to a video signal containing picture information for obtaining a correct raster display. In common practice, a retrace pulse produced in a flyback transformer of the deflection circuit is employed for providing a feedback pulse in a phase-controlled-loop to achieve such

10 synchronization. However, when an ultor supply is energized by the flyback transformer, beam current variations may modulate a shape and a width of the transformer produced retrace pulse. Disadvantageously, the phase of a horizontal deflection current in a horizontal deflection winding may be offset or phase-shifted

15 relative to that of the flyback transformer produced flyback pulse. The result may be an inaccurate synchronization causing a visible, beam current dependent, horizontal picture shift or a raster bending in a horizontal direction. This undesired effect may be further aggravated when East-West (E-W) distortion raster

20 correction is utilized.

It may be desirable, instead of using the transformer produced retrace pulse, to use a retrace pulse developed in the horizontal deflection winding for the phasing of the deflection circuit to the video signal. To that end, it may be desirable to

25 have an end terminal of the horizontal deflection winding at a common conductor or ground potential, during retrace.

In a horizontal deflection circuit, embodying an aspect of the invention, one end terminal of the horizontal deflection winding is coupled to ground potential. A loose coupling is

30 provided between the flyback transformer and a retrace resonant circuit that includes the deflection winding. The grounded terminal of the deflection winding permits a more accurate phasing of the horizontal deflection winding retrace pulse to the video signal. The loose coupling reduces beam current dependent

35 phase modulation of the horizontal deflection current and also reduces generation of so-called "mouseteeth" type raster distortion. Mouseteeth distortion is described in detail in, for



example, U.S. Patent No. 4,634,937, entitled, EAST-WEST CORRECTION CIRCUIT, in the name of Haferl.

5 A television deflection apparatus, embodying an inventive feature, includes a source of a first input signal at a frequency that is related to a first deflection frequency. A retrace resonant circuit, includes a deflection winding and a first retrace capacitance. A supply inductance is coupled to a source of input supply voltage for generating a flyback pulse voltage in the supply inductance. A first switching arrangement is responsive to
10 the first input signal and coupled to the retrace resonant circuit and to the supply inductance for generating a deflection current in the deflection winding and a first retrace pulse voltage in the retrace resonant circuit during a retrace interval of a given deflection cycle. A source of a modulation second input signal is
15 provided. A second switching arrangement is responsive to the first and second input signals and coupled to the supply inductance and to the retrace resonant circuit for decoupling the supply inductance from the retrace resonant circuit during a controllable first portion of the first retrace pulse voltage that
20 varies in accordance with the second input signal. The flyback pulse voltage is developed at a first main current conducting terminal of the second switching means and is decoupled by the second switching means from the retrace resonant circuit. The first retrace pulse voltage is developed at a second main current
25 conducting terminal of the second switching means and is decoupled by the second switching means from the supply inductance.

FIGURE 1 illustrates a deflection circuit embodying an aspect of the invention that includes an outside pincushion
30 correction arrangement;

FIGURES 2a-2g illustrate waveforms useful in explaining the operation of the circuit of FIGURE 1; and

FIGURE 3 illustrates a deflection circuit embodying another aspect of the invention that includes outside and inside
35 pincushion correction arrangement.

A horizontal deflection circuit 250 of FIGURE 1, embodying an aspect of the invention, provides horizontal deflection in, for example, an FS color cathode ray tube (CRT) type



A66EAS00X01. Circuit 250 includes a switching transistor Q2 operating at a horizontal frequency f_H that is about 15.7 KHz in the NTSC standard and an anti-parallel damper diode DQ2, both being constructed as one integrated circuit. A series arrangement of retrace capacitors C2 and C3 is coupled in parallel with transistor Q2 and diode DQ2. A deflection winding L_H is coupled in series with an S-shaping trace capacitance C_s and with a linearity inductance L_{LIN} , forming a circuit branch that is coupled in parallel with each of transistor Q2, diode DQ2 and series coupled retrace capacitors C2 and C3, to form a retrace resonant circuit 100, during horizontal retrace.

A phase control stage 101 that includes a horizontal oscillator and a phase detector, not shown in detail in FIGURE 1, is responsive to a horizontal synchronizing signal H_s . Signal H_s is derived from, for example, a video detector of a television receiver, not shown in the FIGURES and is referenced to a common conductor or ground potential. Capacitors C2 and C3 form a voltage divider to obtain a sample, low amplitude retrace voltage V4a that is referenced to the common conductor or ground. Voltage V4a is applied via a coupling network 101b to a second input 101a of stage 101 to synchronize retrace pulse voltage V4 to synchronizing signal H_s . Stage 101 applies, via a conventional driver stage 102, a switching voltage V1 to the base-emitter junction of transistor Q2 for producing a base drive current at the horizontal frequency f_H . Voltage V1 is also referenced to the common conductor or ground potential.

A switched raster distortion correction circuit 200, embodying a feature of the invention, includes an E-W control circuit 300 that controls switching timing of a bipolar, switching transistor Q1 of a flyback circuit 251. A primary winding W1 of a flyback transformer T1 of circuit 251 is coupled between a source of a B+ voltage and a collector of switching transistor Q1. A flyback capacitor C1 is coupled to a junction terminal W1a, between transistor Q1 and winding W1, to form with winding W1 a flyback resonant circuit 99 of circuit 251.

In carrying out an inventive feature, a secondary winding W2 of transformer T1 is coupled at a terminal W2a to a driver stage 201 of transistor Q1 to supply power to stage 201.



The emitter of transistor Q1 is coupled via a current limiting resistor R1 to the collector of transistor Q2 of circuit 250. An anti-parallel damper diode DQ1 is coupled between the collector and emitter of transistor Q1. A diode D1 having an anode that is coupled between terminal W1a of winding W2 and the collector of transistor Q1 and a cathode that is coupled to terminal W2a, together with winding W2, provides an inrush current path and over-voltage protection for E-W switching transistor Q1.

Resonant circuits 99 and 100 are parallel coupled by transistor Q1, during a controllable portion of the retrace interval to supply energy to deflection circuit 250. Resonant circuits 99 and 100 have the same resonant frequency, 44 KHz. Therefore, resonant circuits 99 and 100 can be coupled in parallel without changing the resulting resonant frequency of circuit 100.

FIGURES 2a-2g illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2g indicate similar items or functions. Transistors Q1 and Q2 of FIGURE 1 are in saturation during a trace interval, t_6-t_1' , as illustrated by waveforms of FIGURES 2a and 2d showing drive voltages V1 and V3, respectively. An upramping trace portion of a current i_1 of FIGURE 2c flows through series coupled transistors Q1 and Q2 of FIGURE 1 to ground. Deflection current i_3 of FIGURE 2g flows through transistor Q2 of FIGURE 1 to ground. Negative portions of currents i_1 and i_3 flow through the respective integrated diodes DQ1 and DQ2 of transistors Q1 and Q2.

Deflection transistor Q2 is turned off at time t_1 of FIGURE 2a to initiate a retrace interval t_1-t_6 . Current i_3 of FIGURE 1 flows then through capacitors C2 and C3 to produce retrace voltage V4, as shown in FIGURE 2f. A feedback path formed by a resistor R14 of FIGURE 1 couples voltage V4a in capacitor C3 to E-W control circuit 300. A diode D2 coupled across capacitor C3 clamps the trace portion of voltage V4a across capacitor C3 to ground potential. E-W control circuit 300 of FIGURE 1 generates a drive voltage V3 at the base of transistor Q1 to turn off transistor Q1 at a controllable instant that occurs during a portion of the retrace interval, interval t_2-t_3 of FIGURE 2d, as explained later on. The amplitude of retrace voltage V2 of



FIGURE 2b is regulated or stabilized by supply voltage B+ and is independent of variations in the state of conduction of transistor Q1. From time t1 of FIGURE 2e until transistor Q1 is turned off, current i2 in transistor Q1 replenishes energy losses in resonant circuit 100.

5 Flyback current i1 is split into a first portion, current i2, of FIGURE 2e, having a small amplitude, flowing through transistor Q1 and capacitors C2 and C3. The remaining portion of current i1 flows through capacitor C1. Current i2 is modulated by
10 the operation of transistor Q1 to obtain amplitude modulation of vertical rate, parabolic shaped envelope of retrace voltage V4 and of deflection current i3, required for correction of E-W raster distortion, as shown in the waveforms of FIGURES 2f and 2g at the right-hand side.

1.5 From top toward the center of the raster, the turn-off instant of transistor Q1 of FIGURE 1 is increasingly delayed, from time t2 to time t3 of FIGURE 2d. This causes an increasing amount of current i2 to flow into deflection circuit 250 to produce increasing amplitudes of retrace voltage V4 and of deflection
20 current i3 of FIGURES 2f and 2g, respectively. From the center to the bottom of the raster, the turn-off instant of transistor Q1 is increasingly advanced from time t3 to time t2 of FIGURE 2d. As a result, decreasing amounts of current i2 of FIGURE 2e flow into deflection circuit 250 of FIGURE 1 causing decreasing amplitudes
2.5 of voltage V4 and current i3. In this way beam positioning or pincushion distortion error is corrected.

During interval t4-t5 of FIGURE 2e, negative current i2 flows from deflection circuit 250 to flyback circuit 251. Negative current i2 is proportional to positive current i2. Energy losses in
30 circuit 250 are replenished in accordance with the sum of the positive and negative portions of current i2. The negative portion of current i2 is produced by negative current i1. Negative current i1 supplies retrace energy that circulates into winding W1 and is important for proper operation of deflection circuit 250 and for
3.5 high, or ultor voltage generation, produced via a tertiary winding W3 of transformer T1.

Control circuit 300 includes a driver transistor Q3 responsive to an E-W modulating current iD6 coupled via a diode



D6 from a differential amplifier, formed by transistors Q4 and Q5. A trace voltage across winding W2 is rectified via diode DQ1 of transistor Q1 that is coupled in series with diode D1 for producing a supply voltage across a capacitor C9 of about 40 volts, required for the operation of transistors Q3 and Q1 of circuit 300.

During flyback, a flyback voltage across winding W2 is voltage divided by capacitors C7 and C8 to obtain a flyback voltage V5 in capacitor C8 of about 35 volts peak-to-peak. An upramping portion of voltage V5, shown at the left side of FIGURE 1, is used for phase modulation of a leading edge of voltage V3, during interval t_2 - t_3 , shown in the FIGURE at the left side of FIGURE 1. A diode D5 and a resistor R5 couple voltage V5 in capacitor C8 to the base of transistor Q3 for providing a base current drive and determine, in part, by way of peak voltage rectification, a DC, average value of voltage V5.

Assume, for explanation purposes, a situation in which no current flows through diode D6. It follows that diode D5 discharges capacitors C7 and C8 until voltage V5 is smaller than a minimum, threshold voltage, REF, required for turning on transistor Q3, as shown in the waveforms of FIGURE 1. As a result, transistor Q3 remains turned off throughout retrace, voltage V3 remains positive that causes transistor Q1 to be conductive throughout retrace.

Increasing charge current i_{D6} that flows through diode D6, produced in a manner explained later on, level-shifts the entire waveform of voltage V5 closer toward threshold voltage REF. The retrace portion of voltage V5 that exceeds or crosses threshold voltage REF, produces a current that flows through diode D5 and resistor R5. The result is that transistor Q3 is switched into saturation and produces the leading edge of voltage V3 that turns off transistor Q1 at an instant that is controlled by the magnitude of current i_{D6} .

A capacitor C6 has a first terminal that is coupled between diode D5 and resistor R5 and a second terminal that is coupled to a collector terminal 250a of transistor Q2. During retrace, capacitor C6 charges approximately to the peak voltage of voltage V5 to supply a base drive current in transistor Q3 that keeps transistor Q3 saturated, until the end of retrace, as shown in



the waveform of voltage V6 of FIGURE 1. At the end of retrace, capacitor C6 discharges via a series arrangement of resistor R5, a diode D4, a capacitor C16, a resistor R17 and winding W2, at time t6 that produces the trailing edge of voltage V3 to turn-off transistor Q3.

During retrace, capacitor C16 is charged to a negative voltage via a diode D9 and a resistor R17. During trace, it is discharged via a diode D3, a resistor R4, a diode D4 and resistor R17 for reverse biasing the base-emitter of transistor Q3. Base current of transistor Q1 is supplied via series coupled resistors R2 and R3 to keep transistor Q1 in saturation during the trace interval. Thus, the turn-off instant of transistor Q1 is modulated by the amount of charge current i_{D6} flowing through diode D6. A higher charge current i_{D6} level-shifts voltage V5 in a positive direction and causes transistor Q1 to turn-off at earlier time t2. A smaller charge current i_{D6} increasingly delays the turn-off instant, toward later time t3.

The differential amplifier that includes transistors Q4 and Q5 generates current i_{D6} to charge capacitor C8. In the amplifier, a vertical rate parabolic, E-W drive voltage VP is applied to the base of transistor Q4, produced by a vertical deflection circuit 210 in a conventional manner. A feedback portion of voltage VQ5, developed in an integrating capacitor C13 at the base of transistor Q5, is coupled via a resistor R14 and an integrating capacitor 13 from voltage V4a in capacitor C3 and is indicative of a magnitude of deflection current i_3 . A second portion of voltage VQ5 is developed via a resistor R15 from circuit 210 to provide trapeze correction. Charge current i_{D6} that varies in a vertical rate is supplied via the collector of transistor Q4 and via diode D6, only during the trace interval, when transistor Q2 is saturated and voltage V4 is zero.

Diodes D7 and D8, coupled in series, limit the voltage across a capacitor C12 coupled in parallel with a collector load resistor R12 of transistor Q4. Therefore, diodes D7 and D8 also limit voltage V5 across capacitor C8 to prevent transistor Q3 from being turned on prior to time t1, when the leading portion of voltage V2 occurs. Diode D6 is nonconductive, during retrace, to isolate the low voltage differential amplifier, formed by



transistors Q4 and Q5 from retrace pulse V4 on which voltage V5 is superimposed. Thus, capacitor C8 is charged during trace for establishing the turn-off instant of transistor Q1, during retrace.

Transistors Q1 and Q2 are protected against excessive
5 currents by resistor R1, and by a series arrangement of diode D3 and resistor R4, that is coupled between the base of transistor Q3 and a junction terminal, between resistor R1 and transistor Q1. When a voltage across current sampling resistor R1 that is coupled
10 in series with transistors Q1 and Q2 exceeds the sum of the forward voltages of diode D3 and of the base-emitter junction of transistor Q3, transistor Q3 turns on and reduces the current flow in transistors Q1 and Q2. Deflection linearity is, advantageously, not degraded by resistor R1 because resistor R1 is outside deflection circuit 250.

15 Transistor Q1 operates in a common base mode during current inrush. When the B+ voltage is initially applied to the circuit, transistor Q3 is in cut off. Consequently, the base of transistor Q1 is coupled to the B+ voltage via resistors R3 and R2, winding W2, diode D1 and winding W1. When transistor Q2 starts
20 the switching operation, transistor Q1 conducts in common base mode until a rectified trace voltage, developed across a capacitor C9, supplies sufficient base current via resistors R2 and R3 to keep transistor Q1 in saturation.

The circuit that includes diode D1, winding W2 and
25 capacitor C9 is coupled between the collector and emitter of transistor Q1. When a flyback voltage across transistor Q1 exceeds a sum of the voltages across capacitor C9 and across winding W2, that is 350 volts, flyback current flows through diode D1, winding W2 and capacitor C9 into deflection circuit 250. This
30 causes an increase of voltage V4 and subsequently a limitation of the collector-emitter voltage of transistor Q1 to 350 volts. Thus the E-W control range is limited by such over-voltage protection circuit. Advantageously, the over-voltage protection for transistor Q1 allows the use of a transistor with a lower voltage rating than
35 transistor Q2.

The total flyback capacitance of flyback transformer T1 includes capacitor C1 and capacitor C7. A capacitor C5 coupled between the dotted terminals of windings W1 and W2, terminal



W1a, does not contribute to the flyback time because the flyback voltage across capacitor C5 is low. It has been found, however, that capacitor C5, advantageously, reduces an output impedance of an ultor voltage supply 220, energized by winding W3, at a high beam current i_{BEAM} .

FIGURE 3 illustrates a deflection circuit embodying another aspect of the invention that is similar to that in FIGURE 1, with the differences noted below. Similar symbols and numerals in FIGURES 1, 2a-2g and 3 indicate similar items or functions.

The arrangement of FIGURE 3 provides horizontal deflection in a CRT, Philips 45AX type A66EAK00X01, which requires both outside and inside pincushion correction. An inside pincushion correction circuit 240 includes a coil L1 that may be variable for adjustment purposes, a capacitor C15 and a retrace capacitor C14. Series coupled coil L1 and capacitor C15 form an arrangement that is parallel coupled to capacitor C_s , during the trace interval via transistor Q1. Coil L1, capacitor C_s and capacitor C15 form a trace resonant circuit that is tuned to, for example, 12-14 KHz, that is higher than the trace resonance frequency, of about 6 KHz of winding L_H and capacitor C_s . Thus, a current i_4 in coil L1 has a higher degree of "S" shaping than deflection current i_3 , as shown in the waveform of current i_4 in FIGURE 3. Current i_4 is generated by a voltage V7 developed across capacitor C_s . Current i_4 is modulated by the retrace voltage across transistor Q1. This retrace voltage is the difference between voltages V2 and V4 and, therefore, is amplitude modulated by the outside pincushion circuit of FIGURE 1. Retrace voltage V4 of FIGURE 3 is of opposite phase to voltage V7, resulting in a modulation of current i_4 and of voltage V7. Thus, a low flyback voltage across transistor Q1 produces an increased amplitude of each of current i_4 and voltage V7 and, in turn, more "S"-shaping of deflection current i_3 . Similarly, less "S"-shaping is obtained at a higher amplitude of the retrace voltage across transistor Q1. Retrace capacitor C14 provides a current path for current i_4 during retrace to prevent increased coupling between flyback transformer T1 and deflection circuit 250.

The circuits of FIGURES 1 and 3 may be modified for operation at a horizontal deflection frequency $2xf_H$. In this case,



an MOS transistor, instead of a bipolar transistor, may be utilized as transistor Q1. Advantageously, mooseteeth distortions are reduced in the circuits of FIGURES 1 and 3. This is so because by decoupling circuits 250 and 251 of, for example, FIGURE 1, during
5 a significant portion of retrace, transistor Q1 reduces beam current dependent energy transfer from deflection circuit 250 back to deflection circuit 251.

In accordance with another inventive feature, transistor Q1 is coupled between resonant circuits 99 and 100
10 such that the collector of transistor Q1 is coupled to resonant circuit 99 via a current path section Q1a that excludes the emitter of transistor Q1; whereas the emitter of transistor Q1 is coupled to resonant circuit 100 via a current path section Q1b that excludes the collector of transistor Q1 and the common conductor. The
15 result is that when, during retrace, transistor Q1 is nonconductive, resonant circuits 99 are decoupled from each other by transistor Q1. Therefore, advantageously, when transistor Q1 is nonconductive, resonant circuit 99 does not cause a distortion in the waveform of pulse voltage V4a in capacitor C3.

20 The waveform of voltage V4a in capacitor C3 is coupled to input terminal 101a of stage 101 via network 101b in a manner that bypasses transformer T1. Both capacitor C3 and stage 101 are referenced to the common conductor. Thus, by decoupling circuits 250 and 251, the waveform at terminal 101a
25 is not distorted by beam current loading in transformer T1 and E-W modulation and, hence, more accurately represents the timings of deflection current i3 to provide more accurate phasing or synchronization in stage 101.

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WHAT IS CLAIMED IS:

1. A television deflection apparatus, comprising:
 - a source of a first input signal (H_S) at a frequency that is related to a first deflection frequency;
 - a retrace resonant circuit (100), including a deflection winding (LH) and a first retrace capacitance (C2);
 - a source of an input supply voltage (B+);
 - a supply inductance (W1) coupled to said source of input supply voltage for developing at least a portion of a flyback pulse voltage (V2) in said supply inductance;
 - first switching means (Q2) responsive to said first input signal and coupled to said retrace resonant circuit and to said supply inductance for generating a deflection current (C3) in said deflection winding and for developing at least a portion of a first retrace pulse voltage (V4) in said retrace resonant circuit during a retrace interval of a given deflection cycle;
 - a source (LV) of a modulation second input signal (VP); and characterized in that
 - second switching means (Q1) responsive to said first and second input signals and coupled to said supply inductance and to said retrace resonant circuit for decoupling said supply inductance from said retrace resonant circuit and to develop said flyback pulse voltage at a first main current conducting terminal (collector of Q1) of said second switching means and said first retrace pulse voltage at a second main current conducting terminal (emitter of Q2) of said second switching means, during a controllable first portion (t_3 - t_6) of said first retrace pulse voltage that occurs when said supply inductance and said retrace resonant circuit are decoupled, the controllable first portion of said first retrace pulse voltage varying in accordance with said second input signal.
2. An apparatus according to Claim 1 characterized in that said first main current conducting terminal (collector of Q1) of said second switching means (Q1) is coupled to said supply inductance (W1) at a point (W1a) remote from said retrace resonant circuit (100), and said second main current conducting terminal (emitter) of said second switching means is coupled to





said retrace resonant circuit at a point (250a) remote from said supply inductance.

3. An apparatus according to Claim 1 characterized in that said second switching means (Q1) forms, during said first portion (t3-t6), a high impedance that is interposed between said supply inductance (W1) and said retrace resonant circuit (100).

4. An apparatus according to Claim 1 characterized by, a flyback capacitance (C1) coupled to said supply inductance (W1) to form a flyback resonant circuit (251) that is coupled via said second switching means (Q1) to said deflection winding (LH) during a second portion (t1-t3) of said first retrace pulse voltage (V4).

5. An apparatus according to Claim 4 characterized in that said resonant circuits (100, 251) have, each, substantially equal resonance frequencies.

6. An apparatus according to Claim 4 characterized in that a resonance frequency of a combined resonant circuit that includes said supply inductance (W1), said deflection winding (LH) said first retrace capacitance (C2) and said flyback capacitance (C1) is substantially the same as that of said retrace resonant circuit (100), alone.

7. An apparatus according to Claim 1 characterized in that said supply inductance (W1) comprises a primary winding of a flyback transformer (T1) having a second winding (W3) that is coupled to an ultor voltage power supply (220) that is energized by a high voltage developed in said second winding of said transformer, said ultor voltage power supply forming a load that varies in accordance with a beam current (i_{BEAM}) variation.

8. An apparatus according to Claim 1 characterized in that said second switching means (Q1) operates in a conductive state during a first portion (t3-t6) of said first retrace pulse





voltage (V4) and in a nonconductive state during said first portion (t1-t3) of said first retrace pulse voltage.

9. An apparatus according to Claim 8 characterized in that said second portion (t1-t3) precedes said first portion during a given retrace interval (t1-t6).

10. An apparatus according to Claim 8 characterized in that a retrace resonance frequency of said retrace resonant circuit (100) is maintained substantially the same when said second switching means (Q1) is conductive and when said second switching means is nonconductive.

11. An apparatus according to Claim 1 characterized in that said supply inductance (W1) comprises a winding of a flyback transformer (T1) that is decoupled from said retrace resonant circuit (100) by said second switching means (Q1) when said second switching means is nonconductive and that is coupled through said second switching means to said retrace resonant circuit when said second switching means is conductive.

12. An apparatus according to Claim 1 characterized by, a phase-control-stage (101) responsive to said first input signal (H_S) and to a feedback retrace pulse voltage (V4a) that is coupled from said retrace resonant circuit (100) in a manner that bypasses said supply inductance (W1).

13. An apparatus according to Claim 1 characterized in that said second switching means (Q1) is coupled in series with said first switching means (Q2) during a trace portion (t6-t1') of said given deflection cycle.

14. An apparatus according to Claim 1 characterized by, a trace capacitance (C_S) that is coupled to said deflection winding (LH) to form a first trace resonant circuit during a trace interval (t6-t1') of said deflection cycle and a second trace resonant circuit (240, Fig. 3) that is coupled to said trace capacitance to provide an inside pincushion distortion correction.





15. An apparatus according to Claim 1 characterized in that each of said first (Q2) and second (Q1) switching means operates at a horizontal rate and wherein said second switching means becomes nonconductive, within said retrace interval, at an instant that varies at a vertical rate parabolic manner that provides pincushion distortion correction.

16. An apparatus according to Claim 1 characterized by, means (Q4, Q5) responsive to a signal at a vertical rate (VP) for producing a control signal (V3) at a control terminal (base) of said second switching means (Q1) such that a phase of said control signal varies in accordance with said vertical rate signal.

17. An apparatus according to Claim 1 characterized by, a second retrace capacitance (C3) that is coupled in series with said first retrace capacitance (C2) to develop in said second retrace capacitance a second retrace pulse voltage (V4a) and a phase-control stage (101) having an input (101a) coupled between said retrace capacitances in a manner that bypasses said supply inductance (W1).

18. An apparatus according to Claim 1 characterized by, a control circuit (200) that is referenced to a junction terminal (250a) between said first (Q2) and second (Q1) switching means for generating a control signal (V3) at a control terminal (base) of said second switching means wherein, during a trace interval (t6-t1') of said deflection cycle, said junction terminal is at a constant potential and wherein, during said retrace interval (t1-t6), a retrace voltage (V4) is developed at said junction terminal.

19. An apparatus according to Claim 1 characterized by, a load circuit (220) coupled to said supply inductance (W1) and energized by said flyback pulse voltage (V2) wherein said second switching means (Q1) forms a high impedance that reduces mouseteeth distortions by reducing energy transfer from said





retrace resonant circuit (100) to said load circuit, during said retrace interval (t1-t6).

20. An apparatus according to Claim 1 characterized by, means (101) responsive to said first input signal (H_S) and to said first retrace pulse voltage (V_4) for generating a control signal (V_1) that is coupled to a control terminal (base) of said first switching means (Q_2) to form a phase-control-loop, wherein said second switching means (Q_1) decouples said flyback pulse voltage (V_2) from said control signal generating means.

21. An apparatus according to Claim 20 characterized in that said first retrace pulse voltage (V_4 , V_{4a}) is referenced to a reference potential (GROUND) of said control signal generating means (101).

22. An apparatus according to Claim 1 characterized in that said first (Q_2) and second (Q_1) switching means are coupled in series, during a portion (center of trace to t1') of a trace interval of said deflection cycle and wherein said supply inductance (W_1), said second switching means (Q_1) and said retrace resonant circuit (100) are coupled in series during a second portion (t1-t3) of said first retrace pulse voltage (V_4).

23. An apparatus according to Claim 1 characterized in that said second switching means (Q_1) decouples said first retrace pulse voltage (V_4) from said supply inductance (W_1) and said flyback pulse voltage (V_2) from said retrace resonant circuit (100), during said controllable first portion (t3-t6) of said retrace pulse voltage.

24. A deflection apparatus with beam positioning error correction, comprising:

a source of a first input signal (H_S) at a frequency that is related to a horizontal deflection frequency;

a retrace resonant circuit (100) including a deflection winding (LH) and a retrace capacitance (C_2);





a first transistor switch (Q2) responsive to said first input signal and coupled to said retrace resonant circuit for generating a horizontal deflection current (i3) in said deflection winding and a retrace pulse voltage (V4) in said retrace resonant circuit;

a flyback resonant circuit (251) including a supply inductance (W1) for generating a flyback pulse voltage (V2) in said supply inductance;

a source of a second input signal (LV) at a frequency that is related to a vertical deflection frequency;

means (Q4, Q5) responsive to said first and second input signals for generating a control signal (V3) at a horizontal frequency that varies in accordance with said vertical deflection frequency; characterized by

a second transistor switch (Q1), coupled in series with said first transistor switch (Q2) during a trace interval (t6-t1') of a given cycle of said horizontal deflection current, said second transistor switch coupling said resonant circuits during a first period (t1-t3) of said deflection cycle and decoupling said resonant circuits during a portion (t3-t6) of a retrace interval of said deflection cycle, the retrace interval portion varying in accordance with said control signal, such that during said retrace interval portion, said flyback pulse voltage is developed at a first main current conducting terminal (collector) of said second transistor switch and said retrace pulse voltage is developed at a second main current conducting terminal (emitter) of said second transistor switch.

25. An apparatus according to Claim 24 characterized by, a protection circuit (D1) responsive to a voltage (V2) that is developed across said second transistor switch for generating a current that causes an increase in an amplitude of said retrace pulse voltage (V4) when an over-voltage condition occurs in a manner to protect said second transistor switch (Q1) against said over-voltage condition.

26. A television deflection apparatus, comprising:





a source of a first input signal (H_S) at a frequency that is related to a first deflection frequency;

a retrace resonant circuit (100), including a deflection winding (L_H) and a first retrace capacitance (C_2);

a source of an input supply voltage (B_+);

a supply inductance (W_1) coupled to said source of input supply voltage;

first switching means (Q_2) responsive to said first input signal and coupled to said retrace resonant circuit and to said supply inductance for generating a deflection current (13) in said deflection winding, a first retrace pulse voltage (V_4) in said first retrace capacitance, and a flyback pulse voltage (V_2) in said supply inductance during a retrace interval of a given deflection cycle;

a source of a modulation second input signal (LV);
characterized by

second switching means (Q_1) responsive to said first and second input signals and having a first main current conducting terminal (collector) that is coupled to said supply inductance via a current path section (Q_{1a}) that excludes a common conductor (GROUND) and a second main current conducting terminal (emitter) of said second switching means, said second main current conducting terminal being coupled to said retrace resonant circuit via another current path section (Q_{1b}) that excludes said common conductor and said first main current conducting terminal, the two current path sections and said second switching means coupling said supply inductance to said retrace resonant circuit during a first period (t_1 - t_3) of said first retrace pulse voltage, the first period of said first retrace pulse voltage varying in accordance with said second input signal, said second switching means decoupling said retrace resonant circuit from said supply inductance during a second period (t_3 - t_6) of said first retrace pulse voltage.

