

Semiconductor Structures, Memory Device Constructions, and Methods for Forming Semiconductor Structures

TECHNICAL FIELD

[0001] The invention pertains to semiconductor structures, memory device constructions, and methods for forming semiconductor structures.

BACKGROUND OF THE INVENTION

[0002] A continuing goal of semiconductor device application is to increase the level of device integration, or in other words to increase the density of devices across a supporting substrate. Methods for increasing the density can include decreasing the size of individual devices, and/or increasing the packing density of the devices (i.e., reducing the amount of space between adjacent devices). In order to develop higher levels of integration, it is desired to develop new device constructions which can be utilized in semiconductor applications, and to develop new methods for fabricating semiconductor device constructions.

[0003] A relatively common semiconductor device is a memory device, with a dynamic random access memory (DRAM) cell being an exemplary memory device. A DRAM cell comprises a transistor and a memory storage structure, with a typical memory storage structure being a capacitor. Modern applications for semiconductor devices can utilize vast numbers of DRAM unit cells. It would therefore be desirable to develop new semiconductor device constructions applicable for utilization in DRAM structures, and it would also be desirable to develop new methods for fabricating DRAM structures.

[0004] Although the invention was motivated from the perspective of improving DRAM structures and methods of forming such structures, the invention is not to be limited to such aspects. Rather, the invention is only limited by the accompanying claims as literally worded, without interpretive or other limiting reference to the specification and drawings, and in accordance with the doctrine of equivalents.

SUMMARY OF THE INVENTION

[0005] In one aspect, the invention encompasses a method of forming a semiconductor structure. A semiconductor substrate is provided, and first and second materials are formed over the substrate. The first and second materials are selectively

etchable relative to one another. The first material is formed to be a lattice, and the second material is formed to be repeating regions spaced from one another by segments of the lattice. The repeating regions form an array. The array has a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis. The second pitch is about twice as big as the first pitch. At least some of the first material of the lattice is replaced with one or more conductive materials of a gateline, and at least some of the second material is replaced with doped semiconductor material to form vertically-extending source/drain regions.

[0006] In one aspect, the invention encompasses a semiconductor structure. The structure includes a semiconductor substrate and a gateline lattice over the substrate. The lattice defines an array of non-gateline regions spaced from one another by segments of the lattice. The array has a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis. The second pitch is about twice as big as the first pitch. The non-gateline regions comprise vertically-extending source/drain regions.

[0007] In one aspect, the invention encompasses a memory device construction. The construction includes a semiconductor substrate, and a gateline over the substrate. The construction further includes a pair of vertically-extending source/drain regions over the substrate and at least partially surrounded by the gateline. One of the source/drain regions is a first source/drain region and consists essentially of conductively-doped epitaxial silicon, and the other source/drain region is a second source/drain region which consists essentially of conductively-doped silicon which is not epitaxial. The source/drain regions are gatedly connected to one another through the gateline. A memory storage device is electrically connected to either the first source/drain region or the second source/drain region. A digit line is electrically connected to whichever of the first and second source/drain regions is not electrically connected to the memory storage device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0009] Figs. 1-3 are a diagrammatic, fragmentary top view and cross-sectional side views of a semiconductor construction at a preliminary processing stage. Figs. 2

and 3 are along the lines 2-2 and 3-3, respectively, of Fig. 1; Fig. 3 is along the line 3-3 of Fig. 2; and Fig. 2 is along the line 2-2 of Fig. 3.

[0010] Figs. 4-6 are a diagrammatic, fragmentary top view and cross-sectional side views, respectively, of the fragments of Figs. 1-3, shown at a processing stage subsequent to that of Figs. 1-3. Figs. 5 and 6 are along the lines 5-5 and 6-6 of Fig. 4, respectively; Fig. 6 is along the line 6-6 of Fig. 5; and Fig. 5 is along the line 5-5 of Fig. 6.

[0011] Figs. 7-9 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 4-6. Figs. 8 and 9 are along the lines 8-8 and 9-9, respectively, of Fig. 7; Fig. 9 is along the line 9-9 of Fig. 8; and Fig. 8 is along the line 8-8 of Fig. 9.

[0012] Figs. 10-12 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3, shown at a processing stage subsequent to that of Figs. 7-9. Figs. 11 and 12 are along the lines 11-11 and 12-12, respectively, of Fig. 10; Fig. 12 is along the line 12-12 of Fig. 11; and Fig. 11 is along the line 11-11 of Fig. 12.

[0013] Figs. 13-15 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 10-12. Figs. 14 and 15 are along the lines 14-14 and 15-15 of Fig. 13; Fig. 15 is along the line 15-15 of Fig. 14; and Fig. 14 is along the line 14-14 of Fig. 15.

[0014] Figs. 16-17 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at processing stage subsequent to that of Figs. 13-15. Figs. 17 and 18 are along the lines 17-17 and 18-18, respectively, of Fig. 16; Fig. 18 is along the line 18-18 of Fig. 17; and Fig. 17 is along the line 17-17 of Fig. 18.

[0015] Figs. 19-21 are a diagrammatic, fragmentary top view and cross-sectional side views, respectively, of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 16-18. Figs. 20 and 21 are along the lines 20-20 and 21-21, respectively, of Fig. 19; Fig. 21 is along the line 21-21 of Fig. 20; and Fig. 20 is along the line 20-20 of Fig. 21.

[0016] Figs. 22-24 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 19-21. Figs. 23 and 24 are along the lines 23-23 and 24-24

of Fig. 22; Fig. 24 is along the line 24-24 of Fig. 23; and Fig. 23 is along the line 23-23 of Fig. 24.

[0017] Figs. 25-27 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 21-23. Figs. 26 and 27 are along the lines 26-26 and 27-27, respectively, of Fig. 25; Fig. 27 is along the line 27-27 of Fig. 26; and Fig. 26 is along the line 26-26 of Fig. 27.

[0018] Figs. 28-30 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 24-26. Figs. 29 and 30 are along the lines 29-29 and 30-30 of Fig. 28; Fig. 30 is along the line 30-30 of Fig. 29; and Fig. 29 is along the line 29-29 of Fig. 30.

[0019] Figs. 31-33 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 27-29. Figs. 32 and 33 are along the lines 32-32 and 33-33, respectively, of Fig. 31; Fig. 33 is along the line 33-33 of Fig. 32; and Fig. 32 is along the line 32-32 of Fig. 33.

[0020] Fig. 34 is a diagrammatic, cross-sectional side view of the construction of Fig. 32 drawn to show structures typically comprising the same composition as one another merged into a single structure to simplify the drawing. The diagrammatic representation of Fig. 34 is utilized in the figures following Fig. 34.

[0021] Figs. 35-37 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 31-33. Figs. 36 and 37 are along the lines 36-36 and 37-37, respectively, of Fig. 35; Fig. 37 is along the line 37-37 of Fig. 36; and Fig. 36 is along the line 36-36 of Fig. 37.

[0022] Figs. 38-40 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at processing stage subsequent to that of Figs. 35-37. Figs. 39 and 40 are along the lines 39-39 and 40-40 of Fig. 38; Fig. 40 is along the line 40-40 of Fig. 39; and Fig. 39 is along the line 39-39 of Fig. 40.

[0023] Figs. 41-43 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 38-40. Figs. 42 and 43 are along the lines 42-42 and 43-43

of Fig. 41; Fig. 43 is along the line 43-43 of Fig. 42; and Fig. 42 is along the line of 42-42 of Fig. 43.

[0024] Fig. 44 is a diagrammatic view of the construction of Fig. 43 where structures which would typically have the same composition are shown merged with one another. The representation of Fig. 44 will be utilized in the figures that follow Fig. 44.

[0025] Figs. 45-47 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 41-43. Figs. 46 and 47 are along the lines 46-46 and 47-47 of Fig. 45; Fig. 47 is along the line 47-47 of Fig. 46; and Fig. 46 is along the line 46-46 of Fig. 47.

[0026] Figs. 48-50 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 45-47. Figs. 49 and 50 are along the lines of 49-49 and 50-50 of Fig. 48; Fig. 50 is along the line of 50-50 of Fig. 49; and Fig. 49 is along the line of 49-49 of Fig. 50.

[0027] Figs. 51-53 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 48-50. Figs. 52 and 53 are along the lines 52-52 and 53-53 of Fig. 51; Fig. 53 is along the line 53-53 of Fig. 52; and Fig. 52 is along the line 52-52 of Fig. 53.

[0028] Figs. 54-56 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 51-53. Figs. 55 and 56 are along the lines 55-55 and 56-56 of Fig. 54; Fig. 56 is along the line 56-56 of Fig. 55; and Fig. 55 is along the line 55-55 of Fig. 56.

[0029] Figs. 57-59 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 54-56. Figs. 58 and 59 are along the lines 58-58 and 59-59 of Fig. 57; Fig. 59 is along the line 59-59 of Fig. 58; and Fig. 58 is along the line 58-58 of Fig. 59.

[0030] Figs. 60-62 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 57-59. Figs. 61 and 62 are along the lines 61-61 and 62-62

of Fig. 60; Fig. 62 is along the line 62-62 of Fig. 61; and Fig. 61 is along the line 61-61 of Fig. 62.

[0031] Figs. 63-65 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 60-62. Figs. 64 and 65 are along the lines 64-64 and 65-65 of Fig. 63; Fig. 65 is along the lines 65-65 of Fig. 64; and Fig. 64 is along the line 64-64 of Fig. 65.

[0032] Fig. 66 is a diagrammatic top view of the construction of Fig. 64, shown with structures which would typically have the same composition as one another merging together to form common structures. The diagrammatic aspects of Fig. 66 will be used in the figures which follow Fig. 66.

[0033] Figs. 67-69 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 63-65. Figs. 68 and 69 are along the lines 68-68 and 69-69 of Fig. 67; Fig. 69 is along the line 69-69 of Fig. 68; and Fig. 68 is along the line 68-68 of Fig. 69.

[0034] Figs. 70-72 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 67-69. Figs. 71 and 72 are along the lines 71-71 and 72-72 of Fig. 70; Fig. 72 is along the line 72-72 of Fig. 71; and Fig. 71 is along the line 71-71 of Fig. 72.

[0035] Figs. 73-75 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 70-72. Figs. 74 and 75 are along the lines 74-74 and 75-75 of Fig. 73; Fig. 75 is along the line 75-75 of Fig. 74; and Fig. 74 is along the line 74-74 of Fig. 75.

[0036] Figs. 76-78 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 73-75. Figs. 77 and 78 are along the lines 77-77 and 78-78 of Fig. 76; Fig. 78 is along the line 78-78 of Fig. 77; and Fig. 77 is along the line 77-77 of Fig. 78.

[0037] Figs. 79-81 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 76-78. Figs. 80 and 81 are along the lines 80-80 and 81-81

of Fig. 79; Fig. 81 is along the line 81-81 of Fig. 80; and Fig. 80 is along the line 80-80 of Fig. 81.

[0038] Figs. 82-84 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 79-81. Figs. 83 and 84 are along the lines 83-83 and 84-84 of Fig. 82; Fig. 84 is along the line 84-84 of Fig. 83; and Fig. 83 is along the line 83-83 of Fig. 84.

[0039] Figs. 85-87 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 82-84. Figs. 86 and 87 are along the lines 86-86 and 87-87 of Fig. 85; Fig. 87 is along the line 87-87 of Fig. 86; and Fig. 86 is along the line 86-86 of Fig. 87.

[0040] Figs. 88-90 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 85-87. Figs. 89 and 90 are along the lines 89-89 and 90-90 of Fig. 88; Fig. 90 is along the line 90-90 of Fig. 89; and Fig. 89 is along the line 89-89 of Fig. 90.

[0041] Figs. 91-93 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 88-90. Figs. 92 and 93 are along the lines 92-92 and 93-93 of Fig. 91; Fig. 93 is along the line 93-93 of Fig. 92; and Fig. 92 is along the line 92-92 of Fig. 93.

[0042] Figs. 94-96 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 91-93. Figs. 95 and 96 are along the lines 95-95 and 96-96 of Fig. 94; Fig. 96 is along the line 96-96 of Fig. 95; and Fig. 95 is along the line 95-95 of Fig. 96.

[0043] Figs. 97-99 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 94-96. Figs. 98 and 99 are along the lines 98-98 and 99-99 of Fig. 97; Fig. 99 is along the line 99-99 of Fig. 98; and Fig. 98 is along the line 98-98 of Fig. 99.

[0044] Figs. 100-102 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage

subsequent to that of Figs. 97-99. Figs. 101 and 102 are along the lines 101-101 and 102-102 of Fig. 100; Fig. 101 is along the line 101-101 of Fig. 102; and Fig. 102 is along the line 102-102 of Fig. 101.

[0045] Figs. 103-105 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 100-102. Figs. 104 and 105 are along the lines 104-104 and 105-105 of Fig. 103; Fig. 105 is along the line 105-105 of Fig. 104; and Fig. 104 is along the line 104-104 of Fig. 105.

[0046] Figs. 106-108 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 103-105. Figs. 107 and 108 are along the lines 107-107 and 108-108 of Fig. 106; Fig. 108 is along the line 108-108 of Fig. 107; and Fig. 107 is along the line 107-107 of Fig. 108.

[0047] Figs. 109-111 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 106-108. Figs. 110 and 111 are along the lines 110-110 and 111-111 of Fig. 109; Fig. 110 is along the line 110-110 of Fig. 111; and Fig. 111 is along the line 111-111 of Fig. 110.

[0048] Figs. 112-114 are a fragmentary, diagrammatic top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 109-111. Figs. 113 and 114 are along the lines 113-113 and 114-114 of Fig. 112; Fig. 114 is along the line 114-114 of Fig. 113; and Fig. 113 is along the line 113-113 of Fig. 114.

[0049] Figs. 115-117 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 112-114. Figs. 116 and 117 are along the lines 116-116 and 117-117 of Fig. 115; Fig. 116 is along the line 116-116 of Fig. 117; and Fig. 117 is along the line 117-117 of Fig. 116.

[0050] Figs. 118-120 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 115-117. Figs. 119 and 120 are along the lines 119-119 and 120-120 of Fig. 118; Fig. 120 is along the line 120-120 of Fig. 119; and Fig. 119 is along the line 119-119 of Fig. 120.

[0051] Figs. 121-123 are a diagrammatic, fragmentary top view and cross-sectional side views of the construction of Figs. 1-3 shown at a processing stage subsequent to that of Figs. 118-120. Figs. 122 and 123 are along the lines 122-122 and 123-123 of Fig. 121; Fig. 123 is along the line 123-123 of Fig. 122; and Fig. 122 is along the line 122-122 of Fig. 123.

[0052] Fig. 124 is a diagrammatic, cross-sectional view of an exemplary memory device construction which can be formed in accordance with an aspect of the present invention.

[0053] Fig. 125 is a diagrammatic, cross-sectional view of another exemplary memory device construction which can be formed in accordance with an exemplary aspect of the present invention.

[0054] Fig. 126 is a diagrammatic, cross-sectional view of yet another exemplary memory device construction which can be formed in accordance with an exemplary aspect of the present invention.

[0055] Fig. 127 is a diagrammatic view of a computer illustrating an exemplary application of the present invention.

[0056] Fig. 128 is a block diagram showing particular features of the motherboard of the Fig. 127 computer.

[0057] Fig. 129 is a high-level block diagram of an electronic system according to an exemplary aspect of the present invention.

[0058] Fig. 130 is a simplified block diagram of an exemplary memory device according to an aspect of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0059] The invention includes methods by which a semiconductor construction is formed to comprise a gateline lattice surrounding a plurality of source/drain regions. In some aspects of the invention, such construction can be incorporated into a DRAM array by forming digit lines over and in electrical connection with some of the source/drain regions, and by also forming a plurality of capacitor constructions in electrical connection with some of the source/drain regions.

[0060] Exemplary aspects of the invention are described with reference to Figs. 1-123. Referring initially to Figs. 1-3, a semiconductor construction 10 is illustrated at a preliminary processing stage. Construction 10 comprises a substrate 12. Substrate 12 can comprise, consist essentially of, or consist of appropriately-doped monocrystalline

silicon. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0061] Construction 10 further comprises a material 14 over substrate 12. In particular aspects, material 14 can comprise, consist essentially of, or consist of silicon dioxide, and can be formed to a thickness of, for example, about 3,000Å.

[0062] A layer 16 is over material 14. Layer 16 can comprise, consist essentially of, or consist of silicon, such as, for example, polycrystalline silicon, and can be formed to a thickness of, for example, about 1,000Å. In particular aspects (discussed below) layer 16 can be patterned and utilized as a hard mask. Accordingly, layer 16 can be referred to as a "hard mask layer" in some aspects of the invention.

[0063] In specific aspects of the invention, the structures 12, 14 and 16 of construction 10 can be referred to as a first semiconductor material, oxide-containing material, and silicon-containing hard mask, respectively. In such aspects it is to be understood that material 14 can comprise silicon dioxide and/or any other suitable oxide, and that material 16 can comprise polycrystalline silicon or any other suitable form of silicon. Further, it is to be understood that other semiconductor materials (discussed below) will ultimately be formed over construction 10, and accordingly material 12 can be referred to as a first semiconductor material to distinguish material 12 from the subsequent semiconductor materials formed thereover.

[0064] Referring next to Figs. 4-6, a patterned masking material 18 is formed over layer 16. Masking material 18 can, for example, comprise, consist essentially of, or consist of photoresist, and can be photolithographically patterned into the shown configuration. The patterned material 18 is formed as a plurality of spaced lines 20, with such lines being separated from one another by gaps 22. There is a pitch 19 of the lines and gaps defined by the combined distance of a gap 22 and a line 18. The lines 20 can be considered to extend along a defined horizontal direction.

[0065] Referring next to Figs. 7-9, the pattern from patterned masking material 18 (Figs. 4-6) is transferred to hard mask layer 16. Specifically, gaps 22 are transferred through the hard mask layer to leave spaced lines 26 of the hard mask layer 16

remaining over material 14. Subsequently, the masking material 18 (Figs. 4-6) is removed. The lines 26 can be considered to extend along the same defined horizontal direction as the lines 20 (Figs. 4-6).

[0066] Referring next to Figs. 10-12, a thin layer of material 28 is formed over the lines 26 and within gaps 22 to narrow the gaps. Material 28 can, for example, comprise, consist essentially of, or consist of a nitride-containing material, such as, for example, silicon nitride. Material 28 can be formed to a thickness of, for example, about 160 Å. The lines 26 are shown in dashed-line view in Fig. 10 to indicate that the lines are beneath the material 28.

[0067] Referring next to Figs. 13-15, material 28 is patterned into spacers 30 with an anisotropic etch. After formation of the spacers 30, narrowed gaps 22 extend to an upper surface of material 14.

[0068] Referring next to Figs. 16-18, the narrowed gaps 22 are extended through material 14. Gaps 22 at the processing stage of Figs. 16-18 correspond to openings extending to an upper surface of substrate 12. The gaps are shaped as trenches longitudinally elongated along the horizontally-defined direction of the lines 20 of patterned mask 18 (Figs. 4-6).

[0069] Referring next to Figs. 19-21, spacers 32 are formed within openings 22 to narrow the openings. Spacers 32 can, for example, comprise, consist essentially of, or consist of a nitride-containing material, such as, for example, silicon nitride. Spacers 32 can be formed by providing a thin layer of nitride-containing material (such as, for example, a layer approximately 80Å thick of silicon nitride) over lines 26 and within openings 22, and subsequently utilizing an anisotropic etch to convert the layer to the shown spacers 32.

[0070] Spacers 32 and 28 together form spacer constructions 34. In some aspects, spacers 32 and 28 can be identical in composition to one another, and accordingly will merge together in the spacer constructions 34. The spacer constructions 34 narrow openings 22, and as can be seen in Fig. 19 form strips extending longitudinally in the horizontal direction along interior lateral peripheries of the trenches corresponding to openings 22.

[0071] Referring next to Figs. 22-24, openings 22 are extended into substrate 12 with a suitable etch. If substrate 12 comprises bulk silicon, the etch can be a dry etch. Such etch can extend openings 22 approximately 2,000Å into the substrate 12.

[0072] Masking layer 16 (Figs. 19-21) is removed at the processing stage of Figs. 22-24. Such removal can occur before, after or during the extension of openings 22 into substrate 12. Typically, the etch utilized to extend openings 22 into substrate 12 would be nonselective relative to material of layer 16, and accordingly layer 16 will be removed during the extension of the openings into substrate 12.

[0073] The removal of hard mask material 16 leaves gaps 36 over material 14 and between the spacers 34. Accordingly, spacers 34 can be considered to form paired lines on either side of openings 22, or alternatively can be considered to form paired lines on either side of gaps 36. For instance, Fig. 23 shows three of the spacers 34 labeled as 33, 35 and 37. Spacers 33 and 35 can be considered to form a pair of lines on opposing sides of the gap 22 extending between the spacers. Alternatively, spacers 35 and 37 can be considered to form a pair of lines on opposing sides of the gap 36 extending between the spacers.

[0074] After openings 22 are extended into substrate 14, the openings can be considered to comprise a first portion 38 extending within the semiconductor substrate 12, and a second portion 40 over the first portion.

[0075] Referring next to Figs. 25-27, dielectric material 42 is provided within the first portion 38 of openings 22 to fill the first portion, while leaving the second portion 40 of the openings not filled. Dielectric material 42 can, for example, comprise, consist essentially of, or consist of silicon dioxide. If substrate 12 comprises monocrystalline silicon, dielectric material 42 can be formed by oxidizing substrate 12. Suitable exemplary oxidation conditions are conditions which form oxide 42 to a thickness of about 100Å, which can be sufficient to fill the lower portions of the openings 22.

[0076] Referring next to Figs. 28-30, a material 44 is provided within gaps 22 and 36. The material fills gaps 22 and narrows gaps 36. Material 44 can, for example, comprise, consist essentially of, or consist of a nitride-containing material, such as, silicon nitride. Material 44 can be formed to a thickness of, for example, about 160Å.

[0077] Structures 34 are shown in dashed-line view in 28 to indicate that the structures are beneath material 44.

[0078] Referring next to Figs. 31-33, material 44 is subjected to an appropriate etch to form spaced pillars 46. The pillars 46 extend over material 14. Gaps 48 are between the spaced pillars and separate the pillars from one another. Gaps 48 are over oxide material 14, with each gap extending horizontally linearly along a horizontally-

extending line of the oxide material 14. Gaps 48 can be referred to as second gaps to distinguish the gaps from the gaps 22 discussed previously.

[0079] Referring next to Fig. 34, such shows construction 10 at the processing stage of Fig. 32, but shows components which are typically of similar composition to one another merging into single components. Specifically, the materials 28, 32 and 44 would typically all consist essentially of the same composition as one another (such as, for example, silicon nitride), and accordingly pillars 46 would homogeneously comprise a single material. Fig. 34 thus shows the pillars 46 comprising the same homogeneous material, with such material being indicated by the label 47. The representation of Fig. 34 will be used in the drawings that follow in order to simplify the drawings, but it is to be understood that the aspect represented by Fig. 34 is but one aspect of the invention, and the invention encompasses other aspects in which the materials 28, 32 and 44 are not all the same composition as one another.

[0080] Referring next to Figs. 35-37, gaps 48 are extended through material 14 with a suitable etch. In exemplary aspects, material 14 can consist essentially of silicon dioxide and material 47 can consist essentially of silicon nitride, and the etch can be a dry etch selective for silicon dioxide relative to silicon nitride. In some aspects of the invention, the processing described herein is utilized to form a DRAM array. In such aspects, it can be desired to protect a region peripheral to the array with photoresist or other suitable protective material during the etch utilized to extend openings 48 to substrate 12.

[0081] Referring next to Figs. 38-40, construction 10 is subjected to planarization (such as, for example, chemical-mechanical polishing) to planarize an upper surface of the construction. Such planarization removes material 47 from over material 14 to create resultant pillars 50 comprising planarized upper surfaces 51. Each of the pillars comprises a single line of material 47 sandwiched between a pair of lines of material 14. The lines extend along the horizontal direction, as can be seen in Fig. 38. The pillars 50 are separated from one another by the gaps 48.

[0082] Although upper surface 51 is shown at about the same elevational location as the original upper surface of material 14, it is to be understood that the planarization can remove some of material 14 so that surface 51 is below the original surface of 14 in some aspects of the invention. The height of the pillars 50 remaining after the chemical-mechanical polishing can be, in some aspects of the invention, about 5500Å.

[0083] Referring next to Figs. 41-43, a material 52 is deposited within gaps 48, and over pillars 50 (the pillars can also be referred to as lines, in that the pillars extend longitudinally in the horizontal direction). Material 52 can, for example, comprise, consist essentially of, or consist of a nitride-containing material, such as, for example, silicon nitride. In particular aspects of the invention, material 52 is provided to a thickness of about 200Å, which is sufficient to completely fill gaps 48. Layers 14 and 47 are shown in dashed-line view in Fig. 41 to indicate that such layers are beneath the material 52.

[0084] In particular aspects of the invention, materials 52 and 47 will comprise the same composition as one another, and accordingly will merge into a single structure. Such aspects are shown in Fig. 44, in which a single material 53 represents the combination of materials 52 and 47. Material 53 can, for example, comprise, consist essentially of, or consist of silicon nitride. The aspect of Fig. 44 will be utilized in the drawings following Fig. 44 in order to simplify the drawings. Accordingly, the drawings will utilize composition 53 in place of the compositions 47 and 52 (Fig. 42). However, it is to be understood that the invention encompasses aspects in which compositions 47 and 52 differ from one another. There is a repeating pattern in Fig. 44 comprised by pedestals 14 and the material 53 in the gaps between the pedestals, with such pattern defining a pitch 55 comprising the distance of one gap and one of the pedestals 14.

[0085] Referring to Figs. 45-47, a patterned masking material 54 is provided over material 53. Masking material 54 can comprise, for example, photoresist, and accordingly can be patterned by photolithographic processing. Patterned material 54 comprises a plurality of vertically-extending lines 56 which are spaced from one another by gaps 58.

[0086] The lines 56 and spaces 58 form a repeating pattern, with such pattern having a pitch 59 defined as the distance of one gap 58 and one line 56. In particular aspects of the invention, the pitch 59 and the pitch 19 (Fig. 5) will be about the same as one another, and the pitch 55 (Fig. 44) will be about one-half of the pitches 19 and 59.

[0087] Referring next to Figs. 48-50, gaps 58 are extended through materials 53 and 14, and subsequently masking layer 54 (Figs. 45-47) is removed. Such forms vertically-extending lines 60 from materials 14 and 53. Such lines can be considered to be separated from one another by vertically-extending trenches corresponding to the openings 58.

[0088] Referring next to Figs. 51-53, a material 62 is provided over lines 60 and within gaps 58. Material 62 can, for example, comprise, consist essentially of, or consist of silicon nitride, and can be formed to a thickness of about 375Å. Material 62 partially fills gaps 58 to narrow the gaps. Lines 60 are shown in dashed-line view in Fig. 51 to indicate that the lines are beneath material 62.

[0089] Referring next to Figs. 54-56, material 62 is anisotropically etched to form spacers 64. After formation of spacers 64, gaps 58 extend between the spacers to an upper surface of substrate 12.

[0090] Referring next to Figs. 57-59, openings 58 are extended into substrate 12 and subsequently a dielectric material 66 is formed within the openings. The openings can be extended into substrate 12 to a depth of, for example, about 2000Å. Dielectric material 66 can comprise, for example, silicon dioxide, and in applications in which substrate 12 comprises monocrystalline silicon can be formed by oxidizing silicon. The openings 58 can be considered to comprise a lower portion 68 and an upper portion 70, with the lower portion 68 being filled with dielectric material 66 and the upper portion 70 not being filled.

[0091] Referring next to Figs. 60-62, a material 72 is formed over lines 60 and within gaps 58. Material 72 can, for example, comprise, consist essentially of, or consist of an oxide-containing material, such as, for example, silicon dioxide. In exemplary aspects, material 72 is deposited to a thickness of about 350Å. The materials 53 and 62 are shown in dashed-line view in Fig. 60 to indicate that such materials are under material 72.

[0092] Referring next to Figs. 63-65, an upper surface of construction 10 is subjected to planarization to form the planarized upper surface 75. The planarization removes materials 72 and 53 from over upper surfaces of material 14. The planarization can also remove some of material 14 so that the planarized surface 75 is beneath the initial elevational level of the upper surface of material 14. The planarization can be accomplished by, for example, chemical-mechanical polishing, and can be conducted to leave upper surface 75 about 5500Å above an uppermost surface of substrate 12 in exemplary embodiments. After the planarization, the alternating layers 53 and 14 extend along a vertical direction and the alternating layers 14, 62 and 72 extend along a horizontal direction, as illustrated in the top view of Fig. 63.

[0093] In particular aspects, material 53 is (i.e. consists of) silicon nitride, material 14 is silicon dioxide, material 62 is silicon nitride, and material 72 is silicon

dioxide. Accordingly, the planarized surface 75 of Fig. 64 extends across alternating layers of silicon nitride and silicon oxide; and similarly the planarized upper surface 75 of Fig. 65 also extends across alternating surfaces of silicon dioxide and silicon nitride. This concept is illustrated in Fig. 66, which is a simplified top view at the processing stage of Fig. 63 where layers which would typically have the same composition as one another are shown merged together. Specifically, layers 53 and 62 would typically comprise the same composition as one another, and can, in particular aspects, comprise, consist essentially of, or consist of silicon nitride. Such layers are shown merged together in Fig. 66 to form a single structure 76. The materials 14 and 72 are shown extending through the structure 76. In particular aspects, materials 14 and 72 will comprise the same composition as one another, and can, for example, comprise, consist essentially of, or consist of silicon dioxide.

[0094] Materials 76 and 14 can, in some aspects, be materials which are selectively etchable relative to one another. In such aspects, material 76 can be considered a first material which is formed in a lattice, and material 14 can be considered to be a second material which is formed to be repeating regions spaced by segments of the lattice. The repeating regions 14 form an array, with such array having a first pitch 80 along the a first axis of the array (with the pitch 80 being shown along a vertically-elongated axis of the shown array), and having a second pitch 82 along a second axis which is substantially orthogonal to the first axis (with the shown second pitch being along a horizontally-extending axis of the array). The second pitch is about twice as big as the first pitch.

[0095] Although the invention is described with the first material 76 being silicon nitride and the second material 14 being silicon dioxide, it is to be understood that the materials can be reversed in other aspects of the invention. Accordingly, material 14 can comprise, consist essentially of, or consist of silicon nitride, and material 76 can comprise, consist essentially of, or consist of silicon dioxide.

[0096] The terms "horizontal" and "vertical" are utilized in reference to the top view of Fig. 66 to refer to axes which extend left-right across the page and up-down across the page, respectively. It is to be understood that the term "vertical" can also be utilized herein to refer to projections extending upwardly from a substrate, and accordingly the term "vertical" can be utilized in reference to the structure of, for example, Fig. 65 to refer to the projections 14, 62 and 72 as extending "vertically" from the upper surface of substrate 12. In order to avoid confusion introduced by using the

term "vertically" to refer to both a lateral direction and an elevational direction, the terms "elevationally vertically elongated" and "elevationally elongated" can be used herein to refer to projections extending upwardly from a surface (such as, for example, the projections 14, 62 and 72 of Fig. 65).

[0097] The simplified diagram of Fig. 66 will be utilized in the figures following Fig. 66 in order to simplify the discussion that follows. However, it is to be understood that the invention encompasses aspects in which materials 53 and 62 (Fig. 63) are different from one another so that the materials do not merge into the single common structure 76.

[0098] Referring next to Figs. 67-69, a masking material 84 is formed over regions 72 to protect the regions from subsequent processing (discussed below). Masking material 84 can comprise, for example, photoresist, and can be patterned utilizing photolithographic processing. The masking material 84 forms vertically-extending lines (or strips) in the top view of Fig. 67. The material 72 is shown in dashed-line view in Fig. 67 to indicate the material 72 is beneath masking material 84 in the shown view. The cross-sections of Figs. 68 and 69 have different labeling than those of Fig. 64 and 65, in that the label 76 is utilized to refer to the materials 53 and 62 of Figs. 64 and 65, to be consistent with the labeling convention described previously with reference to Fig. 66 and adopted in the figures following Fig. 66.

[0099] Referring next to Figs. 70-72, material 14 is selectively removed relative to material 76, and subsequently masking material 84 (Figs. 67-69) is removed. The removal of material 14 forms openings 86 extending through material 76 to an upper surface of substrate 12. If material 14 comprises silicon dioxide, and material 76 comprises silicon nitride, the selective removal of material 14 can be accomplished with, for example, a dry or wet oxide etch.

[00100] Referring next to Figs. 73-75, semiconductor material 88 is formed within openings 86. Material 88 can be formed by, for example, forming polycrystalline silicon within openings 86 and over material 76, and subsequently removing the polycrystalline silicon from over material 76 by planarization or other suitable methods. Alternatively, if substrate 12 comprises a monocrystalline semiconductive material (such as, for example, monocrystalline silicon), material 88 can be epitaxially grown from an upper surface of substrate 12. Epitaxially grown semiconductor material is generally single crystal material, whereas non-epitaxially grown semiconductor material is typically not

single crystal material. Rather, non-epitaxially grown semiconductor material is typically amorphous and/or polycrystalline.

[00101] Material 88 is shown having an uppermost surface which is elevationally below the uppermost surface of materials 76 and 72, but it is to be understood that the uppermost surface of material 88 can be coplanar with those of material 76 and 72, or can be elevationally above the surfaces of material 76 and 72, in various alternative aspects of the invention which are not shown.

[00102] Although all of the openings are shown simultaneously filled with material 88, it is to be understood that the openings can be divided into sets, with one set filled with semiconductor material 88 of one type and another set filled with semiconductor material 88 of another type. For instance, the semiconductor material 88 within openings 86 can ultimately correspond to source/drain regions, with some of the source/drain regions ultimately being connected to a digit line, and others of the source/drain regions ultimately being connected to memory storage devices (such as, for example, capacitors). The material 88 utilized in source/drain regions connected to digit lines can be one set and the material 88 utilized in source/drain regions connected to memory storage devices can be another set. Thus, the material 88 connected to digit lines can be a different semiconductor material than the material 88 connected to memory storage devices. For instance, the semiconductor material 88 ultimately connected to digit lines can be formed of epitaxial material, and the material 88 ultimately connected to memory storage devices can be formed of polycrystalline semiconductor material. P-n junctions in epitaxial silicon tend to be leakier than p-n junctions in bulk silicon, which can be advantageous in some aspects of the invention. Such aspects are discussed in more detail below relative to Figs. 124-126.

[00103] The semiconductor material 88 can be conductively doped either as-deposited (i.e., can be *in situ* doped), and/or can be doped subsequent to the deposition with one or more suitable implants. Also, regions of substrate 12 proximate openings 86 can be appropriately conductively doped either prior to provision of material 88 within the openings, or after provision of material 88 with suitable implants and/or out-diffusion of dopant from material 88. In some aspects, substrate 12 will have appropriate conductivity-enhancing dopants provided therein at a processing stage prior to that of Figs. 1-3, and specifically prior to formation of material 14 over the substrate. In alternative, or additional, aspects dopant will be provided in the substrate after the formation of openings 86 so that the dopant is self-aligned to the openings. Particular

dopants that can be provided within substrate 12 and regions 88 in particular aspects of the invention are discussed below with reference to Figs. 124-126.

[00104] In exemplary aspects of the invention, material 88 comprises, consists essentially of, or consists of epitaxially-grown silicon which is *in-situ* doped during the growth of the silicon, and which is grown to a thickness (i.e., a vertical height in Figs. 74 and 75) of about 1400Å.

[00105] Referring next to Figs. 76-78, material 76 (Figs. 73-75) is removed to leave openings 90. The openings extend between the vertical lines of material 72 and around the pillars of material 88. The openings 90 extend to the upper surface of substrate 12, and also to the upper surface of the dielectric material 42 formed within substrate 12.

[00106] The removal of material 76 is preferably selective for material 76 relative to materials 88 and 72 (with the term "selective" indicating that the conditions for removal of material 76 remove the material at a faster rate than such conditions remove materials 88 and 72, which can include, but is not limited to, aspects in which the rate of removal of materials 88 and 72 is about zero). In aspects in which material 76 consists of silicon nitride, material 88 consists of conductively-doped silicon, and material 72 consists silicon dioxide, the selective removal of material 76 can comprise a dry and/or wet etch of silicon nitride.

[00107] Referring next to Figs. 79-81, a dielectric layer 92 is formed within openings 90, and specifically is formed over exposed surfaces of material 88 and substrate 12. Pedestals 88 are shown in dashed-line view in Fig. 79 to indicate that such pedestals are beneath the dielectric material 92 in such view.

[00108] If material 88 and substrate 12 comprise silicon, dielectric material 92 can comprise silicon dioxide and can be formed by oxidation of surfaces of substrate 12 and material 88. Dielectric 92 can thus comprise, consist essentially of, or consist of silicon dioxide. In the aspect of Figs. 79-81, dielectric material 92, material 42, material 72 and material 66 are shown comprising the same composition as one another and merging into a common dielectric structure. Materials 92, 42, 72 and 66 would typically all comprise, consist essentially of, or consist of silicon dioxide. The merging of materials 92, 42, 72 and 66 simplifies the drawings, and such merging will be shown in the drawings following Figs. 79-81, but it is to be understood that the invention also encompasses aspects in which one or more of materials 92, 42, 72 and 66 has a different composition than the others.

[00109] Dielectric material 92 can ultimately be utilized as a gate oxide, and in such aspects of the invention can be formed to a thickness of about 70Å.

[00110] Referring next to Figs. 82-84, gateline material 94 is formed within openings 90. Although material 94 is illustrated as being homogeneous in the figures, it is to be understood that the structure represented by the label "94" can comprise a plurality of different layers. In particular aspects, material 94 can comprise, consist essentially of, or consist of metal, metal alloys and/or conductively-doped silicon. It can be preferred that material 94 comprise, consist essentially of, or consist of conductively-doped polycrystalline silicon in some aspects of the invention. Material 94 is shown only partially filling openings 90, but it is to be understood that the invention encompasses other aspects (not shown) in which material 94 completely fills the openings. In an exemplary aspect, material 94 comprises conductively-doped polycrystalline silicon which is initially deposited to 300Å thickness. Such thickness can be sufficient to completely fill openings 90 as the width of the openings is less than 600Å. Thus, the polysilicon deposited to a thickness of 300Å can form vertical pedestals within the openings having a height of 2000Å or more. The polycrystalline silicon is then etched back with a dry etch so that the silicon within the openings 90 only extends to an upper elevational level of about 850Å.

[00111] The gateline material 94 gatedly connects source/drain regions of pairs of pedestals of material 88 to form transistor constructions. A pair of pedestals which can be gatedly connected to one another and incorporated into a single transistor construction are identified by the label 89 in Fig. 83.

[00112] Referring next to Figs. 85-87, construction 10 is subjected to appropriate conditions which remove exposed portions of material 72 and of dielectric 92. In exemplary aspects, both material 72 and dielectric 92 consist of silicon dioxide, and the conditions utilized to remove exposed portions of material 72 and dielectric 92 are a wet oxide etch which removes about 150Å of oxide. The removal of the dielectric material from over pedestals 88 exposes upper surfaces of the pedestals.

[00113] Referring next to Figs. 88-90, a second dielectric material is formed over gateline material 94 and exposed surfaces of pedestals 88. In particular aspects, the second dielectric material comprises the same composition as first dielectric material 92 (Figs. 85-87). For instance, the first and second dielectric materials can both comprise, consist essentially of, or consist of silicon dioxide. The second dielectric material is shown comprising the same composition as material 92, and accordingly the two

dielectric materials merge to form a single dielectric material 98. In aspects in which the second dielectric material consists essentially of silicon dioxide, material 88 comprises silicon and material 94 comprises silicon, the second dielectric material can be formed by oxidation of exposed surfaces of materials 88 and 94. In such aspects, the second dielectric material can consist of silicon dioxide formed to a thickness of about 70Å. The material 98 comprising the combined first and second dielectric materials can consist of silicon dioxide and have a thickness of about 70Å throughout.

[00114] In particular aspects of the invention, pedestals 88 are vertically-elongated source/drain regions (specifically, elevationally vertically elongated), and material 94 is a gateline extending around the source/drain regions. It is noted that dielectric material 98 and gateline material 94 of Figs. 88-90 have together replaced the first material 76 of Fig. 66, and vertically-elongated source/drain regions 88 have replaced the second material 14 of Fig. 66. Accordingly, the gateline material 94 of Figs. 88-90 now forms a lattice comparable to the lattice formed by material 76 of Fig. 66, and the source/drain regions 88 form an array with repeating regions spaced from one another by segments of the lattice. The array has the first pitch along a first axis discussed with reference to Fig. 66, and the second pitch along a second axis orthogonal to the first axis, with the second pitch being about twice as big as the first pitch. In particular aspects, the first material 76 is silicon nitride and the second material 14 is non-nitride material (for example, silicon dioxide), and accordingly the invention encompasses replacing at least some of the silicon nitride lattice with one or conductive materials of a gateline, and replacing at least some of the non-nitride regions within the lattice with doped semiconductor material to form vertically-extending source/drain regions. In other aspects of the invention, the composition of the lattice 76 and the spaced regions 14 can be reversed, so that the lattice of Fig. 66 is silicon dioxide and the spaced regions 14 are non-oxide materials (for example, silicon nitride). In such aspects, at least some of the silicon dioxide lattice can be replaced with one or more conductive materials of the gateline, and at least some of the non-oxide regions 14 can be replaced with vertically-extending source/drain regions.

[00115] In the aspect of the invention of Figs. 66-90, spaced regions 14 of Fig. 66 are replaced with source/drain material before the lattice material 76 is replaced with gateline material. It is to be understood, however, that the invention encompasses other aspects in which the lattice is replaced with one or more gateline materials before the regions 14 are replaced with source/drain materials.

[00116] Referring next to Figs. 91-93, an electrically insulative capping material 100 is formed over the dielectric material 98. Capping material 100 can comprise any suitable electrically insulative material, and in particular aspects will comprise, consist essentially of, or consist of silicon nitride. Such silicon nitride can be formed to a thickness of, for example, about 200Å. The materials 72 and 88 are shown in dashed-line view in Fig. 91 to indicate that such regions are below other materials in the shown view.

[00117] Referring next to Figs. 94-96, material 100 is subjected to a spacer etch which forms spacers 102 and openings 104 extending between the spacers.

[00118] Referring next to Figs. 97-99, an electrically insulative material 106 is formed over the spacers 102 of material 100, and within openings 104. Material 106 can comprise, consist essentially of, or consist of, for example, silicon dioxide, and can be formed to a thickness of, for example, about 500Å.

[00119] Referring next to Figs. 100-102, an upper surface of construction 10 is planarized to remove materials 106 and 98 from over upper surfaces of pedestals 88, and to thereby expose the upper surfaces of pedestals 88. The planarization of material 106 forms a planarized surface 107. The planarization can be accomplished by, for example, chemical-mechanical polishing, and can be conducted down to an elevational level of about 4300Å above the uppermost surface of substrate 12. The materials 106 and 98 can be identical to one another, and in particular aspects can both be silicon dioxide.

[00120] Referring next to Figs. 103-105, a dielectric material 110 is formed over planarized surface 107 and a patterned masking material 112 is formed over dielectric material 110. Material 110 can comprise any suitable material, and in particular aspects will comprise, consist essentially of, or consist of silicon dioxide. If material 110 is silicon dioxide, such can be formed to an exemplary thickness of about 200Å. Patterned masking material 112 can be, for example, photoresist, which is formed into the shown pattern with photolithographic processing. Material 112 is shown to form a plurality of horizontally-extending strips 114 in the views of Figs. 103 and 104, with such strips being spaced from one another by gaps 116. Pedestals 88 are shown in dashed-line view in the top view of Fig. 103, to indicate that such pedestals have other materials thereover.

[00121] Referring next to Figs. 106-108, gaps 116 are extended through material 110, and subsequently masking layer 112 (Figs. 103-105) is removed. In aspects in

which material 110 comprises silicon dioxide, the etch through material 110 can comprise a dry etch which removes at least about 300Å of silicon dioxide. Such etch exposes upper surfaces of one set of the conductive pedestals, while leaving another set of the conductive pedestals covered by material 110. The exposed sets and covered sets alternate in horizontally-extending lines in the top view of Fig. 106. The exposed set of pedestals is ultimately connected to digit lines while the covered sets will ultimately be connected to memory storage devices, as will become more clear in the discussion that follows.

[00122] The material 110 remaining after gaps 116 are extended through material 110 is in the form of a plurality of lines 118 extending along a horizontal direction in the top view of Fig. 106.

[00123] Referring next to Figs. 109-111, a first conductive digit line material 120 is formed within gaps 116 and over the lines 118 of material 110. Conductive digit line material 120 contacts the set of pedestals exposed within gaps 116, but does not contact the set of pedestals protected by lines 118 of material 110. Conductive material 120 can comprise any suitable electrically conductive material, and in particular aspects will comprise, consist essentially of, or consist of conductively-doped silicon. For instance, material 120 can be conductively-doped polycrystalline silicon formed to a thickness of about 500Å.

[00124] A second conductive digit line material 122 is formed over the first conductive digit line material 120. Second material 122 can comprise any suitable material, and in particular aspects will comprise, consist essentially of, or consist of metal and/or metal compounds. For instance, material 122 can comprise, consist essentially of, or consist of tungsten. In an exemplary application, material 122 can be tungsten formed to a thickness of about 500Å.

[00125] An electrically insulative cap 124 is formed over second conductive layer 122. Electrically insulative cap can comprise any suitable material, and in particular aspects will be a nitride-containing material. For instance, cap 124 can be silicon nitride formed to a thickness of about 1000Å.

[00126] A patterned masking material 126 is formed over cap 124. Masking material 126 can be, for example, photoresist formed into the shown pattern with photolithographic processing. Mask 126 is formed in a series of lines 128 spaced from one another by gaps 130. Mask 126 defines a digit line pattern. The lines 126 and gaps 130 are illustrated in the top view of Fig. 109 as extending in a horizontally-

elongated direction. The pedestals 88 are shown in dashed-line view in Fig. 109 to indicate that the pedestals are beneath other materials.

[00127] Referring next to Figs. 112-114, a pattern is transferred from patterned masking layer 126 (Figs. 109-111) through layers 120, 122 and 124, and subsequently masking layer 126 is removed. The transferring of the pattern through layers 120, 122 and 124 extends gap 130 through the layers, and forms the layers 120, 122 and 124 into patterned stacks corresponding to horizontally-extending digit line stacks 132.

[00128] The materials 120, 122 and 124 can be patterned utilizing any suitable etch or combination of etches. For instance, material 124 can be silicon nitride, and can be patterned utilizing a dry etch; material 122 can be tungsten, and can be patterned utilizing a dry etch; and material 120 can be polysilicon and can be patterned utilizing a dry etch.

[00129] The conductive digit line material 120 contacts a first set of pedestals 88, and a second set of pedestals is exposed within openings 130. The first set of pedestals is shown in dashed-line view in Fig. 112 to indicate that such set is covered by other materials in the shown view.

[00130] Referring next to Figs. 115-117, insulative material spacers 134 are formed along stacks 132. Spacers 134 can comprise, consist essentially of, or consist of silicon nitride, and can be formed by depositing a layer of silicon nitride having a thickness of about 200Å, and subsequently subjecting such layer to an anisotropic spacer etch. Spacers 134 narrow openings 130 between the stacks 132.

[00131] An electrically insulative material 136 is formed within the openings 130, and also over stacks 132. Electrically insulative material 136 can, for example, comprise, consist essentially of, or consist of silicon dioxide. In particular aspects, material 136 is silicon dioxide formed to a thickness of about 3000Å. Alternatively, material 136 can be borophosphosilicate glass (BPSG) formed to a thickness of about 3000Å. Material 136 has a planarized upper surface 137 which can be formed by, for example, chemical-mechanical polishing across the surface of material 136. In particular aspects, material 136 is chemical-mechanical polished so that the remaining thickness of material 136 from a base of openings 130 to an uppermost surface of the material 136 is about 7000Å.

[00132] A patterned masking material 138 is formed over material 136. Material 138 can be photoresist formed into the shown pattern by photolithographic processing. Patterned mask 138 is formed in a series of lines 140 spaced from one another by gaps

142. The lines and gaps extend in a horizontal direction in the top view of Fig. 115. The pedestals 88 are shown diagrammatically in top view 115 to provide a reference of the location of lines 140.

[00133] Referring next to Figs. 118-120, gaps 142 are extended through material 136 to expose the set of pedestals which is not covered by digit line stacks 132, and subsequently patterned mask 138 (Figs. 115-117) is removed.

[00134] The etch utilized to extend through material 136 is preferably selective for material 136 relative to the material of spacers 134. Accordingly, the spacers protect conductive digit line materials 120 and 122 from being exposed during the removal of material 136. In particular aspects, material 136 can be silicon dioxide, spacers 134 can be silicon nitride, and the etch utilized to remove material 136 can be a dry etch which removes about 4000Å of silicon dioxide.

[00135] Referring next to Figs. 121-123, an electrically conductive material 146 is formed within gaps 142. Electrically conductive material 146 can comprise any suitable material. In particular aspects, the conductive material will comprise, consist essentially of, or consist of conductively-doped silicon. For instance, material 146 can be conductively-doped polycrystalline silicon formed to a thickness of about 500Å. The material 146 would typically be formed over material 136, and then subjected to planarization to form the shown planarized upper surface 147 extending across materials 136 and 146.

[00136] A plurality of memory storage devices 145, 148, 150 and 152 are diagrammatically illustrated as being electrically connected with conductive material 146. The memory storage devices can comprise, for example, capacitors, and are electrically connected through conductive pedestals defined by material 146 to underlying source/drain regions incorporated within the pedestals 88.

[00137] The top view of Fig. 121 shows that the pedestals 146 and digit line stacks 132 form alternating horizontally-elongated rows. Although not shown in Fig. 121, it is to be understood that there would typically be isolation regions provided along the horizontally-extending row of conductive pedestals 146 so that each of the source/drain regions 88 along the row would be electrically connected to a single memory storage unit electrically separated from the memory storage units that other source/drain regions along the same row are connected to. Thus, each source/drain region within the row can be utilized to store a single bit of information.

[00138] The source/drain regions electrically connected to conductive pedestal material 146 are paired with source/drain regions electrically connected to digit line stacks 132 to define individual transistors. Such pairing is illustrated diagrammatically in Fig. 121 by the brackets 160 and 162 which illustrate exemplary source/drain regions which can be paired within individual transistors. The gateline material 94 defines the gate of the transistor which gatedly connects the paired source/drain regions to one another. Particular transistor constructions which can be utilized in exemplary aspects of the present invention are described with reference to Figs. 124-126.

[00139] Referring to Fig. 124, a fragment of construction 10 is illustrated in cross-sectional view at a processing stage at or after the processing stage of Figs. 82-84 in accordance with an exemplary aspect of the invention. In referring to the construction of Fig. 124, identical numbering will be used as was used above in describing Figs. 1-123, where appropriate. Accordingly, the construction 10 of Fig. 124 is shown to comprise the substrate 12, gateline material 94, and gate dielectric material 92 described previously. The construction of Fig. 124 further comprises a pair of pedestals 200 and 202 which are particular aspects of the pedestals 88 described previously. The pedestals 200 and 202 are paired within a transistor construction, and accordingly can correspond to a pair of the pedestals along the cross-sectional view 83, such as the paired pedestals 89 discussed above with reference to Fig. 83. The pedestals and gateline material differ in Fig. 124 relative to pedestals and gateline material described previously in this application in that the pedestals of Fig. 124 are at about the same elevational height over substrate 12 as is the gateline material, whereas such was not the case in the aspects of the invention described with reference to Figs. 1-123. The gateline/pedestal relationships of Fig. 124 and of Figs. 1-123 can be utilized interchangeably in the various aspects of the invention described herein.

[00140] One of the pedestals 88 of the Fig. 124 construction can ultimately be a source/drain region utilized to electrically connect to a digit line, and the other can ultimately be a source/drain region utilized to electrically connect to a memory storage device. In order to distinguish the pedestals from one another, one of the pedestals is labeled as 200, and the other is labeled as 202. In exemplary aspects, the pedestal 200 will be utilized for connecting to a digit line and the pedestal 202 would be utilized for connecting to a memory device, but it is to be understood that the utilizations of the pedestals can be reversed. The gateline material 94 between pedestals 200 and 202 ultimately functions as a transistor gate of a transistor device, and such transistor gate

gatedly connects a source/drain region associated with pedestal 202 with a source/drain region associated with pedestal 200.

[00141] Each of pedestals 200 and 202 has a heavily-doped region source/drain in an uppermost portion of the pedestal, with the heavily-doped region of pedestal 200 being labeled 204 and the heavily-doped region of pedestal 202 being labeled 206. In the shown exemplary aspect of the invention, both heavily-doped regions are doped to be n-type doped regions. The regions are shown to be n+ regions to indicate that the regions are doped comparatively heavily relative to other regions of the Fig. 124 construction.

[00142] Pedestal 202 comprises a lightly-doped region extending from the heavily doped region 206 to an upper surface of substrate 12, with such lightly-doped region being indicated to be n-. Substrate 12 comprises a diffusion region 210 therein, and the lightly-doped portion of pedestal 88 is shown electrically connecting with the diffusion region 210. In the shown aspect of the invention, the diffusion region 210 is doped to an n- level.

[00143] Pedestal 200 comprises an intermediately doped region extending from the heavily-doped region 204 to an upper surface of substrate 12. The intermediately-doped region is shown to be a p-type region, and is labeled as being "p". Such label indicates that the region is more heavily doped than would be a p- or n- region, but less heavily doped than would be an n+ or p+ region.

[00144] Substrate 12 comprises a conductively-doped diffusion region 212 beneath pedestal 200, and the intermediately-doped region of pedestal 200 is shown electrically connecting with conductively-doped region 212. In the shown aspect of the invention, conductively-doped region 212 is shown to be lightly doped with p-type dopant, and accordingly is shown as a p- region.

[00145] Substrate 12 has a p-- region interconnecting the diffusion regions 210 and 212.

[00146] The transistor gate of gateline 94 gatedly connects the heavily-doped source/drain region 204 with the heavily-doped source/drain region 206 through the conductively-doped pedestals 200 and 202, through the conductively-doped regions 210 and 212, and through the p-- region of substrate 12. The channel length of the transistor device is the length extending from source/drain region 204 to source/drain region 206. The channel characteristics of the device can be influenced by tailoring the dopant concentrations and types along the channel length. Additionally, characteristics of the

device can be influenced by the type of materials utilized for pedestals 200 and 202. For instance, if epitaxial material is utilized for the pedestals, such material tends to be relatively leaky compared to other semiconductor materials. In some aspects it can be advantageous to have the source/drain region associated with the digit line be relatively leaky while the source/drain region associated with the memory storage device be less leaky. In such aspects it can be advantageous to form the pedestals associated with the digit line source/drain region to comprise, consist essentially of, or consist of conductively-doped epitaxial semiconductor material (such as, epitaxial silicon) while the pedestal associated with the source/drain region of the memory storage device comprises, consists essentially of, or consists of conductively-doped semiconductor material which is not epitaxial, such as, for example, conductively-doped silicon which is not epitaxial. If the non-epitaxial semiconductor material is silicon, such can be in the form of, for example, amorphous silicon or polycrystalline silicon. As indicated above, in particular aspects pedestal 200 will be associated with a digit line and pedestal 202 will be associated with a memory storage device.

[00147] Another aspect of the invention is described with reference to Fig. 125. In referring to Fig. 125, similar numbering will be used as was used above in describing Fig. 124. Fig. 125 shows a construction 10 comprising gateline material 94, a pair of pedestals 200 and 202, substrate 12, and gate dielectric material 92. Pedestals 200 and 202 comprise the heavily-doped source/drain regions 204 and 206, but differ from the pedestals described in Fig. 124 in that the pedestals of Fig. 125 are identical to one another and both comprise lightly-doped (shown as p-) regions extending between the heavily-doped regions 204 and 206 and the substrate 12. The substrate 12 comprises p-- doping interconnecting the pedestals 200 and 202. As discussed above with reference to Fig. 124, both of the pedestals can comprise the same composition as one another, or alternatively one of the pedestals can be epitaxial while the other is not.

[00148] Fig. 126 shows yet another aspect of the invention. Similar numbering will be used in referring to Fig. 126 as was used above in describing Figs. 124 and 125. Fig. 126 comprises the gateline material 94, gate dielectric material 92, substrate 12, pedestals 200 and 202, and heavily-doped source/drain regions 204 and 206 described previously. The construction of Fig. 126 differs from those of Figs. 124 and 125 in several aspects. First, the construction of Fig. 126 comprises spacers 216 and 218 proximate the pedestal 202. Such spacers can narrow pedestal 202 relative to pedestal 200 (i.e., reduce a horizontal cross-sectional width of pedestal 202 relative to the

horizontal cross-sectional width of pedestal 200). Spacers 216 can be provided in additional processing steps beyond those described above with reference Figs. 1-123 by methodology which will be recognized by persons of ordinary skill in the art. Spacers 216 and 218 can comprise, for example, silicon nitride. The utilization of spacers 216 and 218 adjacent pedestal 202 but not adjacent pedestal 200 can allow the electrical characteristics of pedestals 202 and 200 to be specifically tailored to the particular applications that the pedestals are to be utilized in, which can be advantageous in some aspects of the invention. The control of the pedestal width can allow additional control beyond that which can be obtained by controlling doping alone within the pedestal. Although the pedestals are shown having different widths relative to one another, it is to be understood that spacers analogous to 216 and 218 can also be formed adjacent pedestal 200 so that pedestal 200 is also narrowed.

[00149] The substrate 12 is shown comprising the conductively-doped diffusion regions 210 and 212 discussed previously with reference to Fig. 124, and pedestals 200 and 202 are shown comprising the same type of doping as was discussed with reference to Fig. 124. It is to be understood, however, that the aspect of the invention of utilization of spacers adjacent one of the pedestals can be used with any appropriate doping of the pedestals and substrate, and that the aspect of Fig. 126 is but one of many aspects of the invention.

[00150] Figs. 124-126 illustrate exemplary aspects of the invention, and it is to be understood that the invention also encompasses various modifications of such aspects. For instance, the dopant types shown in the figures can be reversed relative to the shown aspects. Thus, all of the n-type regions can be converted to opposite conductivity (i.e. p-type) regions, and likewise the p-type regions can be converted to opposite-conductivity (i.e. n-type) regions.

[00151] Methodology of the invention can be used in numerous applications. For instance, the invention can be utilized for forming two-vertical transistor, one-capacitor $4F^2$ DRAM cells. In particular aspects, the invention can be considered to comprise vertical DRAM cell technology. One transistor is utilized to connect the cell to a substrate, and another transistor connects the digit line to the substrate. The self-aligned lateral transistor connects vertical source/drain region pedestals to one another. The cell can have low digit capacitance and low wordline resistance, and also can have redundancy against vertical axis problems.

[00152] Although the gateline is shown extending entirely around source/drain regions in the shown aspects of the invention, it is to be understood that the invention encompasses other aspects (not shown) in which the gateline extends less than fully around the source/drain regions. For instance, the gateline can extend one-quarter of the way around the source/drain region, halfway around the source/drain region, three-quarters of the way around the source/drain region, etc.

[00153] Persons of ordinary skill in the art will recognize that the methodology of Figs. 1-123 advantageously self-aligns numerous features relative to one another.

[00154] Fig. 127 illustrates generally, by way of example, but not by way of limitation, an embodiment of a computer system 400 according to an aspect of the present invention. Computer system 400 includes a monitor 401 or other communication output device, a keyboard 402 or other communication input device, and a motherboard 404. Motherboard 404 can carry a microprocessor 406 or other data processing unit, and at least one memory device 408. Memory device 408 can comprise various aspects of the invention described above. Memory device 408 can comprise an array of memory cells, and such array can be coupled with addressing circuitry for accessing individual memory cells in the array. Further, the memory cell array can be coupled to a read circuit for reading data from the memory cells. The addressing and read circuitry can be utilized for conveying information between memory device 408 and processor 406. Such is illustrated in the block diagram of the motherboard 404 shown in Fig. 128. In such block diagram, the addressing circuitry is illustrated as 410 and the read circuitry is illustrated as 412. Various components of computer system 400, including processor 406, can comprise one or more of the constructions described previously in this disclosure.

[00155] Processor device 406 can correspond to a processor module, and associated memory utilized with the module can comprise teachings of the present invention.

[00156] Memory device 408 can correspond to a memory module. For example, single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) may be used in the implementation which utilize the teachings of the present invention. The memory device can be incorporated into any of a variety of designs which provide different methods of reading from and writing to memory cells of the device. One such method is the page mode operation. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell arrays and randomly accessing

different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed.

[00157] An alternate type of device is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on a memory bus. Other alternative types of devices include SDRAM, DDR SDRAM, SLDRAM, VRAM and Direct RDRAM, as well as others such as SRAM or Flash memories.

[00158] Memory device 408 can comprise memory formed in accordance with one or more aspects of the present invention.

[00159] Fig. 129 illustrates a simplified block diagram of a high-level organization of various embodiments of an exemplary electronic system 700 of the present invention. System 700 can correspond to, for example, a computer system, a process control system, or any other system that employs a processor and associated memory. Electronic system 700 has functional elements, including a processor or arithmetic/logic unit (ALU) 702, a control unit 704, a memory device unit 706 and an input/output (I/O) device 708. Generally, electronic system 700 will have a native set of instructions that specify operations to be performed on data by the processor 702 and other interactions between the processor 702, the memory device unit 706 and the I/O devices 708. The control unit 704 coordinates all operations of the processor 702, the memory device 706 and the I/O devices 708 by continuously cycling through a set of operations that cause instructions to be fetched from the memory device 706 and executed. In various embodiments, the memory device 706 includes, but is not limited to, random access memory (RAM) devices, read-only memory (ROM) devices, and peripheral devices such as a floppy disk drive and a compact disk CD-ROM drive. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that any of the illustrated electrical components are capable of being fabricated to include memory constructions in accordance with various aspects of the present invention.

[00160] Fig. 130 is a simplified block diagram of a high-level organization of various embodiments of an exemplary electronic system 800. The system 800 includes a memory device 802 that has an array of memory cells 804, address decoder 806, row access circuitry 808, column access circuitry 810, read/write control circuitry 812 for controlling operations, and input/output circuitry 814. The memory device 802 further

includes power circuitry 816, and sensors 820, such as current sensors for determining whether a memory cell is in a low-threshold conducting state or in a high-threshold non-conducting state. The illustrated power circuitry 816 includes power supply circuitry 880, circuitry 882 for providing a reference voltage, circuitry 884 for providing the first wordline with pulses, circuitry 886 for providing the second wordline with pulses, and circuitry 888 for providing the bitline with pulses. The system 800 also includes a processor 822, or memory controller for memory accessing.

[00161] The memory device 802 receives control signals 824 from the processor 822 over wiring or metallization lines. The memory device 802 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 802 has been simplified to help focus on the invention. At least one of the processor 822 or memory device 802 can include a memory construction of the type described previously in this disclosure.

[00162] The various illustrated systems of this disclosure are intended to provide a *general understanding of various applications for the circuitry and structures of the present invention*, and are not intended to serve as a complete description of all the elements and features of an electronic system using memory cells in accordance with aspects of the present invention. One of the ordinary skill in the art will understand that the various electronic systems can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device(s).

[00163] Applications for memory cells can include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

CLAIMS

The invention claimed is:

1. A method for forming a semiconductor structure, comprising:
providing a semiconductor substrate;
forming a first material and a second material over the substrate, the first and second materials being selectively etchable relative to one another, the first material being formed to be a lattice and the second material being formed to be repeating regions spaced from one another by segments of the lattice, the repeating regions forming an array, the array having a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis; the second pitch being about twice as big as the first pitch;
replacing at least some of the first material of the lattice with one or more conductive materials of a gateline; and
replacing at least some of the second material with doped semiconductor material to form upwardly elongated source/drain regions over the substrate.
2. The method of claim 1 wherein the replacing at least some of the first material occurs before the replacing at least some of the second material.
3. The method of claim 1 wherein the replacing at least some of the second material occurs before the replacing at least some of the first material.
4. The method of claim 1 wherein the first material comprises silicon nitride and the second material comprises silicon dioxide.
5. The method of claim 1 wherein the first material consists essentially of silicon nitride and the second material consists essentially of silicon dioxide.
6. The method of claim 1 wherein the first material comprises silicon dioxide and the second material comprises silicon nitride.
7. The method of claim 1 wherein the first material consists essentially of silicon dioxide and the second material consists essentially of silicon nitride.
8. The method of claim 1 wherein the one or more conductive materials of the gateline include conductively-doped silicon.

9. The method of claim 1 wherein the one or more conductive materials of the gateline include one or more metals.

10. The method of claim 1 wherein the one or more conductive materials of the gateline include one or more metal alloys.

11. The method of claim 1 wherein the substrate comprises monocrystalline semiconductor material and wherein at least some of the doped semiconductor material of the upwardly-elongated source/drain regions is epitaxially grown from the monocrystalline semiconductor material of the substrate.

12. The method of claim 1 wherein:
the substrate comprises monocrystalline semiconductor material;
some of the doped semiconductor material of the upwardly-elongated source/drain regions is single crystal material epitaxially grown from the monocrystalline semiconductor material of the substrate; and
some of the doped semiconductor material of the upwardly-elongated source/drain regions is not single crystal material.

13. The method of claim 1 further comprising forming a digit line over and in electrical connection with some of the upwardly-elongated source/drain regions.

14. The method of claim 13 wherein the digit line is over and in electrical connection with a first set of the upwardly-elongated source/drain regions, and is not in electrical connection with a second set of the source/drain regions; and further comprising forming memory storage devices over and in electrical connection with the second set of source/drain regions.

15. The method of claim 14 wherein the memory storage devices are capacitors.

16. A method for forming a semiconductor structure, comprising:
providing a semiconductor substrate;
forming a nitride-containing material lattice over the substrate; the lattice defining an array of non-nitride regions spaced from one another by segments of the lattice;
replacing nitride-containing material of the lattice with one or more conductive materials of a gateline; and
replacing non-nitride regions with doped semiconductor material to form upwardly-elongated source/drain regions.

17. The method of claim 16 wherein the array has a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis; and wherein the second pitch is larger than the first pitch.

18. The method of claim 17 wherein the second pitch is about twice as big as the first pitch.

19. The method of claim 16 wherein only some of the lattice is replaced by the one or more conductive materials of the gateline; and wherein some of the lattice is replaced by dielectric material provided between the gateline and the vertically-extending source/drain regions.

20. The method of claim 16 wherein the nitride-containing material comprises silicon nitride.

21. The method of claim 16 wherein the nitride-containing material consists essentially of silicon nitride.

22. The method of claim 16 wherein the nitride-containing material consists of silicon nitride.

23. The method of claim 16 wherein the non-nitride regions comprise silicon dioxide prior to replacing the non-nitride regions with the doped semiconductor material.

24. The method of claim 16 wherein the non-nitride regions consist essentially of silicon dioxide prior to replacing the non-nitride regions with the doped semiconductor material.

25. The method of claim 16 wherein the non-nitride regions consist of silicon dioxide prior to replacing the non-nitride regions with the doped semiconductor material.

26. The method of claim 16 wherein the doped semiconductor material comprises epitaxially-grown silicon.

27. The method of claim 16 wherein the doped semiconductor material consists essentially of doped epitaxially-grown silicon.

28. The method of claim 16 wherein the doped semiconductor material consists of doped epitaxially-grown silicon.

29. The method of claim 16 further comprising forming a digit line over and in electrical connection with some of the upwardly-elongated source/drain regions.

30. The method of claim 29 wherein the digit line is over and in electrical connection with a first set of the upwardly-elongated source/drain regions, and is not in electrical connection with a second set of the source/drain regions; and further comprising forming memory storage devices over and in electrical connection with the second set of source/drain regions.

31. The method of claim 30 wherein the memory storage devices are capacitors.

32. A method for forming a semiconductor structure, comprising:
providing a first semiconductor material;
forming an oxide-containing material over the first semiconductor material;
forming openings extending through the oxide-containing material;
forming nitride-containing spacers within the openings to narrow the openings;
extending the narrowed openings into the first semiconductor material, the narrowed openings having a first portion extending within the first semiconductor material and a second portion over the first portion;
providing a dielectric material to fill the first portion of the openings and leave the second portion not filled;
providing a nitride-containing material over the dielectric material to fill the second portion of the openings;
replacing the oxide-containing material with a doped second semiconductor material to form upwardly-elongated source/drain regions; and
replacing the nitride-containing material and nitride-containing spacers with one or more conductive materials of a gateline.
33. The method of claim 32 wherein the nitride-containing material and nitride-containing spacers comprise the same composition as one another.
34. The method of claim 32 wherein the nitride-containing material and nitride-containing spacers comprise silicon nitride.
35. The method of claim 32 wherein the nitride-containing material and nitride-containing spacers consist essentially of silicon nitride.
36. The method of claim 32 wherein the nitride-containing material and nitride-containing spacers consist of silicon nitride.
37. The method of claim 32 wherein the dielectric material is a first dielectric material, and further comprising providing a second dielectric material between the upwardly-elongated source/drain regions and the gateline.

38. The method of claim 32 further comprising forming a digit line in electrical connection with some of the source/drain regions, and forming capacitor constructions in electrical connection with others of the source/drain regions.

39. The method of claim 38 wherein the digit line is formed to be above said some of the source/drain regions.

40. The method of claim 32 wherein the first semiconductor material is monocrystalline silicon, and wherein the second semiconductor material is silicon epitaxially grown from the first semiconductor material.

41. The method of claim 32 wherein the openings are trenches longitudinally elongated along a defined horizontal direction, wherein the nitride-containing material is a first nitride-containing material, and wherein the first nitride-containing material within the openings is in the form of strips extending longitudinally in the horizontal direction; the method further comprising:

forming a second nitride-containing material in strips extending along a defined vertical direction; the first and second nitride-containing materials together forming a lattice; wherein the oxide-containing material is in the form of an array of pillars, individual pillars of the array being surrounded by the lattice of the first and second nitride-containing materials; and

replacing the second nitride-containing material with said one or more conductive materials simultaneously with the replacing of the first nitride-containing material.

42. The method of claim 41 wherein the first and second nitride-containing materials comprise the same composition as one another.

43. The method of claim 41 wherein the first and second nitride-containing materials comprise silicon nitride.

44. The method of claim 41 wherein the first and second nitride-containing materials consist essentially of silicon nitride.

45. The method of claim 41 wherein the first and second nitride-containing materials consist of silicon nitride.

46. A method for forming a semiconductor structure, comprising:
- providing a first semiconductor material;
 - forming an oxide-containing material over the first semiconductor material;
 - forming a hard mask layer over the oxide-containing material;
 - patterning the hard mask layer into a plurality of spaced lines extending along a defined horizontal direction, the spaced lines being separated by first gaps;
 - forming nitride-containing spacers along the hard mask to narrow the first gaps;
 - extending the narrowed first gaps through the oxide-containing material;
 - removing the hard mask layer while leaving the nitride-containing spacers; the spacers forming sets of paired lines extending along the narrowed first gaps;
 - filling the narrowed first gaps with a first nitride-containing material, the first nitride-containing material extending upwardly between the sets of paired lines to form nitride-containing pillars over the oxide-containing material, the first nitride-containing material and nitride-containing spacers together being incorporated into spaced horizontally-extending pillars over the oxide-containing material, the spaced horizontally-extending pillars being separated by second gaps;
 - extending the second gaps through the oxide-containing material; and
 - filling the second gaps with a second nitride-containing material.
47. The method of claim 46 wherein the oxide-containing material comprises silicon dioxide.
48. The method of claim 46 wherein:
- the filling the narrowed first gaps with the first nitride-containing material comprises forming the first nitride-containing material over the nitride-containing spacers and across regions of the oxide between the nitride-containing spacers that are ultimately to be the second gaps; and
 - the incorporating the first nitride-containing material and nitride-containing spacers into the spaced horizontally-extending pillars comprises anisotropically etching the first nitride-containing material to remove the first nitride-containing material from across the regions and thereby form the second gaps.

49. The method of claim 46 wherein:

the first and second nitride-containing materials are the same as one another in composition;

the spaced lines and first gaps repeat along a vertical direction to define a first vertical pitch, the first vertical pitch having a first distance corresponding to a line/first gap pair;

the first nitride-containing material within the narrowed first gaps and the second nitride-containing material within the second gaps form horizontally-extending nitride-containing lines spaced from one another by lines of the oxide-containing material; the lines of oxide-containing material and lines of nitride-containing material forming a repeating pattern along the vertical direction to define a second vertical pitch, the second vertical pitch having a second distance corresponding to a nitride-containing-material line/oxide-containing-material line pair; and

the second distance is about one-half of the first distance.

50. The method of claim 46 wherein the nitride-containing spacers, first nitride-containing material and second nitride-containing material all contain the same composition as one another and together are incorporated into a nitride-containing lattice, and further comprising forming a plurality of transistor constructions by:

replacing at least some of the nitride-containing lattice with one or more electrically-conductive gate line materials; and

replace at least some of the oxide-containing material with conductively-doped source/drain structures.

51. The method of claim 50 wherein the composition of the nitride-containing spacers, first nitride-containing material and second nitride-containing material comprises silicon nitride.

52. The method of claim 50 wherein the composition of the nitride-containing spacers, first nitride-containing material and second nitride-containing material consists essentially of silicon nitride.

53. The method of claim 50 wherein the composition of the nitride-containing spacers, first nitride-containing material and second nitride-containing material consists of silicon nitride.

54. A semiconductor structure, comprising:
a semiconductor substrate;
a nitride-containing material lattice over the substrate; and
an array of non-nitride regions spaced from one another by segments of the lattice; the array having a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis; the second pitch being about twice as big as the first pitch.

55. The structure of claim 54 wherein the nitride-containing material comprises silicon nitride.

56. The structure of claim 54 wherein the nitride-containing material consists essentially of silicon nitride.

57. The structure of claim 54 wherein the nitride-containing material consists of silicon nitride.

58. The structure of claim 54 wherein the non-nitride regions comprise silicon dioxide.

59. The structure of claim 54 wherein the non-nitride regions consist essentially of silicon dioxide.

60. The structure of claim 54 wherein the non-nitride regions consist of silicon dioxide.

61. A semiconductor structure, comprising:
a semiconductor substrate;
a gateline lattice over the substrate; and
an array of non-gateline regions spaced from one another by segments of the lattice; the array having a defined first pitch along a first axis and a defined second pitch along a second axis substantially orthogonal to the first axis; the second pitch being about twice as big as the first pitch; the non-gateline regions comprising upwardly-elongated source/drain regions; the gateline lattice and source/drain regions together forming a plurality of transistor constructions in which pairs of the source/drain regions are gatedly connected to one other through the gateline lattice.

62. The structure of claim 61 wherein the gateline lattice comprises at least one metal.
63. The structure of claim 61 wherein the gateline lattice comprises at least one metal alloy.
64. The structure of claim 61 wherein the gateline lattice comprises conductively-doped silicon.
65. The structure of claim 61 wherein the gateline lattice consists essentially of conductively-doped silicon.
66. The structure of claim 61 wherein the gateline lattice consists of conductively-doped silicon.
67. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions comprise conductively-doped epitaxial silicon.
68. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions consist essentially of conductively-doped epitaxial silicon.
69. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions consist of conductively-doped epitaxial silicon.
70. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions comprise conductively-doped polycrystalline silicon.
71. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions consist essentially of conductively-doped polycrystalline silicon.
72. The structure of claim 61 wherein at least some of the upwardly-elongated source/drain regions consist of conductively-doped polycrystalline silicon.
73. The structure of claim 61 wherein some of the upwardly-elongated source/drain regions consist essentially of conductively-doped epitaxial silicon and others consist essentially of conductively-doped polycrystalline silicon.

74. The structure of claim 73 wherein source/drain regions consisting essentially of conductively-doped epitaxial silicon are gatedly connect to source/drain regions consisting essentially of conductively-doped polycrystalline silicon.

75. The structure of claim 61 wherein the non-gateline regions comprise dielectric material separating the upwardly-elongated source/drain regions from the gateline lattice.

76. A memory device construction, comprising:
a semiconductor substrate;
a gateline over the substrate;
a pair of upwardly-elongated source/drain regions over the substrate and at least partially surrounded by the gateline, one of the source/drain regions being a first source/drain region and consisting essentially of conductively-doped epitaxial silicon, the other source/drain region being a second source/drain region and consisting essentially of conductively-doped silicon which is not epitaxial, the first and second source/drain regions being gatedly connected to one another through the gateline;
a memory storage device electrically connected to either the first source/drain region or the second source/drain region; and
a digit line electrically connected to whichever of the first and second source/drain regions is not electrically connected to the memory storage device.

77. The construction of claim 76 wherein the memory storage device is electrically connected to the first source/drain region.

78. The construction of claim 76 wherein the memory storage device is electrically connected to the second source/drain region.

79. The construction of claim 76 wherein the digit line and memory storage device are above the first and second source/drain regions.

80. The construction of claim 76 wherein the first and second source/drain regions have a first horizontally cross-sectional width and a second horizontally cross-sectional width respectively; and wherein the first and second horizontally cross-sectional widths are about the same as one another.

81. The construction of claim 76 wherein the first and second source/drain regions have a first horizontally cross-sectional width and a second horizontally cross-sectional width respectively; and wherein the first and second horizontally cross-sectional widths are not about the same as one another.

82. The construction of claim 81 wherein the second horizontally cross-sectional width is less than the first horizontally cross-sectional width.

83. The construction of claim 81 wherein the first horizontally cross-sectional width is less than the second horizontally cross-sectional width.

84. The construction of claim 81 wherein the memory storage device is a capacitor.

85. The construction of claim 81 wherein the memory storage device and gateline are together comprised by a DRAM cell.

86. An electronic system comprising the construction of claim 85.

87. A memory device construction, comprising:
a semiconductor substrate;
a gateline over the substrate;
a pair of upwardly-elongated source/drain regions over the substrate and at least partially surrounded by the gateline, one of the source/drain regions being a first source/drain region and the other source/drain region being a second source/drain region;
a memory storage device electrically connected to said first source/drain region;
a digit line electrically connected to said second source/drain region; and
wherein:

the first source/drain region consists essentially of a first conductively-doped semiconductor material having an uppermost region doped to a first conductivity type and a remainder doped to a second conductivity type opposite the first conductivity type;

the first source/drain region consists essentially of a second

conductively-doped semiconductor material having an uppermost region doped to the first conductivity type, and a remainder doped to the second conductivity type; and

the substrate comprises a segment extending between the first and second source/drain regions and doped to the second conductivity type.

88. The construction of claim 87 wherein the first conductivity type is n-type and the second conductivity type is p-type.

89. The construction of claim 87 wherein the first conductivity type is p-type and the second conductivity type is n-type.

90. The construction of claim 87 wherein the digit line is above the second source/drain region.

91. The construction of claim 87 wherein one of the first and second conductively-doped semiconductor materials consists essentially of conductively-doped epitaxial semiconductor material and the other consists essentially of conductively doped semiconductor material which is not epitaxial.

92. The construction of claim 91 wherein the first conductively-doped semiconductor material consists essentially of the conductively-doped epitaxial semiconductor material.

93. The construction of claim 91 wherein the second conductively-doped semiconductor material consists essentially of the conductively-doped epitaxial semiconductor material.

94. The construction of claim 87 wherein the memory storage device and gateline are together comprised by a DRAM cell.

95. An electronic system comprising the construction of claim 94.

96. A memory device construction, comprising:
a semiconductor substrate;
a gateline over the substrate;
a pair of upwardly-elongated source/drain regions over the substrate and at least partially surrounded by the gateline, one of the source/drain regions being a first source/drain region and the other source/drain region being a second source/drain region;
a memory storage device electrically connected to said first source/drain region;
a digit line electrically connected to said second source/drain region; and
wherein:

the first source/drain region consists essentially of a first conductively-doped semiconductor material having an uppermost region doped to n+, and a remainder doped to n-;

the second source/drain region consists essentially of a second conductively-doped semiconductor material having an uppermost region doped to n+, and a remainder doped to p; and

the substrate comprises:

a first conductively-doped diffusion region ohmically connected to the first source/drain region and doped to n-;

a second conductively-doped diffusion region ohmically connected to the second source/drain region and doped to p-; and

a segment extending from the first conductively-doped diffusion region to the second conductively-doped diffusion region and doped to p--.

97. The construction of claim 96 wherein the first and second conductively-doped semiconductor materials consist essentially of epitaxial silicon.

98. The construction of claim 96 wherein one of the first and second conductively-doped semiconductor materials consists essentially of conductively-doped epitaxial silicon and the other comprises consists essentially of conductively-doped silicon which is not epitaxial.

99. The construction of claim 98 wherein the conductively-doped silicon which is not epitaxial is conductively-doped polycrystalline silicon.

100. The construction of claim 98 wherein the second conductively-doped semiconductor material consists essentially of the conductively-doped epitaxial silicon.

101. The construction of claim 98 wherein the memory storage device and gateline are together comprised by a DRAM unit cell.

102. An electronic system comprising the construction of claim 101.