HIGH DENSITY PLASMA AND BIAS RF POWER PROCESS TO MAKE STABLE FSG WITH LESS FREE F AND SIN WITH LESS H TO ENHANCE THE FSG/SIN INTEGRATION RELIABILITY

Abstract

An embodiment of the invention is a HDP CVD FSG layer and an HDP CVD SIN layer with more stability (e.g., less free F and less free H). A feature is that the FSG and SIN are formed using a HDP CVD process with a high plasma density between 1E12 and 1E15 ions/cc and more preferably between 1E14 and 1E15 ions/cc. The high bias has sufficient energy to break the F-Si bonds in the FSG. The high bias has sufficient energy to break the H-Si bonds in the silicon nitride. Whereby the FSG layer has less F and the SiN layer has less H that increases the FSG/SiN interface reliability. The embodiments can be used on smooth surfaces (non-gap fill applications).

FIGURE 2