

Description

This invention relates to integrated circuits including programmable logic arrays.

A programmable logic array (PLA) implements a desired logical truth table by accepting a plurality of logical input signals and decoding them to provide a plurality of output signals. The decoding function is usually accomplished using two arrays of logic gates, referred to as the "AND" plane and the "OR" plane. The input signals are applied to the AND plane, which partially decodes them, and applies the intermediate results as inputs to the OR plane. The terms AND and OR are representative of the Boolean algebra operations that are typically performed in the respective arrays. However, electrically both of the arrays are usually similar, and comprise a series of signal line conductors whose voltage state represents the logical value of a given logic output term (OR plane), or intermediate result (AND plane).

The signal line conductors in both the AND and OR planes are precharged to a high voltage state in the case of a dynamic PLA. In the case of a static PLA, they are connected to a load device that tends to continuously pull them up to a high voltage state. In either case, logic transistors are connected in a desired parallel pattern between the signal lines and a reference voltage (e.g., ground). Then, in order to perform a decoding operation, the input signals (or intermediate results) are applied to the control terminals of the logic transistors. If any of the logic transistors connected to a given signal line is thereby placed in the conductive state, that signal line is pulled down to the ground voltage state. Hence, electrically both the AND and OR planes perform a "NOR" operation.

The dynamic PLA design provides for low current consumption, since no dc current flows through the conductive logic transistors during a decode operation. However, clocks are required to switch between the precharge and decode operations for the AND and OR planes in a dynamic PLA. A first clock is applied to the AND plane, and a second clock delayed relative to the first is applied to the OR plane, so that the AND plane has sufficient time to complete its decode operation prior to performing the decode in the OR plane. The delay between the clocks must be sufficiently long to ensure that no erroneous discharge of a conductor occurs in the OR plane, since once discharged there is no further precharge signal available, and an erroneous output results. A disadvantage of using two clocks is that the circuit required for the clock signals does not readily fit in the area of either the AND or the OR plane, so that it is placed externally thereto. This complicates the layout of the integrated circuit, especially when

computer aided design techniques that utilize geometrically regular blocks of circuitry are used.

It is known to use a static array for both the AND and OR planes, instead of a dynamic array. The static array eliminates the need for any clocks, since both planes are receptive to decode input signals whenever they arrive. However, a static array draws dc current whenever any of the logic transistors is in the "on" (i.e., conducting) state, and hence the power consumption is undesirably high for some applications.

EP-A-0178437 discloses a CMOS programmable logic array including a dynamic AND plane and OR plane having precharge transistors. A clock delay circuit in parallel with the elements of the AND plane generates the clock signal for the OR plane. The clock delay circuit is driven by the clock signal supplied to the AND plane, and includes load devices that conform to the elements in the AND plane, thereby delaying the clock signal for the OR plane with respect to the clock signal for the AND plane. As a result, the circuit elements in the AND plane may generate their product terms before the delayed clock is supplied to the OR plane. The clock delay circuit also includes an output inverter that drives the OR plane precharge transistors.

It is therefore desirable to obtain a programmable logic array that obtains low power consumption and ease of layout.

According to this invention there is provided an integrated circuit as claimed in claim 1.

The invention will now be described with reference to the accompanying drawing, the single figure of which shows schematically an embodiment of the invention.

The following detailed description relates to a programmable logic array that allows a simplified layout, while obtaining low power consumption.

Referring to the Figure, a clock signal (CLOCK) is applied to the gates of p-channel precharged transistors M1-M5. The clock itself (not shown) may be on the same integrated circuit as the PLA, or may be located externally thereto. When the clock is low, the PLA is in the precharge mode. In precharge mode, all of the p-channel devices (M1...M5) connected to VDD and the AND plane lines (AR...A0) are turned on, due to the low clock voltage on their gates. Furthermore, since the clock is low, all of the outputs of the AND driver gates (G1...G5) are held low, and thus all of the n-channel transistors (M6...M16) in the AND plane are off (i.e., non-conducting). As a result, all of the AND plane logic lines (A0...A3) are precharged high (to VDD), as is the AND plane reference delay line (AR). With the AND plane logic lines (A0...A3) being all high, all of the n-channel logic transistors (M21...M25) in the OR plane are on. In addition, since the AND

plane reference line (AR) is high, all of the p-channel clocked load transistors (M17...M20) connected to VDD and the OR plane logic lines (O0...O3) are off. As a result, all of the OR plane logic lines, O0...O3, are at ground potential (VSS) during precharge. Since CLOCK is low, and CLOCK high, during precharge, the input transmission gates T1...T4 are conducting. This allows the logic input signals X0,X1 to pass to the inputs of inverters I1...I4, where they are capacitively stored. The inverter outputs are then applied to the inputs of driver gates G2...G5; the outputs of the driver gates then control the logic transistors (M6...M13).

When the clock signal goes high, the PLA decodes the inputs (X0,X1) to produce the output signals (Y0...Y3). The illustrative circuit implements the logic function $Y0 = X0 \cdot X1$, $Y1 = X0 \cdot \bar{X1}$, $Y2 = X0 \cdot \bar{X1} + \bar{X0} \cdot X1$, and $Y3 = \bar{X0} \cdot \bar{X1}$. This is accomplished in the following manner: The clock going high turns off the p-channel precharge transistors (M1...M5) connected to the AND plane lines (AR...A0). The high clock signal also causes the output of G1 to go high, as well as the output of one input driver gate in each pair (G2-G3 and G4-G5). Which of the input driver gates goes high depends on whether the input (X0,X1) to the given pair was high or low when the clock was low. During the decode operation, the AND plane logic lines (A0...A3) which are connected to one or more n-channel logic transistors (M6...M13) that are turned on by an AND driver gate going high are discharged to VSS through the one or more logic transistors. Those logic lines in the AND plane that remain precharged high are considered to be in the "true" state.

The AND plane reference delay line AR will always discharge to VSS through an n-channel device (M16), which is turned on by the reference AND driver gate (G1). The reference AND driver gate goes high whenever the clock is high, and also drives dummy n-channel transistors (M14, M15). These dummy devices serve to capacitively load the reference driver gate G1 so as to match the worst case loading seen by any of the input driver gates (G2...G5). Similarly, dummy n-channel transistors (M34, M35) serve to capacitively load the AND plane reference delay line AR so as to match the worst case loading seen by any of the AND plane logic lines A0...A3. Therefore, AR will discharge to VSS no sooner than any of the AND plane logic lines A0...A3. The AR line discharging low turns on the p-channel load transistors (M17...M20) connected to VDD and the OR plane logic lines (O0-O3). Since the signal on the AR line is derived (and delayed) from the clock signal, the load transistors M17...M20 are considered herein to be clocked load transistors.

When in the decode state, the clocked load

transistors tend to pull the logic lines in the OR plane toward a high voltage state. Which of the OR logic lines are pulled high, and which remain low, is a function of the AND plane logic line decoding. For those OR plane logic lines which are a function of AND plane logic lines that have all decoded false (i.e., discharged to VSS), the corresponding n-channel transistors in the OR plane are turned off, and those OR plane logic lines are allowed to be pulled high by their p-channel clocked load transistors. On the other hand, for those OR plane logic lines which are a function of at least one AND plane logic line that has decoded true (i.e., remain precharged to VDD), the corresponding n-channel transistor in the OR plane remains on. The on-impedance of the n-channel transistors in the OR plane (M21...M25) is chosen to be sufficiently less than the on-impedance of the p-channel load transistors so that the true OR plane logic lines remain at a low voltage level (though not at VSS) as dc current flow occurs. Note that the dc current flow occurs only when the PLA is in the decode state, and hence the power dissipation remains relatively low as compared to static designs.

Deriving the OR plane clock by a delay line from the AND plane clock is hence very advantageous. However, the amount of the delay is optional insofar as the present invention is concerned. That is, if there were no delay in the clock signal applied to the OR plane, the PLA would still decode properly, unlike the case of PLA's having a dynamic OR plane. However, power dissipation is increased somewhat in the case of no delay, since both the clocked load transistors and all of the logic transistors in the OR plane are on simultaneously for a brief period. Providing sufficient delay so that the AND plane logic lines reach their decoded voltage level before the clocked load devices in the OR plane are turned on eliminates that component of the power consumption. An intermediate level of delay produces an intermediate power consumption.

The OR plane logic lines O0...O3 connect to optional output latching circuitry that may also be controlled by the clock. Clocked p-channel transistors M30-M33 serve to bias n-channel transistors M26-29, which provide for a small positive offset voltage, equal to the threshold voltages of diode-connected transistors M26-M29. This speeds up the rise of positive-going output signals. The output signals on lines O0...O3 are then applied to a dynamic output latch that includes clocked transmission gates T5-T12; when CLOCK is high (and CLOCK is low), the transmission gates allow the output signals to pass to inverters I5-I8, producing the desired output terms Y0...Y3. Still other types of output circuitry may be provided as desired.

Note that the foregoing description has illustra-

tively been given for n-channel logic transistors and p-channel precharge and load transistors, as is typical with CMOS technology. However, the opposite conductivity types are possible for these functions.

Claims

1. An integrated circuit including a programmable logic array having an AND plane and an OR plane, wherein said AND plane includes conductive AND logic lines (A0...A3), a conductive delay line (AR), precharge transistors (M5...M1) controllable by a clock for charging the AND logic lines and the delay line to a high voltage level during a first clock state, and at least one capacitive load transistor (M34, M35) connected to the delay line, characterized in that said OR plane includes conductive OR logic lines (00...03), and clocked load transistors (M17...M20) for continually pulling the OR logic lines toward a high voltage level during a second clock state while the OR logic transistors (M21...M25) are performing a logic decode operation, said conductive delay line (AR) is directly connected to the control electrodes of said clocked load transistors in the OR plane, and said AND plane includes at least one capacitive load transistor (M14, M15) connected to the control electrode of a discharge transistor (M16) for discharging said delay line (AR) to a low voltage level during said second clock state in order to delay the discharge of said delay line relative to said logic lines.
2. A circuit as claimed in claim 1 including input drivers (G2...G5) connected to logic transistors (M6...M13) in said AND plane, and wherein the number of the capacitive load transistors (M14, M15) connected to the control electrode of said discharge transistor (M16) is sufficient to match the worst case loading seen by any of said input drivers.
3. A circuit as claimed in claim 1 or 2 wherein the number of capacitive load transistors (M34, M35) connected to said delay line (AR) is sufficient to match the worst case loading seen by any of said AND logic lines (A0...A3).

Patentansprüche

1. Integrierte Schaltung mit einem programmierbaren Logikarray, das eine UND-Ebene und eine ODER-Ebene besitzt, wobei die UND-Ebene leitende UND-Logikleitungen (A0...A3), eine leitende Verzögerungsleitung (AR), Vorla-

detransistoren (M5...M1), die zur Ladung der UND-Logikleitungen und der Verzögerungsleitung auf einen hohen Spannungspegel durch ein Taktsignal während eines ersten Taktzustandes steuerbar sind, und wenigstens einen kapazitiven Lasttransistor (M34, M35) enthält, der an die Verzögerungsleitung angeschlossen ist,

dadurch gekennzeichnet,

daß die ODER-Ebene leitende ODER-Logikleitungen (00...03) und getaktete Lasttransistoren (M17...M20) enthält, um die ODER-Logikleitungen kontinuierlich auf einen hohen Spannungspegel während eines zweiten Taktzustandes zu ziehen, solange die ODER-Logiktransistoren (M21...M25) eine logische Decodieroperation durchführen,

daß die leitende Verzögerungsleitung (AR) direkt an die Steuerelektrode des getakteten Lasttransistors in der ODER-Ebene angeschlossen ist, und

daß die UND-Ebene wenigstens einen kapazitiven Lasttransistor (M14, M15), enthält, der an die Steuerelektrode eines Entladungstransistors (M16) zur Entladung der Verzögerungsleitung (AR) auf einen niedrigen Spannungspegel während des zweiten Taktzustand angeschlossen ist, um die Entladung der Verzögerungsleitung relativ zu den Logikleitungen zu verzögern.

2. Schaltung nach Anspruch 1,

dadurch gekennzeichnet,

daß Eingangstreiber (G2...G5) vorgesehen sind, die an die Logiktransistoren (M6...M13) in der UND-Ebene angeschlossen sind, und daß die Anzahl der kapazitiven Lasttransistoren (M14, M15), die mit der Steuerelektrode des Entladetransistors (M16) verbunden sind, ausreichend ist, um die Worst-Case-Belastung, die von irgendeinem der Eingangstreiber gesehen wird, anzupassen.

3. Schaltung nach einem der Ansprüche 1 oder 2,

dadurch gekennzeichnet,

daß die Anzahl der kapazitiven Ladetransistoren (M34, M35), die an die Verzögerungsleitung (AR) angeschlossen sind, ausreichend ist, um die Worst-Case-Belastung, die von irgendeiner der UND-Logikleitungen (A0...A3) gesehen wird, anzupassen.

Revendications

1. Circuit intégré comprenant un réseau logique programmable ayant un plan-ET et un plan-OU, dans lequel le plan-ET contient des lignes

tively been given for n-channel logic transistors and p-channel precharge and load transistors, as is typical with CMOS technology. However, the opposite conductivity types are possible for these functions.

Claims

1. An integrated circuit including a programmable logic array having an AND plane and an OR plane, wherein said AND plane includes conductive AND logic lines (A0...A3), a conductive delay line (AR), precharge transistors (M5...M1) controllable by a clock for charging the AND logic lines and the delay line to a high voltage level during a first clock state, and at least one capacitive load transistor (M34, M35) connected to the delay line, characterized in that said OR plane includes conductive OR logic lines (00...03), and clocked load transistors (M17...M20) for continually pulling the OR logic lines toward a high voltage level during a second clock state while the OR logic transistors (M21...M25) are performing a logic decode operation, said conductive delay line (AR) is directly connected to the control electrodes of said clocked load transistors in the OR plane, and said AND plane includes at least one capacitive load transistor (M14, M15) connected to the control electrode of a discharge transistor (M16) for discharging said delay line (AR) to a low voltage level during said second clock state in order to delay the discharge of said delay line relative to said logic lines.

2. A circuit as claimed in claim 1 including input drivers (G2...G5) connected to logic transistors (M6...M13) in said AND plane, and wherein the number of the capacitive load transistors (M14, M15) connected to the control electrode of said discharge transistor (M16) is sufficient to match the worst case loading seen by any of said input drivers.

3. A circuit as claimed in claim 1 or 2 wherein the number of capacitive load transistors (M34, M35) connected to said delay line (AR) is sufficient to match the worst case loading seen by any of said AND logic lines (A0...A3).

Patentansprüche

1. Integrierte Schaltung mit einem programmierbaren Logikarray, das eine UND-Ebene und eine ODER-Ebene besitzt, wobei die UND-Ebene leitende UND-Logikleitungen (A0...A3), eine leitende Verzögerungsleitung (AR), Vorla-

detransistoren (M5...M1), die zur Ladung der UND-Logikleitungen und der Verzögerungsleitung auf einen hohen Spannungspegel durch ein Taktsignal während eines ersten Taktzustandes steuerbar sind, und wenigstens einen kapazitiven Lasttransistor (M34, M35) enthält, der an die Verzögerungsleitung angeschlossen ist,

dadurch gekennzeichnet,

daß die ODER-Ebene leitende ODER-Logikleitungen (00...03) und getaktete Lasttransistoren (M17...M20) enthält, um die ODER-Logikleitungen kontinuierlich auf einen hohen Spannungspegel während eines zweiten Taktzustandes zu ziehen, solange die ODER-Logiktransistoren (M21...M25) eine logische Decodieroperation durchführen,

daß die leitende Verzögerungsleitung (AR) direkt an die Steuerelektrode des getakteten Lasttransistors in der ODER-Ebene angeschlossen ist, und

daß die UND-Ebene wenigstens einen kapazitiven Lasttransistor (M14, M15), enthält, der an die Steuerelektrode eines Entladungstransistors (M16) zur Entladung der Verzögerungsleitung (AR) auf einen niedrigen Spannungspegel während des zweiten Taktzustand angeschlossen ist, um die Entladung der Verzögerungsleitung relativ zu den Logikleitungen zu verzögern.

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

daß Eingangstreiber (G2...G5) vorgesehen sind, die an die Logiktransistoren (M6...M13) in der UND-Ebene angeschlossen sind, und daß die Anzahl der kapazitiven Lasttransistoren (M14, M15), die mit der Steuerelektrode des Entladetransistors (M16) verbunden sind, ausreichend ist, um die Worst-Case-Belastung, die von irgendeinem der Eingangstreiber gesehen wird, anzupassen.

3. Schaltung nach einem der Ansprüche 1 oder 2,

dadurch gekennzeichnet,

daß die Anzahl der kapazitiven Lasttransistoren (M34, M35), die an die Verzögerungsleitung (AR) angeschlossen sind, ausreichend ist, um die Worst-Case-Belastung, die von irgendeiner der UND-Logikleitungen (A0...A3) gesehen wird, anzupassen.

Revendications

1. Circuit intégré comprenant un réseau logique programmable ayant un plan-ET et un plan-OU, dans lequel le plan-ET contient des lignes



logiques ET (A0... A3), une ligne de retard conductrice (AR), des transistors de précharge (M5...M1) pouvant être commandés par un signal d'horloge pour charger les lignes logiques ET et la ligne de retard à un niveau de tension haut pendant un premier état du signal d'horloge, et au moins un transistor de charge capacitif (M34,M35) connecté à la ligne de retard, caractérisé en ce que le plan-OU précité contient des lignes logiques OU conductrices (00...03), et des transistors de charge cadencés (M17...M20) pour tirer de façon continue les lignes logiques OU vers un niveau de tension haut pendant un second état du signal d'horloge tandis que les transistors logiques OU (M21...M25) exécutent une opération de décodage logique, ladite ligne de retard conductrice (AR) est directement connectée aux portes des transistors de charge cadencés dans le plan-OU, et ledit plan-ET contient au moins un transistor de charge capacitif (M14, M15), connecté à l'électrode de commande d'un transistor de décharge (M16) afin de décharger ladite ligne de retard (AR) jusqu'à un niveau de tension bas pendant le second état du signal d'horloge de manière à retarder la décharge de la ligne de retard par rapport aux lignes logiques précitées.

2. Circuit selon la revendication 1, comprenant des dispositifs de commande d'entrée (G2...G5) connectés à des transistors logiques (M6...M13) dans le plan-ET précité, et dans lequel le nombre de transistors de charge capacitifs (M14,M15) connectés à l'électrode de commande dudit transistor de décharge (M16) est suffisant pour s'adapter au plus mauvais cas de charge vue par l'un quelconque des dispositifs de commande d'entrée.

3. Circuit selon la revendication 1 ou 2, dans lequel le nombre de transistors de charge capacitifs (M34,M35) connectés à la ligne de retard (AR) est suffisant pour s'adapter au plus mauvais cas de charge vue par l'une quelconque des lignes logiques ET précitées (A0... A3)

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