USE OF AN INSULATOR SPACER ON THE SIDEWALLS OF A VIA HOLE

ABSTRACT

A process for creating insulator spacers, on the sides of a sub-micron diameter via hole, has been developed. The process features the deposition of an insulator layer, followed by an anisotropic dry etching procedure, creating the insulator spacer. The insulator spacer is used to encapsulate polymer residue material, deposited on the sides of the sub-micron diameter via hole, during the via hole formation process. The insulator spacers are also used to cover the exposed sides of a SOG layer, for cases in which the sub-micron diameter via hole was formed in a composite interlevel dielectric layer, with a SOG layer used as one of the layers. Insulator spacers are also used to fill undercut regions in sub-micron diameter via holes, formed in a composite interlevel dielectric layer, where one of the layers of the composite layer is subjected to a larger isotropic etching component, than the other layers of the composite interlevel dielectric layer.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)