WHAT IS CLAIMED IS:

[Claim 1]. A semiconductor device, comprising:

gate layers and insulating layers that are parallel to each other and stacked alternatingly along a first direction and form a stack;

an array of channel structures being formed in an array region of the stack;

a first staircase formed at a first section in a connection region of the stack, the connection region and the array region arranged in a second direction perpendicular to the first direction;

a second staircase formed at a second section in the connection region of the stack; and

a dummy staircase formed at the first section and disposed between the first staircase and the second staircase, the dummy staircase including dummy group stair steps descending in the second direction, and dummy division stair steps descending in a third direction and a fourth direction that are perpendicular to the second direction, and the first direction and opposite to each other,

wherein the first staircase includes first group stair steps descending in the second direction and first division stair steps descending in the third direction and the fourth direction,

wherein the second staircase includes second group stair steps descending in the second direction and second division stair steps descending in the third direction and the fourth direction,

wherein the first group stair steps, the second group stair steps and the dummy group stair steps all have a same width as a width of all of the first division stair steps, second division stair steps and dummy division stair steps measured along the third and fourth directions.

[Claim 2]. The semiconductor device of claim 1, wherein:

the first staircase is positioned over the second staircase,

wherein each stair step of the first group stair steps has a height of multiple pairs of the gate layers and the insulating layers in the first section, and

each stair step of the first division stair steps has a height of one pair of the gate layer and the insulating layer in the first section.

[Claim 3]. The semiconductor device of claim 1, wherein:

a height difference of two consecutive first group stair steps of the first group stair steps in the first direction is equal to a height of N pairs of the gate layers and the insulating layers in the first section, and

a height difference of two consecutive first division stair steps of the first division stair steps in the first direction is equal to a height of one pair of the gate layer and the insulating layer in the first section, the N being greater than one.

[Claim 4]. The semiconductor device of claim 3, wherein:

the dummy staircase has a same height as the first staircase,

the dummy staircase is positioned over the second staircase.

[Claim 5]. The semiconductor device of claim 2, wherein:

each step of the second group stair steps has a height of multiple pairs of the gate layers and the insulating layers in the second section, and

each stair step of the second division stair steps has a height of one pair of the gate layer and the insulating layer in the second section.

[Claim 6]. The semiconductor device of claim 5, wherein each stair step of the dummy group stair steps has a height of the multiple pairs of the gate layers and the insulating layers in the first section.

[Claim 7]. The semiconductor device of claim 5, wherein corresponding group stair steps of the first group stair steps in the first staircase and the second group stair steps in the second staircase are of a same height.

[Claim 8]. The semiconductor device of claim 5, wherein each stair step of the first group stair steps and the second group stair steps is formed of multiple division stair steps.

[Claim 9]. The semiconductor device of claim 1, further comprising:

a third staircase formed of a third section in the connection region of the stack that corresponds to gate top select transistors in the channel structures.

[Claim 10]. The semiconductor device of claim 1, wherein the first section in the connection region of the stack and the second section in the connection region of the stack have a same number of gate layers.

[Claim 11]. The semiconductor device of claim 1, further comprising:

first contact structures formed on the first staircase, the first contact structures being connected to the gate layers at the first section in the connection region of the stack.

[Claim 12]. The semiconductor device of claim 11, further comprising:

second contact structures formed on the second staircase the second contact structures being connected to the gate layers at the second section in the connection region of the stack.

[Claim 13]. The semiconductor device of claim 12, wherein no contact structures are formed on the dummy staircase.

[Claim 14]. The semiconductor device of claim 1, wherein first contact structures formed on the first staircase and being connected to the gate layers at the first section in the connection region of the stack, a first one and a second one of the first contact structures neighboring to each other in the second direction and having different lengths extending in the first direction, the first one and a third one of the first contact structures neighboring to each other in a third direction perpendicular to the second direction and the first direction and having different lengths extending in the first direction.

[Claim 15]. The semiconductor device of claim 14, wherein:

the first one and a fourth one of the first contact structures neighbor to each other in a fourth direction perpendicular to the second direction and opposite to the third direction, and have different lengths extending in the first direction.

[Claim 16]. The semiconductor device of claim 14, further comprising:

second contact structure formed on the second staircase and being connected to the gate layers at the second section in the connection region of the stack,

wherein some of the first contact structures arranged in a row in the third direction are of a same number as some of the second contact structures arranged in the row in the third direction,

some of the first contact structures arranged in a row in the fourth direction are of a same number as some of the second contact structures arranged in the row in the fourth direction.

[Claim 17]. The semiconductor device of claim 14, wherein the first section in the connection region of the stack and the second section in the connection region of the stack have a same number of the gate layers.