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Declarations under Rule 4.17:

[Continued on next page]

(54) Title: DUAL POWER SCHEME IN MEMORY CIRCUIT

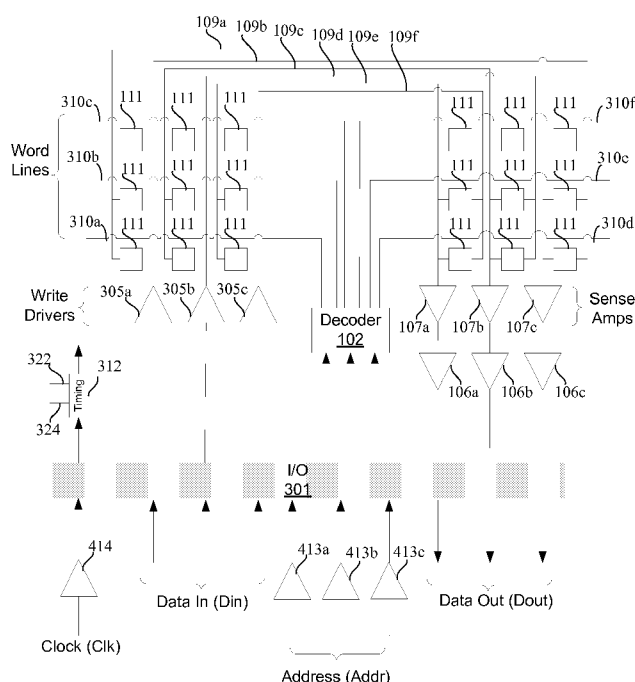


FIG. 3

(57) Abstract: A semiconductor memory device includes address signal level shifters configured to transform a low level address signal into a higher level address signal. A decoder (102) is configured to receive the higher level address signal and, in response, provide word line signals. Write drivers (305) receive low level data input signals and configure bitlines (109) in response to the received input. Memory cells (111) are responsive to the word line signals and to the configured bit lines for storing data therein.



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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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