

CACHE COHERENCY PROTOCOL INCLUDING AN H_R STATE**ABSTRACT**

A cache and method of maintaining cache coherency in a data processing system (8) are described. The data processing system (8) includes a system memory (18), processors, (10a,10n) and multiple caches (12a,12n,14a,14n,15a) coupled to an interconnect (16). Accordingly to the method, a first data item and its corresponding address tag (40) are stored in a first of the caches. A coherency indicator in the first cache is set to a first state indicating a valid address tag (40) and an invalid first data item. If the indicator is set to the first state and the first cache detects data transfer on the interconnect (16), where the data transfer includes another data item, this data item is stored in the first cache with the address tag (40). Also the indicator updates to a second state that indicates a valid second data item and that the first cache can supply the second data item in response to a request.

Fig.2

This Sheet Has Been Replaced



THIS SHEET HAS BEEN
REPLACED