A NEW PROCEDURE FOR FORMING A LIGHTLY-DOPED-DRAIN STRUCTURE

ABSTRACT

A method for fabrication of a lightly-doped-drain (LDD) structure for self aligned polysilicon gate MOSFETs is described wherein a polymer layer, formed along the sidewall during the patterning process of the polysilicon gate electrode, is used to mask the source/drain ion implant. The sidewall polymer layer replaces the conventional silicon oxide sidewall as an LDD spacer and offers improved thickness control as well as an improved sequence of processing steps whereby the deposition of a spacer oxide layer onto the gate oxide is eliminated. A cap oxide layer first deposited over the gate polysilicon layer. This oxide layer is then patterned and etched using RIE under conditions which form a polymer sidewall layer along the edges of the cap oxide pattern. The polysilicon layer is then etched, and has a pattern concentric with the cap oxide pattern but wider by the thickness of the polymer sidewall. After removal of the polymer and residual photoresist, the source/drain implant is performed, followed by removal of the polysilicon lip by RIE using the cap oxide as a mask. The LDD implant is then performed.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)