

INVERSE TRANSPORT PROCESSOR WITH
MEMORY ADDRESS CIRCUITRY

Abstract of the Disclosure

An inverse transport processor for a TDM packet signal TV receiver which selectively extracts and couples desired payloads of program component data to a common buffer memory. A microprocessor (19) also couples data to the common buffer memory (18). The respective payloads and microprocessor data are stored in the common buffer memory in response to associated memory addresses from a multiplexer (17). A decryption device (16) decrypts payload data according to packet specific decryption keys. A detector (15) detects payloads including entitlement data. Payloads containing entitlement data are directed to a smart card which generates the packet specific decryption keys. A memory data output is coupled to respective program component processors (21- 24). Responsive to data requests and data write requests, memory access for read and write functions is arbitrated (17) so no incoming program data is lost, and all component processors are serviced.

Figure 3