

1 519 831

PATENT SPECIFICATION

(11) 1 519 831



- (21) Application No. 25370/75
- (22) Filed 13 June 1975
- (31) Convention Application No. 7409034
- (32) Filed 17 June 1974 in
- (33) Netherlands (NL)
- (44) Complete Specification published 2 Aug. 1978
- (51) INT CL² H01C 10/06 H01L 29/68 H03G 3/00
- (52) Index at acceptance

H3T 1U1 2A1S 2J 3J 4A2 4C 4D 4E1N 4E2N 4F 4P 4X 5E
 H1K 1C1 4C11 9B4X 9E 9R AA FX
 H4R 18AX

(54) SYMMETRICAL CIRCUIT ARRANGEMENT FOR FORMING A VARIABLE A.C. RESISTANCE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a symmetrical circuit arrangement for forming a variable alternating-current resistance between first and second terminals thereof, which arrangement comprises a series combination of first and second *pn* junctions which are connected back-to-back, which series combination is connected between said first and second terminals.

One such arrangement is described, for example, in IEEE Transactions on Broadcast and Television Receivers, August 1972, pages 158—162, and is connected, for example, between the emitters of two transistors which together act as a differential amplifier. A control current is applied to the common point of two junctions so as to forward-bias them, and variation of the control current varies the ac-resistance of the arrangement and hence the gain of the amplifier. The value of the control current through the two *pn* junctions determines their differential resistance (small-signal alternating-current resistance), and this differential resistance in turn determines the degree of negative signal feedback and hence the gain of the amplifier.

The differential resistance of a *pn* junction acts as a linear variable resistance for the signal currents as long as the ratio between the signal current and the control current remains small. With progressive control, however, the signal current increases and the control current

decreases, so that the differential resistance of the *pn* junctions is no longer varied only by the control current but is also varied by the signal current. This gives rise to signal distortion, modulation distortion, cross-modulation and the like.

It is an object of the invention to mitigate this disadvantage.

According to one aspect the invention provides a symmetrical circuit arrangement for forming a variable alternating-current resistance between first and second terminals thereof, said arrangement comprising a first series combination of first and second *pn* junctions which are connected back-to-back, which first series combination is connected between said first and second terminals, a second series combination of a first resistor, third and fourth *pn* junctions and a second resistor in that order, said third and fourth *pn* junctions being connected back-to-back in the same sense with respect to each other as are the first and second *pn* junctions, which second series combination is connected in parallel with said first series combination in such manner that the first resistor is connected to said first terminal and the second resistor is connected to said second terminal, a connection between the common point of the first and second *pn* junctions and the common point of the third and fourth *pn* junctions, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a bias current source circuit connected between said reference point and a first further point being the common point of the first resistor and the third *pn* junction and between said reference point and a second further point being the common point of the second resistor and the fourth *pn* junction in such manner that an impedance is present between said first and second further

50

55

60

65

70

75

80

85

90

(44)(15)

2
5 points, for setting up a potential difference across the series combination of the first resistor and the first load and across the series combination of the second resistor and the second load and for supplying forward current to said first, second, third and fourth *pn* junctions, and a controllable sink for output current of said bias current source circuit, which sink is connected between said reference point and the common point of the first, second, third and fourth *pn* junctions so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value said third and fourth *pn* junctions will conduct before said first and second *pn* junctions conduct.

10
15
20 According to another aspect the invention provides a symmetrical circuit arrangement for forming a variable alternating current resistance between first and second terminals thereof, said arrangement comprising an elongate *pn* junction between a first resistive region in a semiconductor chip and a second region is said chip, which second region is of opposite conductivity type to said first region, the first and second terminals being provided on said first region adjacent first and second portions of said *pn* junction respectively, a third terminal provided on said first region adjacent a third portion of said *pn* junction, which third portion lies substantially midway between said first and second portions on going along said junction, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a bias current source connected between said reference point and said third terminal for setting up a potential difference across the series combination of the first load and that portion of the first region which lies between said first and third terminals and across the series combination of the second load and that portion of the first region which lies between the second and third terminals and for supplying forward current to said *pn* junction, and a controllable sink for output current of said bias current source, which sink is connected between said reference point and said second region so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value an increasing portion of said *pn* junction will become conductive and an increasing portion of the impedance presented between said first and second terminals by said first region will become shunted by a current path which extends through said second region, so reducing the impedance between said first and second terminals.

According to another aspect the invention provides a symmetrical circuit arrangement for forming a variable alternating current resistance between first and second terminals thereof, said arrangement comprising first and second elongate *pn* junctions between a first resistive region in a semiconductor chip and second region in said chip and between a further resistive region in said chip and said second region respectively, said region being of opposite conductivity type to said first and further regions, said first and second terminals being provided on said first and further regions respectively adjacent a first portion of said first *pn* junction and a first portion of said second *pn* junction respectively, a third terminal provided on said first region adjacent a second portion of said first *pn* junction, a fourth terminal provided on said further region adjacent a second portion of said second *pn* junction, the spacing between said first and second portions of the first *pn* junction on going along said first *pn* junction being substantially equal to the spacing between said first and second portions of the second *pn* junction on going along said second *pn* junction, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a first bias current source connected between said reference point and said third terminal for setting up a potential difference across the series combination of the first load and the first region and for supplying forward current to said first *pn* junction, a second bias current source connected between said reference point and said fourth terminal for setting up a potential difference across the series combination of the second load and the further region and for supplying forward current to said second *pn* junction, and a controllable sink for output currents of said bias current sources, which sink is connected between said reference point and said second region so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value increasing portions of said first and second *pn* junctions will become conductive and an increasing portion of the impedance presented between said first and second terminals by said first and further regions will become shunted by a current path which extends through said second region, so reducing the impedance between said first and second terminals.

The arrangement may, for example, be connected between the emitters of a differential-amplifier transistor pair or be incorporated in other types of symmetrical

circuits in which a variable alternating-current resistance is required, for example in modulators, demodulators, mixer stages and the like.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of a first embodiment,

Figure 2 shows a second embodiment,

Figures 3a and 3b show part of a third embodiment,

Figures 4a and 4b show part of a fourth embodiment,

Figures 5a and 5b show part of a fifth embodiment,

Figure 6 shows a sixth embodiment, and

Figures 7a and 7b show part of a seventh embodiment.

Figure 1 shows an amplifier comprising amplifier transistors 1 and 2 which have emitter resistors 3 and 4 respectively and collector resistors 5 and 6 respectively. The signal to be amplified is applied between the bases of the transistors 1 and 2, and the amplified signal can be derived from between the two collectors. The bases are maintained at equal direct-voltage potentials in a manner not shown. A symmetrical circuit arrangement for forming a variable alternating-current resistance between first and second terminals 7 and 8 thereof is included between the emitters of the transistors. The circuit between the terminals 7 and 8 comprises two series-connected *pn* junctions in the form of the emitter-base junctions of two *pn* transistors 10 and 11 which are connected back-to-back. A connection 31 between the bases of the transistors 10 and 11 is connected to a device 30 which carries a control current I_c for controlling the alternating-current resistance between the terminals 7 and 8 and hence for controlling the gain of the entire amplifier. The device 30 is shown in the Figure by means of the current source symbol in order to emphasize that it has a comparatively high impedance, i.e. the internal resistance of the device 30 is high compared with the resistance of the circuit connected to it. Owing to this high internal resistance of the device 30 the signal current which flows between the terminals 7 and 8 cannot flow away to earth via the device 30.

The base-emitter junction of the transistor 10 is shunted by the series combination of a resistor 12 and the emitter-base junction of a transistor 13, and similarly the emitter-base junction of the transistor 11 is shunted by the series combination of a resistor 14 and the emitter-base junction of a transistor 15. The emitter-base junction of the transistor 13 is

in turn shunted by the series combination of a resistor 16 and the emitter-base junction of a transistor 17, and the emitter-base junction of the transistor 15 is shunted by the series combination of a resistor 18 and the emitter-base junction of a transistor 19. Thus a ladder network of series combinations of resistors and *pn* junctions is produced which is desired may be extended at will. A bias-current source in the form of a resistor 200 connected to the positive supply voltage is connected via a terminal 9 and a resistor 21 to the emitter of one end-transistor 17 of the ladder network and via the terminal 9 and a resistor 22 to the emitter of the other end-transistor 19 of the ladder network. The bias-current source provides a bias current I one half of which flows through the resistor 21 to the junction point of 16 and 17 and the other half of which flows through the resistor 22 to the junction point of 18 and 19. The collectors of the transistors 10, 11, 13, 15, 17 and 19 are interconnected but otherwise float.

To illustrate the operation of the circuit of Figure 1 it will be assumed that the control current I_c is initially zero. When this is so all the emitter-base junctions of the transistors 10, 11, 13, 15, 17 and 19 will be cut off, and signal current will flow between the terminals 7 and 8 via the resistors 12, 16, 21, 22, 18 and 14. Hence there is a high amount of alternating-current resistance between the terminals 7 and 8 so that the gain of the amplifier stage is small.

Direct currents $I/2$ flow through the resistors 21, 16 and 12 to the terminal 7 and through the resistors 22, 18 and 14 to the terminal 8 respectively. As a result, the emitters of the transistors 13 and 15 are more positive than the emitters of the transistors 10 and 11 and, in turn, the emitters of the transistors 17 and 19 are more positive than the emitters of the transistors 13 and 15.

If now the control device 30 starts to sink small control current I_c , the transistors 17 and 19 will become conducting owing to their emitter potentials being the most positive, whereas the remaining transistors 10, 11, 13 and 15 remain cut off for the time being. The signal current between the terminals 7 and 8 now flows via the elements 12, 16, 17, 19, 18 and 14, which path has an appreciably lower resistance than that which includes the resistors 21 and 22. Hence the coupling between the transistors 1 and 2 and consequently the gain has increased.

With further increases in the control current first the transistors 13 and 15 and then the transistors 10 and 11 will become conducting. Owing to the gradually decreasing alternating-current resistance in

the circuit between the terminals 7 and 8 the gain will progressively increase. This during a considerable part of the alternating-current resistance between the terminals 7 and 8 is constituted by linear resistors, which do not give rise to signal distortion.

If desired the emitter-base junctions of the transistors 10, 11, 13, 15, 17 and 19 can be replaced by diodes. In a practical version of the circuit arrangement of Figure 1 the resistors 12—22 has increasing values, as follows:

resistors 12 and 14: 68 ohms
resistors 16 and 18: 220 ohms
resistors 21 and 22: 680 ohms.

The components 10—22, with the transistors replaced by diodes, may be realized in integrated-circuit form in the manner shown diagrammatically in Figure 2. The interconnected regions of the diodes, corresponding to the bases of the transistors of Figure 1, are formed by a single *n*-type region 23 of a semiconductor body 24; the control device or current sink 30 is connected to this region via the terminal 31. The other regions of the diodes, corresponding to the emitters of the transistors of Figure 1, and the series resistors of the ladder network are formed by a single *p*-type region 25. The terminals 7 and 8 for the signal current are provided one at each end of the region 25, and the terminal 9 for connection to the bias current source 20 is connected to the centre of the region 25. The discrete emitter-base junctions of the arrangement of Figure 1 are replaced by the distributed *pn* junctions located along the *pn* junction 26 between the regions 23 and 25; the intrinsic distributed resistance of the region 25 between the terminals 7 and 9 replaces the discrete resistors 12, 16 and 21 of Figure 1, and the intrinsic distributed resistance of the region 25 between the terminals 8 and 9 replaces the discrete resistors 14, 18 and 22 of Figure 1. For the time being it will be assumed that the intrinsic resistance of the region 23 is considerably smaller than that of the region 25. (If this is not the case, the influence of the intrinsic resistance of the region 23 can be reduced or neutralized by suitable steps which will be described hereinafter.)

If the control current I_c is zero, the *pn* junction 26 is blocked throughout its length and signal current can only flow from the terminal 7 to the terminal 8 and *vice versa* through the comparatively high-resistance material of the region 25. Hence there is a large and linear alternating-current resistance between the terminals 7 and 8. One half of the bias current I flows from the

terminal 9 to the terminal 7, the other half flowing from the terminal 9 to the terminal 8. The voltage drop across the intrinsic resistance of the region 25 produced by this current causes the region 25 to be more positive in the vicinity of the terminal 9 than in the vicinity of the terminals 7 and 8. If now device 30 sinks a small control current I_c , only a small part of the *pn* junction 26 will become conducting, namely the part which is close to the terminal 9, because this portion of the region 25 is most positive. The alternating current will then follow the path indicated by a broken line from the terminal 7 through the left hand portion of the region 25, then through the central portion of the region 23 and finally through the righthand portion of the region 25 to the terminal 8. Because part of the alternating-current path thus extends through the low-resistance region 23, the alternating-current resistance has become lower. As the control current is increased still further a proportionally larger part of the signal current path runs through the region 23 so that the alternating-current resistance is correspondingly reduced. Eventually the signal current will cross immediately from the terminal 7 to the region 23 and return from the region 23 to the region 25 only at the terminal 8.

The intrinsic resistance of the region 23 may be reduced or shunted in various ways, and these may be employed singly or in various combinations. These ways are as follows:—

1) A further region (see Figure 3a, region 27) which adjoins the region 23 and which is of the same conductivity type as the region 25 may be provided in such a manner that transistor action is produced between the resulting three regions. The part of the signal current which flows into the region 23 (base) from the region 25 (emitter) will now cross to the region 27 (collector). If the resistance of the region 27 is sufficiently low, the signal current will find an easy path through this region.

2) A conductive layer may be connected to various parts of the region 23 or of the aforementioned further region to shunt the intrinsic resistance of this region.

3) A buried layer may be provided underneath the region 23, which buried layer is made of a semiconductor material of the same conductivity type as the region 23 but is more heavily doped.

4) The geometry of the regions may be chosen so that there is a long path length from the terminal 7 to the terminal 8 through the region 25 and a short path length from the terminal 7 to the terminal 8 through the region 23, causing the effective alternating-current resistance of the region

25 to be increased and that of the region 23 to be reduced (see Figures 4a and 4b).

Figure 3 shows how an arrangement incorporating possibilities (1), (2) and (3) above may be obtained in practice. Manufacture starts in known manner from a *p*-type semiconductor substrate in which a *n*-type buried layer 23' (Figure 3a) has been formed by diffusion. An *n*-type epitaxial surface region 23 is then formed on top of the buried layer 23'. Two surface regions 25 and 27 are then formed in the region 23 by diffusion of *p*-type impurities, the region 25 being of elongate form and being entirely surrounded by the region 27. Thus a lateral *pn*p transistor is produced having an emitter 25, a base 23 and a collector 27. The assembly is then covered by an insulating layer in which contact openings are made at the locations indicated by shading for providing contacts to the various regions by means of leads which are shown in Figure 3b. A first lead, which forms the terminal 7, is connected to an end of the region 25 through a contact opening 32. A second lead, which forms the terminal 8, is connected to the other end of the region 25 through a contact opening 34, and a third lead, which forms the terminal 9, is connected to the centre of the region 25 through a contact opening 33. A lead which forms the terminal 31 is connected to the region 23 through a contact opening 35, and a conductor 39 interconnects all the contact openings 36, 37, 38, thereby interconnecting various locations of the region 27. The conductor 39 serves to shunt the intrinsic resistance of the region 27 and hence, indirectly and in conjunction with the buried layer 23', the intrinsic resistance of the region 23, so that an equipotential plane is produced in region 23 at the *pn* junction 26 both for signal current and for direct current.

The leads 9 and 31 are connected to a bias current source and to a controllable sink for the bias current respectively in the manner shown in Figure 1, which source and sink may be provided on the same semiconductor chip. The leads 7 and 8 are connected to a signal current circuit, for example to the emitters of the two *npn* transistors 1 and 2 of Figure 1, which is preferably also accommodated on the same semiconductor chip.

It will be realized that the terminals 7 and 8 have to be dc-connected to the circuit to be controlled, because the difference between the bias current and the control current is conducted away through them i.e. through the resistors 3 and 4 in Figure 1 which act as loads at the terminals 7 and 8. If it is required that the direct current through terminals 7 and 8 be constant, the

output current of source 20 may be varied in the same sense as the control current.

Figure 4 shows how an arrangement incorporating possibilities (2), (3) and (4) may be obtained in practice. The parts of the semiconductor chip of Figures 4a and 4b which correspond to various parts of the chip of Figures 3a and 3b have been given the same reference numerals. In this embodiment the region 25 is formed in the shape of a U so that the two ends to which the terminals 7 and 8 are connected through the contact openings 32 and 34 are spaced by only a small distance. The path through the region 23 through which the signal current flows when the control current is a maximum is in consequence very short so that the intrinsic resistance of the region 23, which in any case is shunted by the buried layer 23', no longer plays an important part in the operation of the arrangement. Hence a further region as shown in Figure 3 at 27 has not been provided. The lead 31 for conducting the control current from the region 23 through the contact opening 35 preferably extends deep into the horse-shoe shape of the region 25 as shown, so that the control current can be taken from any portion of the *pn* junction 26 without appreciable resistance. In this is so then, when the control current is small, only the portion of the *pn* junction near the terminal 9 will become conducting, the remaining portions only becoming conducting when the control current is increased.

When the control current taken from the terminal 31 is a maximum the signal current will follow the shortest path between the terminals 7 and 8 and the resistance to the signal current between these terminals will be a minimum. Normally, however, this minimum resistance will still comprise at least twice the differential resistance (of a few tens of ohms) of a *pn* junction, because the signal current passes through the *pn* junction twice. This minimum resistance can be considerably reduced, in the configuration of Figure 4a by making the two limbs of the U-shaped region 25 approach each other so closely that a transistor is formed in conjunction with the intermediate portion of the region 23, as shown in Figure 5a. In order to achieve this the width (*w*) of the region 23 between the two limbs of the region will have to be smaller than the diffusion length of minority carriers in the region 23. Since there will then be no room between the said two limbs for making contact to the region 23, contact openings 35 for this purpose are shown in Figure 5 disposed externally of the U-shaped region 25. Figure 5b shows the contact openings of Figure 5a with

conductive strips provided thereon for making the various electric connections.

When the maximum control current is carried by the terminal 31, the portion of the *p*-type region 25 in close proximity to the contact opening 32 and the portion of the *p*-type region 25 in close proximity to the contact opening 34 in conjunction with narrow intermediate portion of the *n*-type region 23 will constitute a lateral *pn*p transistor which is in the saturated condition. As is known, such a transistor constitutes only a very small alternating-current resistance (of a few ohms) between its collector and its emitter (the terminals 7 and 8).

The embodiments shown may be modified in various ways. For example, in the embodiment shown in Figure 1 the bias current source, which is connected to the ladder network of diodes and resistors through two resistors 21 and 22, may be replaced by a current source circuit comprising two effectively separate current sources, for example two large-value resistors connected to the positive supply. If this is done the alternating-current resistance between the terminals 7 and 8 in the non-controlled condition will be very high, resulting in an increased control range which however, will generally be at the expense of signal handling capability. If the arrangement of Figure 2 is modified according to this principle, Figure 6 will be obtained. In Figure 6 the region 25 is interrupted at its centre so that two identical part-regions 25a and 25b are formed, two current sources 20a and 20b being connected by terminals 9a and 9b respectively, one on each side of the interruption, to the part-regions 25a and 25b respectively.

Figures 7a and 7b show an embodiment obtained by applying the principle of interrupting the region 25 to the embodiment of Figures 5a and 5b, corresponding reference numerals being used for corresponding components in the two sets of Figures. An elongate lateral *pn*p transistor is obtained in which both ends of one main electrode region 25a and both ends of the other main electrode region 25b are provided with terminals (7, 9a and 8, 9b respectively). The terminals 7 and 8 serve for connecting to the circuit to be controlled whilst the terminals 9a and 9b serve for connection to the current sources 20a and 20b respectively.

In the arrangement of Figure 1 the semiconductor elements 10, 11, 13, 15, 17 and 19 may have their polarities reversed if the directions of the currents I and I₁ are also reversed. Similarly, in Figures 2 to 7 the conductivity types of the various regions may be interchanged if the

polarities of the control current and the bias current are also reversed.

WHAT WE CLAIM IS:—

1. A symmetrical circuit arrangement for forming a variable alternating-current resistance between first and second terminals thereof, said arrangement comprising a first series combination of first and second *pn* junctions which are connected back-to-back, which first series combination is connected between said first and second terminals, a second series combination of a first resistor, third and fourth *pn* junctions and a second resistor in that order, said third and fourth *pn* junctions being connected back-to-back in the same sense with respect to each other as are the first and second *pn* junctions, which second series combination is connected in parallel with said first series combination in such manner that the first resistor is connected to said first terminal and the second resistor is connected to said second terminal, a connection between the common point of the first and second *pn* junctions and the common point of the third and fourth *pn* junctions, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a bias current source circuit connected between said reference point and a first further point being the common point of the first resistor and the third *pn* junction and between said reference point and a second further point being the common point of the second resistor and the fourth *pn* junction in such manner that an impedance is present between said first and second further points, for setting up a potential difference across the series combination of the first resistor and the first load and across the series combination of the second resistor and the second load and for supplying forward current to said first, second, third and fourth *pn* junctions, and controllable sink for output current of said bias current source circuit, which sink is connected between said reference point and the common point of the first, second, third and fourth *pn* junctions so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value said third and fourth *pn* junctions will conduct before said first and second *pn* junctions conduct.

2. An arrangement as claimed in Claim 1, including a third series combination of a third resistor, fifth and sixth *pn* junctions and a fourth resistor in that order, said fifth and sixth *pn* junctions being connected back-to-back in the same sense with respect

conductive strips provided thereon for making the various electric connections.

When the maximum control current is carried by the terminal 31, the portion of the *p*-type region 25 in close proximity to the contact opening 32 and the portion of the *p*-type region 25 in close proximity to the contact opening 34 in conjunction with narrow intermediate portion of the *n*-type region 23 will constitute a lateral *pn*p transistor which is in the saturated condition. As is known, such a transistor constitutes only a very small alternating-current resistance (of a few ohms) between its collector and its emitter (the terminals 7 and 8).

The embodiments shown may be modified in various ways. For example, in the embodiment shown in Figure 1 the bias current source, which is connected to the ladder network of diodes and resistors through two resistors 21 and 22, may be replaced by a current source circuit comprising two effectively separate current sources, for example two large-value resistors connected to the positive supply. If this is done the alternating-current resistance between the terminals 7 and 8 in the non-controlled condition will be very high, resulting in an increased control range which however, will generally be at the expense of signal handling capability. If the arrangement of Figure 2 is modified according to this principle, Figure 6 will be obtained. In Figure 6 the region 25 is interrupted at its centre so that two identical part-regions 25a and 25b are formed, two current sources 20a and 20b being connected by terminals 9a and 9b respectively, one on each side of the interruption, to the part-regions 25a and 25b respectively.

Figures 7a and 7b show an embodiment obtained by applying the principle of interrupting the region 25 to the embodiment of Figures 5a and 5b, corresponding reference numerals being used for corresponding components in the two sets of Figures. An elongate lateral *pn*p transistor is obtained in which both ends of one main electrode region 25a and both ends of the other main electrode region 25b are provided with terminals (7, 9a and 8, 9b respectively). The terminals 7 and 8 serve for connecting to the circuit to be controlled whilst the terminals 9a and 9b serve for connection to the current sources 20a and 20b respectively.

In the arrangement of Figure 1 the semiconductor elements 10, 11, 13, 15, 17 and 19 may have their polarities reversed if the directions of the currents *I* and *I₁* are also reversed. Similarly, in Figures 2 to 7 the conductivity types of the various regions may be interchanged if the

polarities of the control current and the bias current are also reversed.

WHAT WE CLAIM IS:—

1. A symmetrical circuit arrangement for forming a variable alternating-current resistance between first and second terminals thereof, said arrangement comprising a first series combination of first and second *pn* junctions which are connected back-to-back, which first series combination is connected between said first and second terminals, a second series combination of a first resistor, third and fourth *pn* junctions and a second resistor in that order, said third and fourth *pn* junctions being connected back-to-back in the same sense with respect to each other as are the first and second *pn* junctions, which second series combination is connected in parallel with said first series combination in such manner that the first resistor is connected to said first terminal and the second resistor is connected to said second terminal, a connection between the common point of the first and second *pn* junctions and the common point of the third and fourth *pn* junctions, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a bias current source circuit connected between said reference point and a first further point being the common point of the first resistor and the third *pn* junction and between said reference point and a second further point being the common point of the second resistor and the fourth *pn* junction in such manner that an impedance is present between said first and second further points, for setting up a potential difference across the series combination of the first resistor and the first load and across the series combination of the second resistor and the second load and for supplying forward current to said first, second, third and fourth *pn* junctions, and controllable sink for output current of said bias current source circuit, which sink is connected between said reference point and the common point of the first, second, third and fourth *pn* junctions so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value said third and fourth *pn* junctions will conduct before said first and second *pn* junctions conduct.

2. An arrangement as claimed in Claim 1, including a third series combination of a third resistor, fifth and sixth *pn* junctions and a fourth resistor in that order, said fifth and sixth *pn* junctions being connected back-to-back in the same sense with respect



to each other as are the first and second *pn* junctions, which third series combination is connected between said first and second further points in such manner that the third resistor is connected to said first further point and the fourth resistor is connected to said second further point, and a connection between the common point of the fifth and sixth *pn* junctions, and the common of the first, second, third and fourth *pn* junctions, the bias current source circuit being connected between said reference point and a third further point being the common point of the third resistor and the fifth *pn* junction and between said reference point and a fourth further point being the common point of the fourth resistor and the sixth *pn* junction in such manner that an impedance is present between said third and fourth common points and so that the connection of said bias current source circuit to said first further point is *via* said third resistor and the connection of said bias current source to said second further point is *via* said fourth resistor.

3. An arrangement as claimed in Claim 1 or Claim 2, wherein the *pn* junctions are the base-emitter junctions of transistors, the collectors of said transistors being connected together and the bases of said transistors being connected to said controllable sink.

4. A symmetrical circuit arrangement for forming a variable alternating current resistance between first and second terminals thereof, said arrangement comprising an elongate *pn* junction between a first resistive region in a semiconductor chip and a second region in said chip, which second region is of opposite conductivity type to said first region, the first and second terminals being provided on said first region adjacent first and second portions of said *pn* junction respectively, a third terminal provided on said first region adjacent a third portion of said *pn* junction, which third portion lies substantially midway between said first and second portions on going along said junction, a first load connected between said first terminal and a reference point, a second load connected between said second terminal and said reference point, a bias current source connected between said reference point and said third terminal for setting up a potential difference across the series combination of the first load and that portion of the first region which lies between said first and third terminals and across the series combination of the second load and that portion of the first region which lies between the second and third terminals and for supplying forward current to said *pn* junction, and a controllable sink for output current of said

bias current source, which sink is connected between said reference point and said second region so that if in operation the current carried by said controllable sink is varied from a first given value to a second higher given value an increasing portion of said *pn* junction will become conductive and an increasing portion of the impedance presented between said first and second terminals by said first region will become shunted by a current path which extends through said second region, so reducing the impedance between said first and second terminals.

5. An arrangement as claimed in Claim 4, wherein the elongate *pn* junction is the base-emitter junction of a transistor the collector of which is constituted by a further region is said semiconductor chip, which further region is of the same conductivity type as said first region.

6. An arrangement as claimed in Claim 5, including a conductor interconnecting various locations of said further region to shunt the intrinsic resistance of said further region.

7. An arrangement as claimed in any of Claims 4 to 6, including a conductor interconnecting various locations of said second region to shunt the intrinsic resistance of said second region.

8. An arrangement as claimed in Claim 4, wherein the first region has a bent shape which is such that the distance between the two portions of said first region on which the first and second terminals are provided is appreciably shorter than the length of the first region from the first terminal to the second terminal via the third terminal.

9. An arrangement as claimed in Claim 8, wherein said distance is so small that said two portions form a transistor in conjunction with the intermediate portion of the second region.

10. A symmetrical circuit arrangement for forming a variable alternating current resistance between first and second terminals thereof, said arrangement comprising first and second elongate *pn* junctions between a first resistive region in a semiconductor chip and a second region in said chip and between a further resistive region in said chip and said second region respectively, said second region being of opposite conductivity type to said first and further regions, said first and second terminals being provided on said first and further regions respectively adjacent a first portion of said first *pn* junction and a first portion of said second *pn* junction respectively, a third terminal provided on said first region adjacent a second portion of said first *pn* junction, a fourth terminal provided on said further region adjacent a second portion of said second *pn* junction, the spacing



27 21

5 between said first and second portions of
the first *pn* junction on going along said first
pn junction being substantially equal to the
spacing between said first and second
portions of the second *pn* junction on going
along said second *pn* junction, a first load
connected between said first terminal and a
reference point, a second load connected
between said second terminal and said
reference point, a first bias current source
connected between said reference point and
said third terminal for setting up a
potential difference across the series
combination of the first load and the first
region and for supplying forward current
to said first *pn* junction, a second bias
current source connected between said
reference point and said fourth terminal for
setting up a potential difference across the
series combination of the second load and
the further region and for supplying
forward current to said second *pn* junction,
and a controllable sink for output currents
of said bias current sources, which sink is
connected between said reference point
and said second region so that if in
operation the current carried by said
controllable sink is varied from a first given
value to a second higher given value
increasing portions of said first and second
pn junctions will become conductive and an
increasing portion of the impedance
presented between said first and second
terminals by said first and further regions
will become shunted by a current path
which extends through said second region,
so reducing the impedance between said
first and second terminals.
11. An arrangement as claimed in any of
the preceding Claims, wherein the first and
second terminals are connected to the
emitters of first and second transistors
respectively, which transistors are included
one in each of the two halves of a
differential amplifier stage.
12. A symmetrical circuit arrangement
substantially as described herein with
reference to Figure 1 or Figure 2 of the
drawings, to said Figure 2 as modified by
any of Figures 3, 4 or 5 of said drawings, to
Figure 6 of said drawings, or to said Figure
6 as modified by Figure 7 of said drawings.

C. A. CLARK,
Chartered Patent Agent,
Berkshire House,
168—173 High Holborn,
London WC1V 7AQ.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1978
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.

