Alignment Mark and Method of Formation

TECHNICAL FIELD

[0001] The present disclosure relates generally to a method of semiconductor processing and a structure formed thereby and, more particularly, to a method of forming an alignment mark and the structure formed thereby.

BACKGROUND

[0002] In semiconductor processing, the formation of structures and devices generally include the sequential formation of one layer of material or composition of materials over another layer. These layers are commonly etched or doped using photolithography techniques to direct the areas where the layers are etched or doped. For example, the formation a source/drain region of a transistor may include forming a photoresist layer over the semiconductor substrate in which a source/drain region is to be formed, exposing the photoresist layer to light such that the volume of photoresist above the area where the source/drain region is to be formed is removed, and doping the semiconductor substrate using the photoresist to prevent unexposed areas from being doped. Further, a contact to the source/drain region may include depositing an insulating layer over the semiconductor substrate, forming a photoresist over the insulating layer, exposing the photoresist to light such that a volume of photoresist over the source/drain region is removed, etching the insulating layer using the photoresist as a mask, and depositing a metal.

[0003] The integrity of the devices formed using these photolithography techniques is therefore dependent upon proper alignment of features from one layer to another. In the example above, the contact must be aligned with the source/drain region. Misalignment between these layers may prevent a device from being operational.

[0004] The semiconductor processing field has developed alignment marks to allow higher precision in aligning photolithographic processes between layers. Alignment marks allow for the measurement of the placement of a wafer upon which processing has proceeded. Based on a measurement, a stepper may move or modify the position of the wafer to help enable better alignment of the photolithography processes.

SUMMARY

[0005] In accordance with an embodiment, a structure comprises a substrate having a first area and a second area; a through substrate via (TSV) in the substrate penetrating the first area of the substrate; an isolation layer over the second area of the substrate, the isolation layer having a recess; and a conductive material in the recess of the isolation layer, the isolation layer being disposed between the conductive material and the substrate in the recess.

[0006] Another embodiment is a structure having an alignment mark. The structure comprises a substrate comprising a through substrate via (TSV), the TSV extending from a front surface of the substrate to a back surface of the substrate; an isolation layer over the back surface of the substrate, the isolation layer having a cavity; and a conductor positioned in the cavity, the isolation layer being disposed between the conductor and the substrate in the cavity.

[0007] A yet further embodiment is a method for forming a stacked device. The method comprises providing a substrate having a through substrate via (TSV) protruding from a back side; forming an isolation layer over the back side of the substrate, the isolation layer having a recess; and forming a conductive layer in the recess, the isolation layer being disposed between the conductive layer and the substrate in the recess.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] Figures 1A through 1H illustrate a method for forming an alignment mark for a stacked device according to an embodiment;

[0010] Figure 2 illustrates a structure having an alignment mark formed by the method described with respect to Figures 1A through 1H;

[0011] Figures 3A through 3H illustrate another method for forming an alignment mark on a substrate for a stacked device according to another embodiment;

[0012] Figures 4A through 4F illustrate a yet further method for forming an alignment mark according to a yet further embodiment; and

[0013] Figure 5 illustrates a structure having an alignment mark formed by either of the methods described with respect to Figures 3A through 3H or Figures 4A through 4F.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0014] The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosed subject matter, and do not limit the scope of the different embodiments.

[0015] Embodiments will be described with respect to a specific context, namely an alignment mark formed during the processing of a die for a stacked device. Other embodiments may also be applied, however, to an interposer or another structure where an alignment mark is used during processing.

[0016] Figures 1A through 1H illustrate a method for forming an alignment mark for a stacked device according to an embodiment. A structure produced by the method in Figures 1A through 1H is shown in Figure 2. Any sequence described in the method is solely for clarity of description, and the steps of the method may be performed in any logical progression.

[0017] Figure 1A shows a substrate 100, such as a die of a stacked device, in an intermediate stage of processing, such as after front side processing. Particularly, at this point in processing, through substrate vias (TSVs) 102 have been formed in the substrate 100, one or more metallization layers 104 with interconnect structures 106 have been formed on the substrate 100, and conductive bumps 108 have been formed electrically coupled to the interconnect structures 106. The substrate 100 may be any suitable material, such as silicon. The TSVs 102 may comprise a liner layer, a diffusion barrier layer, an adhesion layer, an isolation layer, and/or the like, and filled with a conductive material. The liner layer may be, for example, silicon

nitride, silicon oxide, a polymer material, a combination thereof, and/or the like. The diffusion barrier layers, for example, may comprise one or more layers of TaN, Ta, TiN, Ti, CoW, or the like, and the conductive material may comprise, for example, copper, tungsten, aluminum, silver, combinations thereof, and/or the like, formed by an electro-chemical plating process. The metallization layers 104, interconnect structures 106, and conductive bumps 108 may be any acceptable material and formed with suitable processes, such as those known for back end of the line (BEOL) processing.

[0018] Further, the front side of the substrate 100 has been attached by adhesive 110 to a carrier 112 for back side processing. Generally, the carrier 112 provides temporary mechanical and structural support during subsequent processing steps. In this manner, damage to the substrate 100 may be reduced or prevented. The carrier 112 may comprise, for example, glass, silicon oxide, aluminum oxide, and the like. The adhesive 110 may be any suitable adhesive, such as an ultraviolet (UV) glue, which loses its adhesive property when exposed to UV lights. It should be noted that reference numbers 104 through 112 are not explicitly identified in Figures 1B through 1H and 2; however, the features corresponding to these reference numbers are present in these figures. The omission of these reference numbers is merely for the clarity of the depictions.

[0019] In Figure 1B, the structure of Figure 1A is shown after the substrate 100 is thinned and recessed to expose the TSVs 102 through the back side of the substrate 100. The thinning and recessing may result in the substrate 100 being a thin substrate, i.e. approximately 20 micrometers to approximately 200 micrometers in thickness. The thinning and recessing may be performed by a planarization process, an etch process, a combination thereof, and/or the like. For example, initially a planarizing process, such as a chemical mechanical polish (CMP), may

be performed to initially expose top surfaces of the TSVs 102. Thereafter, one or more etching processes having a high etch-rate selectivity between the material of the TSVs 102 and the substrate 100 may be performed, thereby leaving the TSVs 102 protruding from the back side of the substrate 100.

[0020] Figure 1C shows a photoresist layer 114 formed on the back side of the substrate 100. The photoresist layer 114 may have a thickness that is greater than the height of the protruding portions of the TSVs 102. The photoresist layer 114 has openings 116 formed therein. The openings 116 may be formed using acceptable photolithography techniques, such as using a lithography mask to expose the photoresist layer 114 to light where openings 116 are to be formed. After the formation of the openings 116, an etch process, such as an anisotropic etch, is performed to create openings 118 recessed below the surface of the back side of the substrate 100, as illustrated in Figure 1D. Figure 1E shows the structure of Figure 1D after an ash/flush process is performed to remove the photoresist layer 114.

[0021] Figure 1F illustrates the structure in Figure 1E after the formation of a first isolation layer 120 and a second isolation layer 122. The first and second isolation layers 120 and 122 may be silicon nitride, silicon oxide, silicon carbide, silicon oxynitride, an oxide, a polymer material, a combination thereof, and/or the like. The first and second isolation layers 120 and 122 may further be a single layer or may be multiple layers consisting essentially of the same or different material compositions. In the example shown in Figure 1F, the first isolation layer 120 is a silicon nitride, and the second isolation layer 122 is a silicon oxide. The first and second isolation layers 120 and 122 may be deposited using acceptable deposition techniques, such as a chemical vapor deposition (CVD) process or, further, by a CVD using a low temperature. As depicted in Figure 1F, the first isolation layer 120 and the second isolation layer 122 are both

formed on exposed top surfaces of the substrate 100 within the openings 118 and both conform to those exposed surfaces.

[0022] Figure 1G shows a photoresist layer 124 formed over the second isolation layer 122. The photoresist layer 124 may be patterned, such as by exposing the photoresist layer 124 to light, to allow an etch process to remove portions of the first and second isolation layers 120 and 122 that coat the protruding portions of the TSVs 102. The first and second isolation layers 120 and 122 are then etched, such as by a dry etch, to allow the TSVs 102 to be exposed from under the first and second isolation layers 120 and 122, as shown in Figure 1H. The etchant used for the etch process may have a high selectivity between the materials used for the TSVs 102 and the second isolation layer 122 and the first isolation layer 120. Figure 1H further shows the structure after an ash/flush process is performed to remove the photoresist layer 124.

[0023] Figure 2 illustrates a structure having an alignment mark 130 formed by the method described with respect to Figures 1A through 1H. As shown in Figure 2, the structure of Figure 1H further comprises a first metal layer 126 and a second metal layer 128. The first metal layer 126 may be titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), titanium silicon nitride (TiSiN), tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten (W), tungsten nitride (W_2N), tungsten silicon nitride (WSiN), a combination thereof, and/or the like, and the second metal layer 128 may be copper and/or the like. The first metal layer 126 and the second metal layer 128 may be formed using a suitable deposition technique, such as by a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or an atomic layer deposition (ALD) process. The first metal layer 126 and second metal layer 128 formed in the openings 118 with the second isolation layer 122 and the first isolation layer 120 disposed between the first metal layer 126 and the substrate 100 form alignment marks 130 on

the back side of the substrate 100. A person having ordinary skill in the art will readily understand that portions of the first and second metal layers 126 and 128, such as the portions between the TSVs 102, may be removed in subsequent processing steps, such as after the formation of copper pillars on the TSVs 102, to prevent short circuiting of the TSVs 102.

[0024] Figures 3A through 3H illustrate another method for forming an alignment mark on a substrate for a stacked device according to another embodiment, and Figures 4A through 4F illustrate a yet further method for forming an alignment mark according to a yet further embodiment. A structure produced by these methods is shown in Figure 5. Any sequence herein described in the method is solely for clarity of description, and the steps of the method may be performed in any logical progression.

[0025] The method as depicted in Figures 3A through 3H will be described first. Figure 3A shows a substrate 200 in an intermediate stage of processing, such as after front side processing. Particularly, at this point in processing, through substrate vias (TSVs) 202 have been formed in the substrate 200, one or more metallization layers 204 with interconnect structures 206 have been formed on the substrate 200, and conductive bumps 208 have been formed electrically coupled to the interconnect structures 206. The substrate 200 may be any suitable material, such as silicon. The TSVs 202 may comprise a liner layer, a diffusion barrier layer, adhesion layer, and/or the like, and filled with a conductive material. The liner layer may be, for example, silicon nitride, silicon oxide, a polymer material, a combination thereof, and/or the like. The diffusion barrier layers, for example, may comprise one or more layers of TaN, Ta, TiN, Ti, CoW, or the like, and the conductive material may comprise, for example, copper, tungsten, aluminum, silver, combinations thereof, and/or the like, formed by an electro-chemical plating process. The metallization layers 204, interconnect structures 206, and conductive bumps 208

may be any acceptable material and formed with suitable processes, such as those known for BEOL processing.

[0026] Further, the front side of the substrate 200 has been attached by adhesive 210 to a carrier 212 for back side processing. Generally, the carrier 212 provides temporary mechanical and structural support during subsequent processing steps. In this manner, damage to the substrate 200 may be reduced or prevented. The carrier 212 may comprise, for example, glass, silicon oxide, aluminum oxide, and the like. The adhesive 210 may be any suitable adhesive, such as an ultraviolet (UV) glue, which loses its adhesive property when exposed to UV lights. It should be noted that reference numbers 204 through 212 are not explicitly identified in Figures 3B through 3H and 5; however, the features corresponding to these reference numbers are present in these figures. The omission of these reference numbers is merely for the clarity of the depictions.

[0027] In Figure 3B, the structure of Figure 3A is shown after the substrate 200 is thinned and recessed to expose the TSVs 202 through the back side of the substrate 200. The thinning and recessing may result in the substrate 200 being a thin substrate, i.e. approximately 20 micrometers to approximately 200 micrometers in thickness. The thinning and recessing may be performed by a planarization process, an etch process, a combination thereof, and/or the like. For example, initially a planarizing process, such as a CMP, may be performed to initially expose top surfaces of the TSVs 202. Thereafter, one or more etching processes having a high etch-rate selectivity between the material of the TSVs 202 and the substrate 200 may be performed, thereby leaving the TSVs 202 protruding from the back side of the substrate 200.

[0028] Figure 3C illustrates the structure in Figure 3B after the formation of a first isolation layer 214 and a second isolation layer 216. The first isolation layer 214 is formed over the back

side of the substrate 200, and the second isolation layer 216 is formed over the first isolation layer 216. The first and second isolation layers 214 and 216 may be silicon nitride, silicon oxide, silicon carbide, silicon oxynitride, an oxide, a polymer material, a combination thereof, and/or the like. The first and second isolation layers 214 and 216 may further be a single layer or may be multiple layers consisting of the same or different material compositions. In the example shown in Figure 3C, the first isolation layer 214 is a silicon nitride, and the second isolation layer 216 is a silicon oxide. The first and second isolation layers 214 and 216 may be deposited using acceptable deposition techniques, such as a CVD process or, further, by a CVD using a low temperature.

[0029] Figure 3D shows a photoresist layer 218 formed over the second isolation layer 216. The photoresist layer 218 may be patterned, such as by exposing the photoresist layer 218 to light, to allow an etch process to remove portions of the first and second isolation layers 214 and 216 that coat the protruding portions of the TSVs 202. The first and second isolation layers 214 and 216 are then etched, such as by a dry etch, to allow the TSVs 202 to be exposed from under the first and second isolation layers 214 and 216, as shown in Figure 3E. The etchant used for the etch process may have a high selectivity between the materials used for the TSVs 202 and the second isolation layer 216 and the first isolation layer 216. Figure 3E further shows the structure after an ash/flush process is performed to remove the photoresist layer 218.

[0030] Figure 3F shows a photoresist layer 220 formed over the second isolation layer 216. The photoresist layer 220 has openings 222 formed therein. The openings 222 may be formed using acceptable photolithography techniques, such as using a lithography mask to expose the photoresist layer 220 to light where openings 222 are to be formed. After the formation of the openings 222, an etch process, such as an anisotropic etch, is performed to create openings 224

recessed in the second isolation layer 216, as shown in Figure 3G. The openings 224 may be recessed further into the first isolation layer 214, but not to or below the surface of the back side of the substrate 200. Figure 3H shows the structure of Figure 3G after an ash/flush process is performed to remove the photoresist layer 220.

[0031] The method as depicted in Figures 4A through 4F will now be described. The method proceeds in Figures 4A through 4C as previous discussed with respect to Figures 3A through 3C. Therefore, discussion of these steps is omitted for brevity. Further, like reference numbers refer to the same or similar features and/or materials in Figures 3A through 3C and Figures 4A through 4C.

[0032] Figure 4D shows a photoresist layer 230 formed over the second isolation layer 216. The photoresist layer 230 has openings 232 formed therein. The openings 232 may be formed using acceptable photolithography techniques, such as using a lithography mask to expose the photoresist layer 230 to light. The second isolation layer 216 is then etched, such as by an anisotropic etch, to create openings 234 recessed in the second isolation layer 216, as shown in Figure 4E. The etchant used for the etch process may have a high selectivity between the materials used for the second isolation layer 216 and the first isolation layer 214. Afterwards, a planarization process, such as a CMP, may be used to remove portions of the first and second isolation layer 214 and 216 over the TSVs 202 to allow the TSVs 202 to be exposed at an upper surface, as shown in Figure 4F. Figure 4F further shows the structure after an ash/flush process is performed to remove the photoresist layer 230.

[0033] Figure 5 illustrates a structure having an alignment mark 240 formed by either of the methods described with respect to Figures 3A through 3H or Figures 4A through 4F. As shown in Figure 5, the structure of Figure 3H or 4F further comprises a first metal layer 236 and a

second metal layer 238. The first metal layer 236 may be Ti, TiN, TiW, TiSiN, Ta, TaN, TaSiN, W, W_2N, WSiN, a combination thereof, and/or the like, and the second metal layer 238 may be copper and/or the like. The first metal layer 236 and the second metal layer 238 may be formed using a suitable deposition technique, such as by a PVD process, a CVD process, or an ALD process. The first metal layer 236 and second metal layer 238 formed in the openings 234 with the first isolation layer 216 disposed between the first metal layer 236 and the substrate 300 form alignment marks 240 on the back side of the substrate 200. A person having ordinary skill in the art will readily understand that portions of the first and second metal layers 236 and 238, such as the portions between the TSVs 202, may be removed in subsequent processing steps, such as after the formation of copper pillars on the TSVs 202, to prevent the shorting of the TSVs 202.

[0034] Embodiments may prevent diffusion of metal in the alignment mark. The isolation layer(s) may form a barrier layer to prevent a metal, such as copper, from diffusing into the substrate in the embodiments. By preventing diffusion, devices and structures formed in the substrate are less likely to be inoperable because of shorting or other problems that may be caused by diffusion of the metal in the alignment mark.

[0035] Also, the structures and processes of the embodiments discussed above may provide increased throughput from a process flow. Further, they may ease stress and strain in the thinned substrate because of an improved process flow, such as because of lower temperatures being used.

[0036] Although the present embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the

particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A structure comprising:

a substrate having a first area and a second area;

a through substrate via (TSV) in the substrate penetrating the first area of the substrate;

an isolation layer over the second area of the substrate, the isolation layer having a recess; and

a conductive material in the recess of the isolation layer, the isolation layer being disposed between the conductive material and the substrate in the recess.

2. The structure of claim 1, wherein the recess extends into substrate.

3. The structure of claim 1, wherein the recess does not extend into the substrate.

4. The structure of claim 1, wherein the isolation layer comprises a first sublayer and a second sublayer over the first sublayer, the first sublayer having a different composition from the second sublayer.

5. The structure of claim 4, wherein the recess extends only through the second sublayer.

6. The structure of claim 4, wherein the first sublayer comprises silicon nitride.

7. The structure of claim 1, wherein the TSV extends to protrude from the substrate.

8. A structure having an alignment mark, the structure comprising:

a substrate comprising a through substrate via (TSV), the TSV extending from a front surface of the substrate to a back surface of the substrate;

an isolation layer over the back surface of the substrate, the isolation layer having a cavity; and

a conductor positioned in the cavity, the isolation layer being disposed between the conductor and the substrate in the cavity.

9. The structure of claim 8, wherein the isolation layer comprises a first sublayer and a second sublayer over the first sublayer, the cavity being an opening in the second sublayer, and the first sublayer being disposed between the conductor and the substrate.

10. The structure of claim 8, wherein the cavity comprises a recess in the back surface of the substrate extending into the substrate, the isolation layer conforming to the recess.

11. The structure of claim 8, wherein a surface of the TSV is exposed through the isolation layer.

12. The structure of claim 8, wherein the isolation layer comprises at least one of silicon nitride, silicon carbide, silicon oxynitride, an oxide, a polymer material, and a combination thereof.

13. The structure of claim 8, wherein the conductor comprises at least one of copper, titanium, titanium nitride, titanium tungsten, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, and a combination thereof.

14. A method for forming a stacked device, the method comprising:

providing a substrate having a through substrate via (TSV) protruding from a back side;

forming an isolation layer over the back side of the substrate, the isolation layer having a recess; and

forming a conductive layer in the recess, the isolation layer being disposed between the conductive layer and the substrate in the recess.

15. The method of claim 14, wherein the forming the isolation layer comprises forming an opening in the back side of the substrate, and forming the isolation layer conforming to the opening to form the recess.

16. The method of claim 14, wherein the forming the isolation layer comprises forming an opening in the isolation layer to form the recess, the opening not reaching the back side of the substrate.

17. The method of claim 14 further comprising removing a portion of the isolation layer from a surface of the TSV to expose the surface of the TSV.

18. The method of claim 14, wherein the forming the isolation layer comprises forming a first sublayer and a second sublayer over the first, the first sublayer and the second sublayer having different materials.

19. The method of claim 14, wherein the isolation layer comprises at least one of silicon nitride, silicon carbide, silicon oxynitride, an oxide, a polymer material, and a combination thereof.

20. The method of claim 14, wherein the forming the conductive layer comprises forming a layer of titanium and forming a layer of copper over the layer of titanium.