SEMICONDUCTOR DEVICE WITH DECOUPLING CAPACITANCE AND METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Technical Field

The invention relates generally to semiconductor devices, and more specifically, to decoupling capacitance schemes in semiconductor devices.

2. Background Art

Silicon-on-insulator (SOI) CMOS technologies offer higher performance than conventional bulk-substrate CMOS technologies due to factors such as lower junction capacitances. In SOI technology, lower junction capacitances are obtained by isolating the active circuits from the bulk substrate dielectrically.

However, there are several disadvantages in SOI technology compared to bulk-substrate technology. In bulk-substrate technology, there is generally a high chip decoupling capacitance from the power supply Vdd to ground due mainly to N-well to P substrate junction capacitance. High chip decoupling capacitance provides electrostatic discharge (ESD) protection and protection from high switching noises on the chip. Unfortunately, the ESD protection level for input/output (I/O) devices on SOI is degraded due to higher diode resistances, poor thermal conduction and very low on-chip decoupling capacitance from the power supply VDD to ground. Furthermore, there are high chip and

REPLACED SHEETS SC
Description : paged ..... to paged .....
Claim(s) : paged ..... to paged .....
Drawing(s) : paged ..... to paged .....
Abstract : paged ..... to paged .....
DATE OF RECEIPT .....

I/O switching noises because of the low on-chip decoupling capacitance. Unless thin-oxide capacitors are used, which consume real estate, a chip in SOI technology has very little decoupling capacitance for noise suppression.

A common method of making SOI devices is to implant oxygen atoms into bulk-substrate devices to form a buried oxide layer. This method is known as SIMOX (separation by implanted oxygen). Several approaches to improve the ESD protection level in SOI technology have been proposed for SIMOX. One of them discloses etching off the oxide layer so that the I/O transistors can be built on bulk substrate. This approach, although demonstrating ESD improvement, requires precise and expensive processing and processing controls (*e.g.*, etching and forming circuits over different wafer topographies). Another approach employs a block mask during oxygen implant to keep the ESD circuitry area in the bulk substrate. For this approach, modified SIMOX wafers can be obtained that would offer both high-performance circuits (SOI) and acceptable ESD protection (bulk substrate). Unfortunately, this approach is deficient without a big on-chip decoupling capacitor for noise suppression and proper ESD operation.

SUMMARY OF THE INVENTION

It is thus an advantage of the present invention to provide a decoupling capacitance for a semiconductor device and the method for making the same that eliminates the above described defects.

The advantages of the invention are realized by a semiconductor device comprising a first circuit region having a first device layer over an isolation layer and a second circuit region adjacent the first circuit region having a second device layer over a well. An implant layer is implanted beneath the isolation layer in the first circuit region, which will connect to the well of the second circuit region, forming a high junction capacitance, and thus an acceptable decoupling capacitance for the semiconductor device.

The foregoing and other advantages and features of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred exemplary embodiments of the present invention will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:

FIG. 1 is a simplified diagram of a semiconductor structure in accordance with a preferred embodiment of the present invention;

FIG. 2 is an exemplary device used with the structure of FIG. 1; and

FIGS. 3, 4, 5 and 6 are cross-sectional views showing a fabrication sequence of FIG. 1 in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring to FIG. 1, there is shown, in highly simplified form, a semiconductor structure for an integrated circuit 10 in accordance with the present invention. In this example, a first circuit region of a silicon-on-insulator (SOI) structure comprises isolation oxide layer 22, first device layer 24, isolation layers 20, and a high-dose implant layer 25 of a first polarity type implanted under isolation oxide layer 22 in accordance with an embodiment of the present invention. The second circuit region (*e.g.*, a bulk device region), which is adjacent the first circuit region, comprises bulk area 30, wells 32 and 34 of a first polarity type, second device regions comprising regions 36, 38, 42, and 44 of first and second polarity types, and isolation layers 20. Both circuit regions are located in a substrate 50 of the second polarity type, the first circuit region covering most of the chip. Although only one second circuit region is shown, it will be appreciated that a plurality of such regions may be employed on a single semiconductor substrate, each delineating a subsequent active area of a device. An optional dopant 40 of the second polarity type under the implant layer 25, such as a 1MV energy implant routinely used in non-epi technology, may also be used if more capacitance is desired, or the substrate water itself may be a P+ water with a P- epitaxial layer on top.

Referring to FIG. 2, an I/O ESD device 110 is disclosed as an exemplary device that may be integrated into the present invention. Although a P-type substrate 150 with the corresponding polarity type regions is shown in FIG. 2, an N-type substrate, or an N-type substrate with a P-region created by doping, etc. with corresponding regions and modifications to the integrated circuit 110 may also be used. The I/O ESD device 110 is formed from the semiconductor substrate with I/O pad 60 connecting to P+ region 138 and N+ region 144; with N+ region 136 connecting to Vdd to form a first diode; and with P+

region 142 connecting to ground to form a second diode. An I/O ESD device, or similar device, may also be formed from an N-type substrate, with appropriate connections and modifications for proper performance. As aforementioned, an optional P-type dopant 140 under the N-type implant layer (or N-type dopant under the P-type implant layer in the case of a N-type substrate) may also be used if more capacitance is desired.

As can be seen in FIG. 2, a high junction capacitance is then formed from Vdd to ground. Vdd is coupled to the N-type implant layer 125 via N-well 132, which is coupled to N+ region 136. The P-type bulk area 130 is connected to ground via P+ region 142. A P-type dopant 140 may also be used for added capacitance. Yet another option is to use a degenerately doped (P+ , in this example) water with a lightly doped epitaxial layer (P-, in this example) +, provide both high capacitance and low resistance. As will be shown in subsequent figures, one advantage of the present invention is that high junction capacitance from Vdd to ground may be added without using any extra masks than those typically used in a SIMOX process.

Referring now to FIGS. 3-6, fabrication of a preferred embodiment of the present invention will be discussed. As seen in FIG. 3, a non-critical mask 70 is used to define the second circuit regions (bulk area regions) of a substrate 50 of a second polarity type as described in FIG. 1. An oxygen and a dopant implant 75 of a first polarity type is then applied substantially simultaneously to substrate 50 to form an isolation oxide layer 22 and an implant layer 25 of the first polarity type buried under isolation oxide layer 22, as seen in FIG. 4. Since the isolation oxide layer 22 anneal temperature is rather high (approximately 1200-1300 degrees Celsius), the implant layer 25 will out-diffuse (*i.e.*, diffuses beyond the implantation boundaries) as illustrated in FIG. 5. Thus, as shown in FIG. 6, after subsequent, standard formation of the SOI and bulk area regions, the implant

layer 25 will connect to the wells 32 and 34 of the first polarity type in the bulk area region.

Thus, this invention provides a decoupling capacitance from Vdd to ground by implanting an implant layer under the isolation oxide. Furthermore, the implant may be done at the same time as the isolation oxide formation without the need of an extra mask. A second implant (such as a P+ or N+ dopant) may also be used for added capacitance.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first circuit region having a first device layer over an isolation layer;

a second circuit region adjacent the first circuit region having a second device layer over a well of a first polarity type; and

an implant layer of the first polarity type implanted beneath the isolation layer and connected to the well.

2. The apparatus of claim 1, wherein said well is an N-well, and said implant layer is an N-type implant layer.

3. The apparatus of claim 1, wherein said well is a P-well, and said implant layer is a P-type implant layer.

4. The apparatus of claim 2, further comprising:

a P-type implant layer implanted beneath said N-type implant layer.

5. The apparatus of claim 3, further comprising:

an N-type implant layer implanted beneath said P-type implant layer.



This Sheet Has Been Replaced



6. A method of developing decoupling capacitance in a semiconductor device having a substrate comprising the steps of:

a) defining a first circuit region and a second circuit region on the substrate with a mask;

b) implanting an isolation layer in the first circuit region;

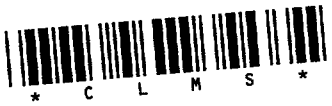
c) implanting an implant layer under the isolation layer in the first circuit region; and

d) forming a well in the second circuit region, wherein said implant layer is electrically coupled to said well.

7. The method of claim 6, wherein steps b) and c) are done substantially simultaneously.

8. The method of claim 6, wherein said well is an N-well, and said implant layer is an N-type implant layer.

9. The method of claim 6, wherein said well is a P-well, and said implant layer is a P-type implant layer.



This Sheet Has Been Replaced



10. The method of claim 6, further comprising the steps of:

e) forming a first device layer over an isolation layer in the first circuit region; and

f) forming a second device layer over the well in the second circuit region.

11. The method of claim 6, further comprising between step c) and step d) the step of: heating the first circuit region for annealing the isolation layer, wherein the implant layer diffuses out from the implantation.

12. The method of claim 6, wherein the implant layer is connected to the well.

13. The method of claim 6 further comprising the step of:

e) implanting a second implant layer beneath said implant layer in the first circuit region.



This Sheet Has Been Replaced



14. A semiconductor device comprising:

a substrate;

a first circuit region in the substrate having an isolation layer beneath a first device formed in the substrate and an implant layer beneath the isolation layer; and

a second circuit region in the substrate adjacent the first circuit region and having a well with a second device formed therein,

wherein the implant layer is electrically coupled to the well.

15. The device of claim 14, wherein said well is an N-well, and said implant layer is an N-type implant layer.

16. The device of claim 14, wherein said well is a P-well, and said implant layer is a P-type implant layer.

17. The device of claim 15, further comprising:

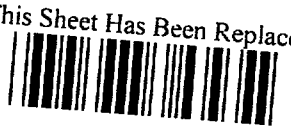
a P-type implant layer implanted beneath said N-type implant layer.

18. The apparatus of claim 16, further comprising:

an N-type implant layer implanted beneath said P-type implant layer.



This Sheet Has Been Replaced



19. In an apparatus having a bulk device region adjacent an SOI device region, the improvement comprising:

an implant layer beneath a isolation layer in the SOI device region connected to a well beneath the bulk device region.

20. The apparatus of claim 19, wherein said well is an N-well, and said implant layer is an N-type implant layer.

21. The device of claim 19, wherein said well is a P-well, and said implant layer is a P-type implant layer.



This Sheet Has Been Replaced

