ABSTRACT

A method of forming shallow trench isolations is described. A plurality of isolation trenches are etched through a first etch stop layer into the underlying semiconductor substrate. An oxide layer is deposited over the first etch stop layer and within the isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) wherein after the oxide layer fills the isolation trenches, the deposition component is discontinued while continuing the sputtering component until corners of the first etch stop layer are exposed at edges of the isolation trenches whereby the oxide layer within the isolation trenches is disconnected from the oxide layer overlying the first etch stop layer. Thereafter, a second etch stop layer is deposited overlying the oxide layer within the isolation trenches, the oxide layer overlying the first etch stop layer, and the exposed first etch stop layer corners. The second etch stop layer is polished away until the oxide layer overlying the first etch stop layer is exposed. The exposed oxide layer overlying the first etch stop layer is removed. The first and second etch stop layers are removed to complete the planarized shallow trench isolation regions in the manufacture of an integrated circuit device.

FIGURE 5