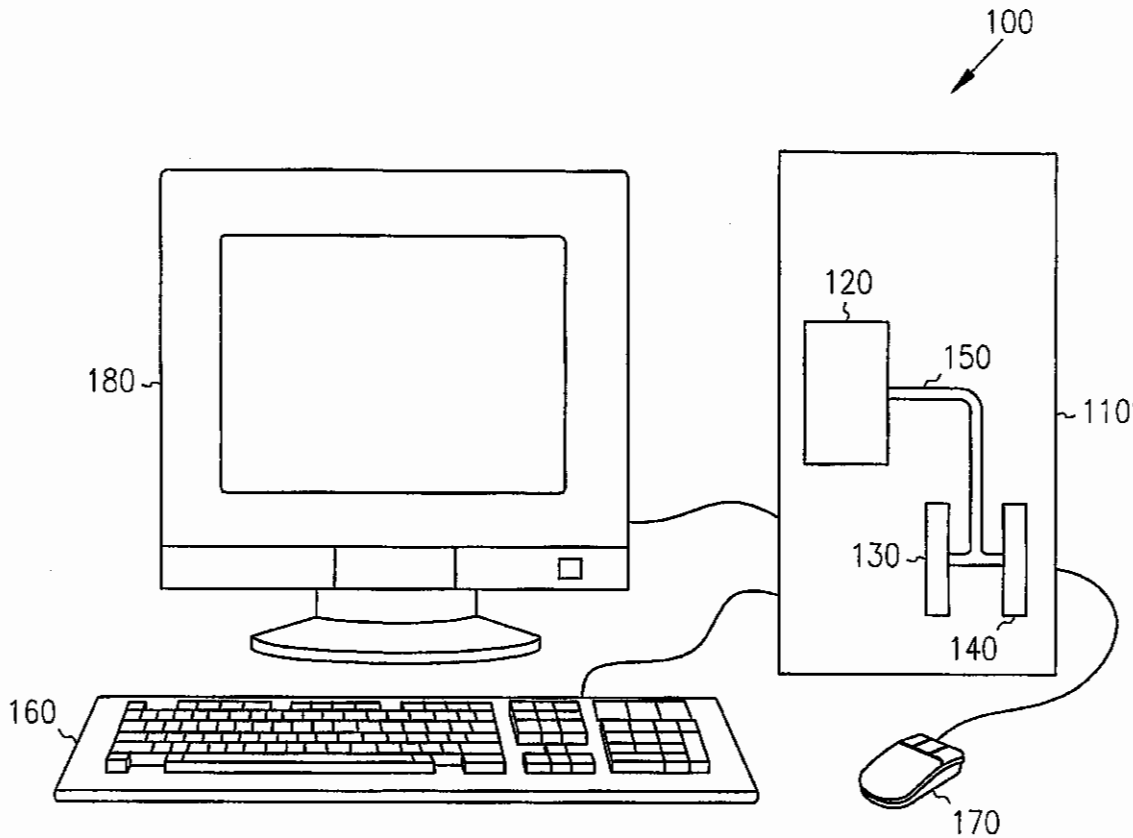


FIG. 1

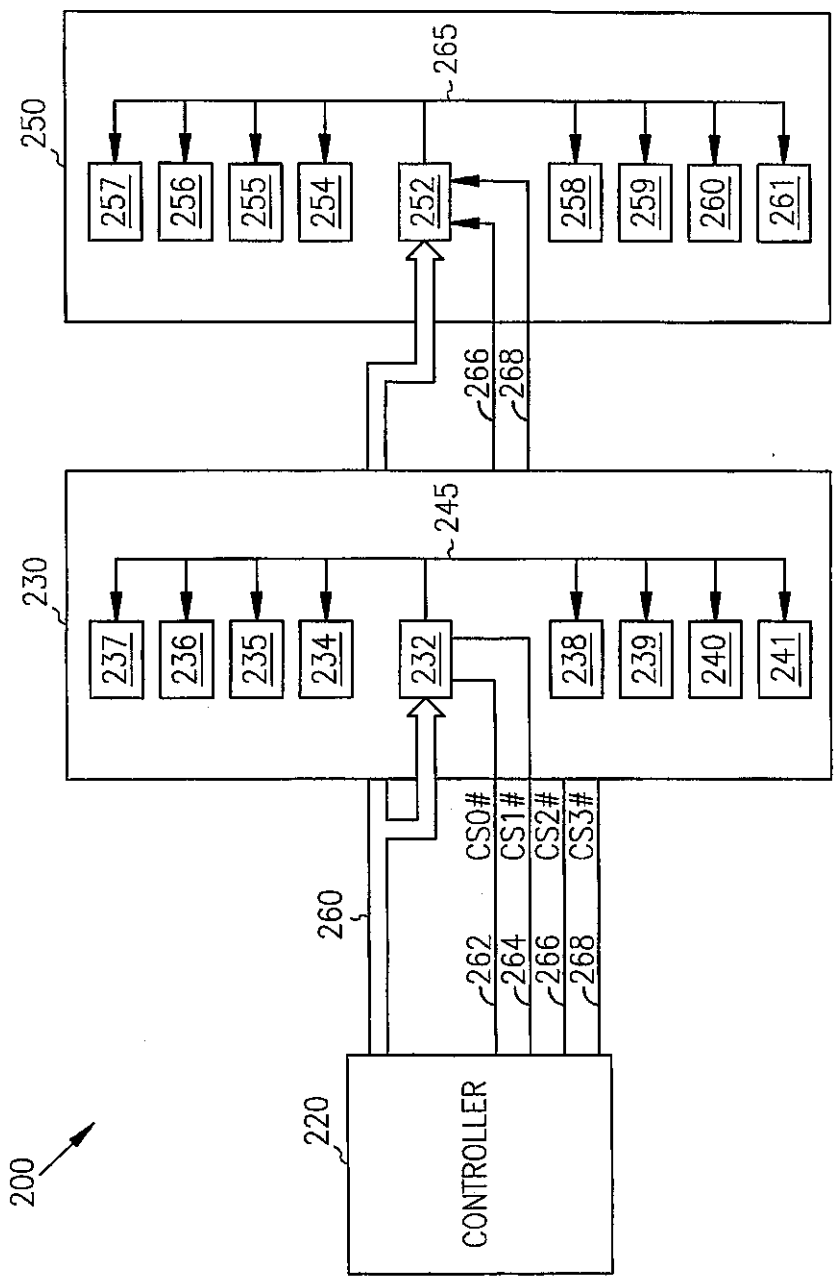

200
220
CONTROLLER
260
262
264
266
268
CS0#
CS1#
CS2#
CS3#
230
245
237
236
235
234
232
238
239
240
241
250
265
257
256
255
254
252
258
259
260
261
266
268

FIG. 2

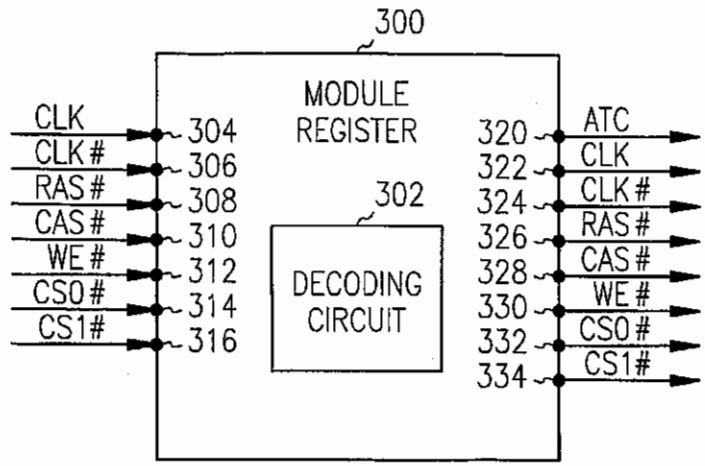

300
MODULE REGISTER
302
DECODING CIRCUIT
CLK
CLK#
RAS#
CAS#
WE#
CS0#
CS1#
304
306
308
310
312
314
316
320
322
324
326
328
330
332
334
ATC
CLK
CLK#
RAS#
CAS#
WE#
CS0#
CS1#

FIG. 3

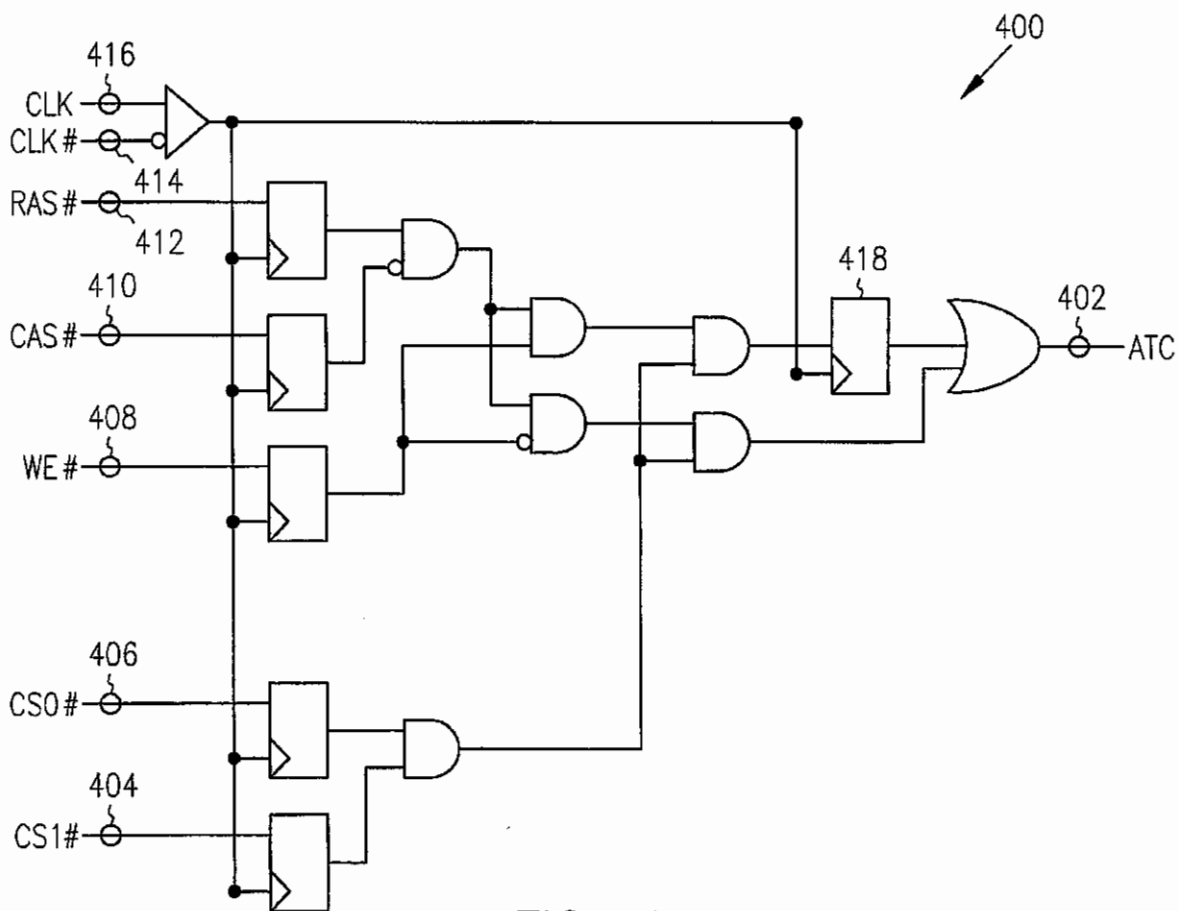

400
416
CLK
CLK#
414
RAS#
412
410
CAS#
408
WE#
406
CS0#
404
CS1#
418
402
ATC

FIG. 4

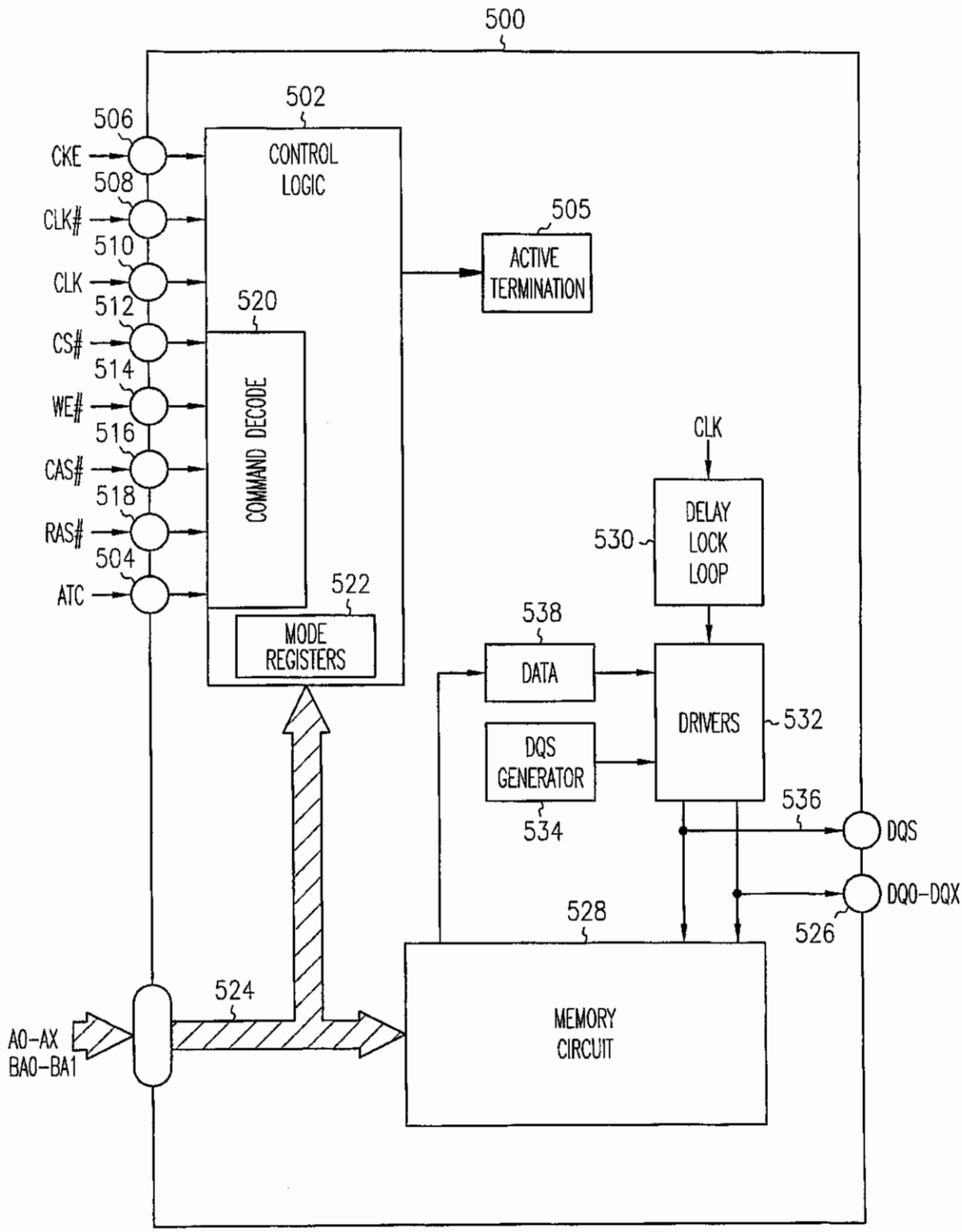

500
502
506
CKE
508
CLK#
510
CLK
512
CS#
514
WE#
516
CAS#
518
RAS#
504
ATC
CONTROL LOGIC
505
ACTIVE TERMINATION
520
COMMAND DECODE
522
MODE REGISTERS
CLK
530
DELAY LOCK LOOP
538
DATA
DQS GENERATOR
534
DRIVERS
532
536
DQS
DQ0-DQX
526
528
524
A0-AX
BA0-BA1
MEMORY CIRCUIT

FIG. 5

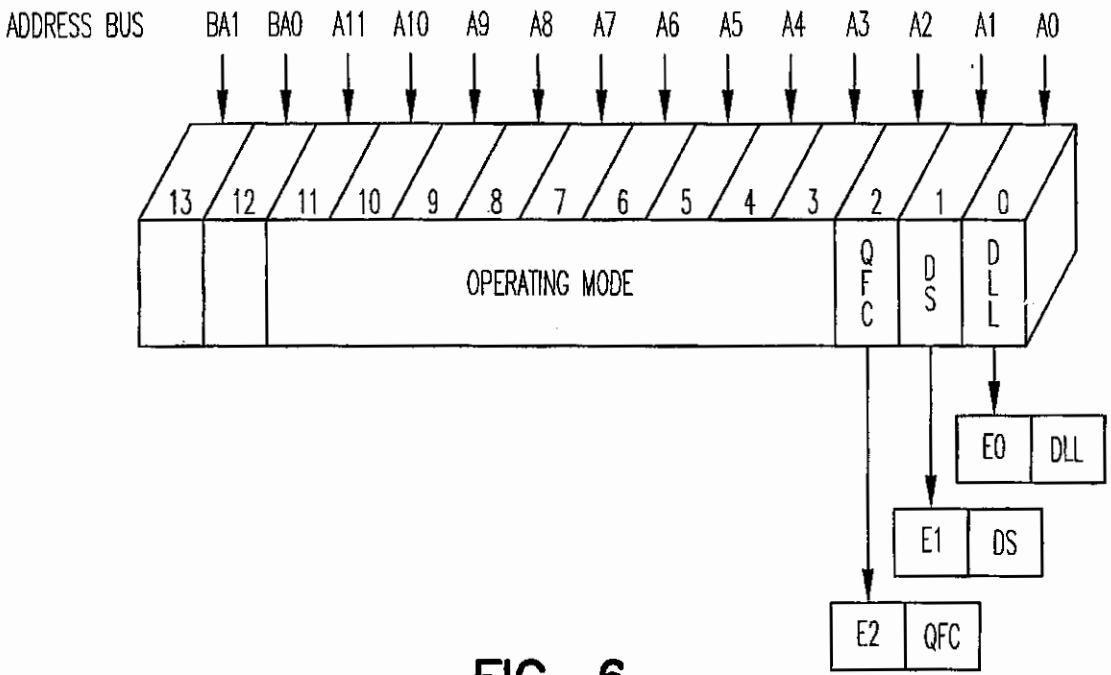

ADDRESS BUS
BA1
BA0
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OPERATING MODE
QFC
DS
DLL
E0
DLL
E1
DS
E2
QFC

FIG. 6

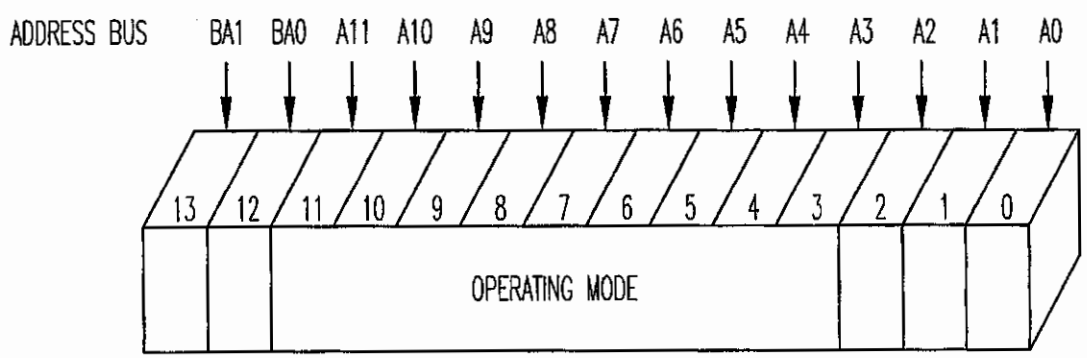

ADDRESS BUS
BA1
BA0
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OPERATING MODE

FIG. 7

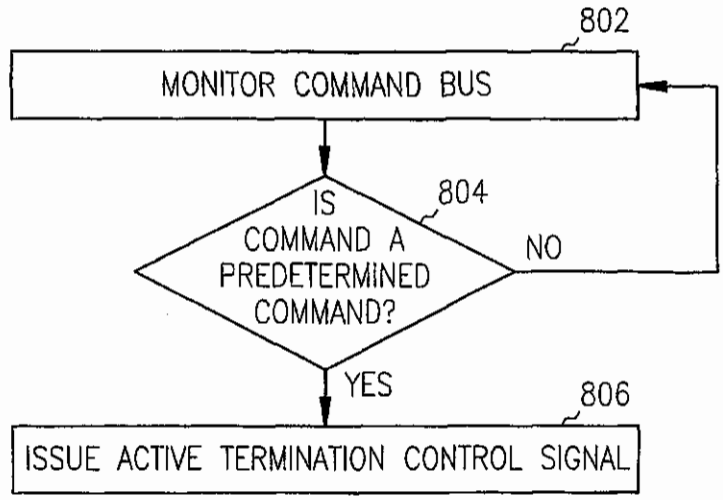


FIG. 8

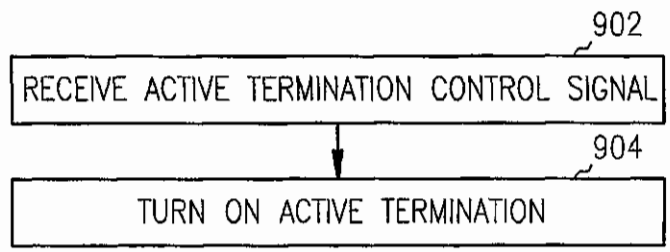


FIG. 9

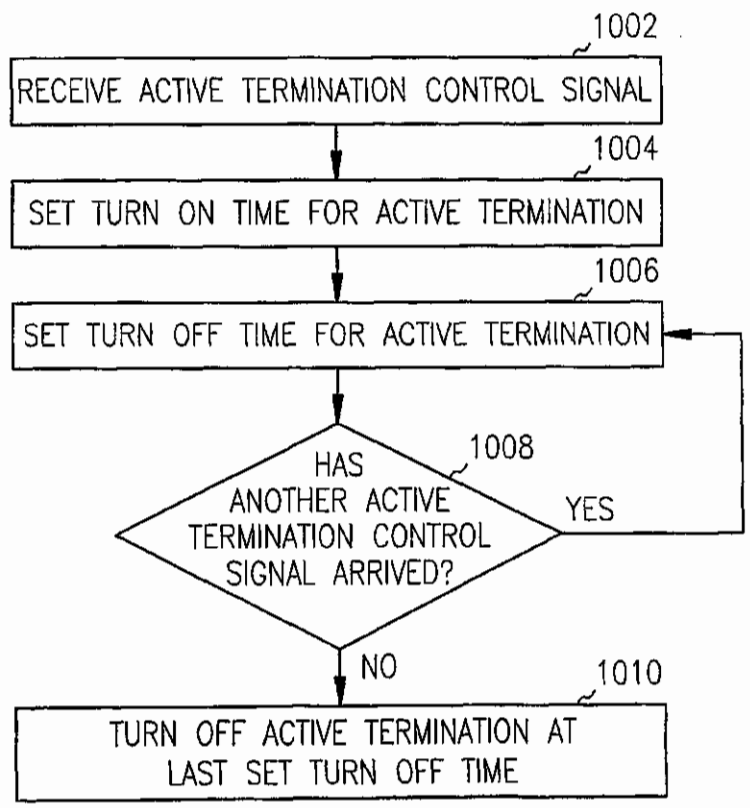


FIG. 10

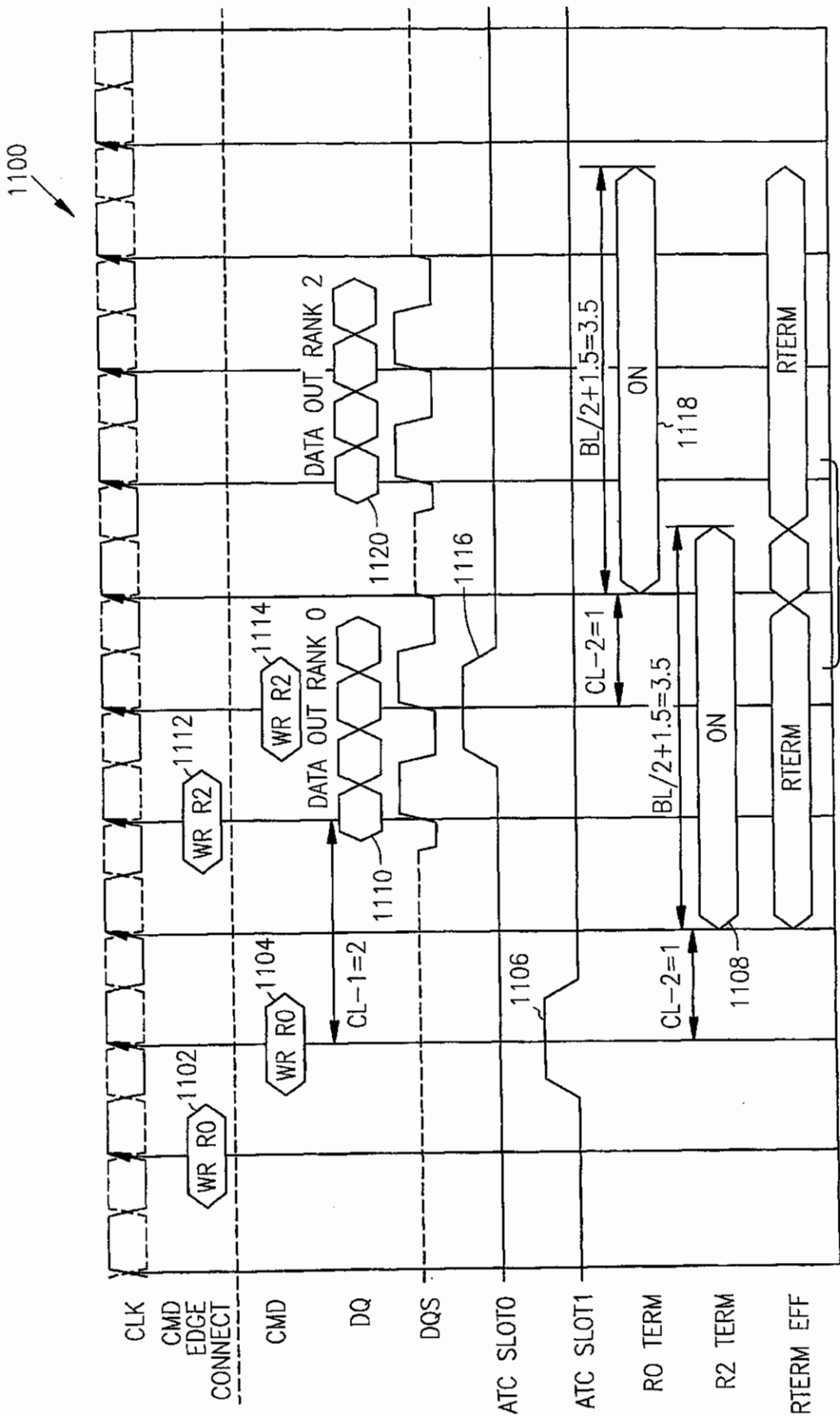

1100
CLK
CMD EDGE CONNECT
CMD
DQ
DQS
ATC SLOT0
ATC SLOT1
R0 TERM
R2 TERM
RTERM EFF
WR R0
WR R2
1102
1104
1106
1108
1110
1112
1114
1116
1118
1120
1122
DATA OUT RANK 0
DATA OUT RANK 2
CL-1=2
CL-2=1
BL/2+1.5=3.5
ON
RTERM

FIG. 11

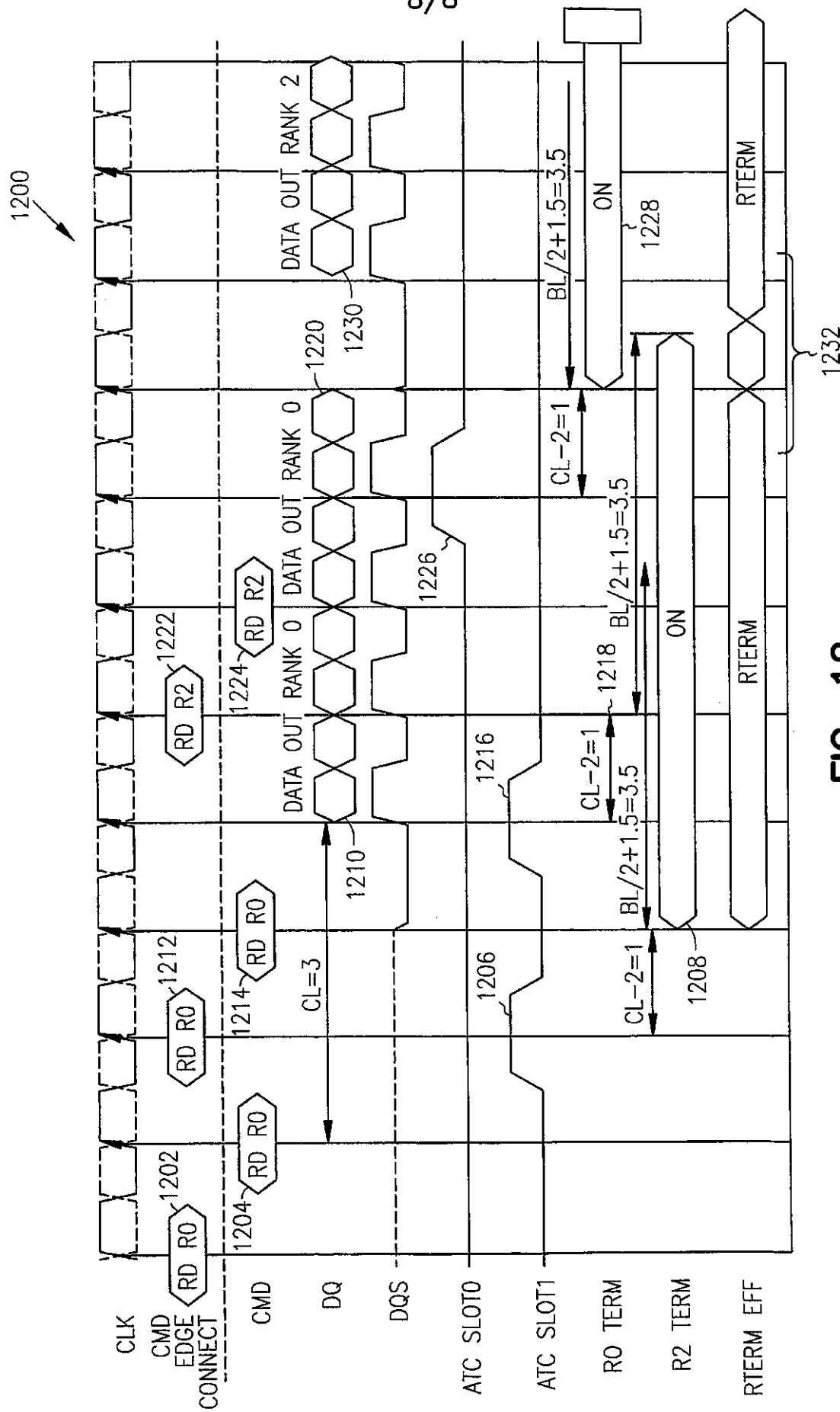

1200
CLK
CMD EDGE CONNECT
CMD
DQ
DQS
ATC SLOT0
ATC SLOT1
R0 TERM
R2 TERM
RTERM EFF
RD R0
RD R2
1202
1204
1212
1214
1222
1224
CL=3
1210
1216
1206
1226
DATA OUT RANK 0
DATA OUT RANK 2
1220
1230
CL-2=1
BL/2+1.5=3.5
1218
ON
1228
1208
RTERM
1232

FIG. 12