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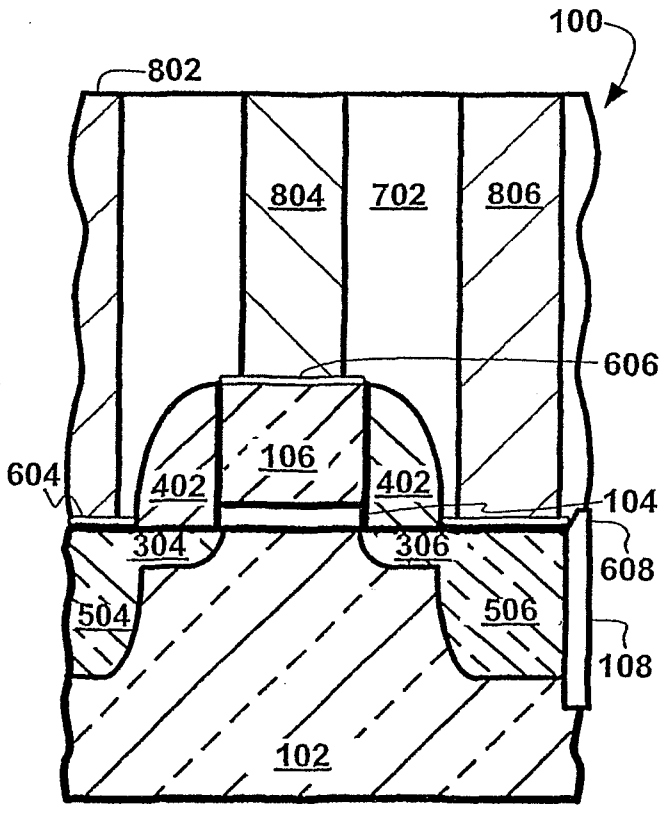
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(54) Title: LOW STRESS SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY



(57) Abstract: A method (900) of forming an integrated circuit with a semiconductor substrate (102) is provided. A gate dielectric (104) is formed on the semiconductor substrate (102), and a gate (106) is formed on the gate dielectric (104). Source/drain junctions (304) (306) are formed in the semiconductor substrate (102). A sidewall spacer (402) is formed around the gate (106) using a low power plasma enhanced chemical vapor deposition process A silicide (604) (606) (608) is formed on the source/drain junctions (304) (306) and on the gate (106), and an interlayer dielectric (702) is deposited above the semiconductor substrate (102). Contacts (802) (804) (806) are then formed in the interlayer dielectric (702) to the silicide (604) (606) (608).

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