CLAIMS

1. A manufacturing method of a semiconductor structure, comprising:

providing a substrate;

forming an ion implantation area in the substrate, an upper surface of the ion implantation area having a distance from an upper surface of the substrate;

forming an initial word line trench in the substrate, the initial word line trench extending from the upper surface of the substrate into the ion implantation area; and

widening the initial word line trench to form a word line trench, a width of a bottom of the word line trench being greater than a minimum width of the word line trench;

wherein, after the word line trench is formed, the manufacturing method of a semiconductor structure further comprises:

performing ion implantation of a first conductive type in the substrate to eliminate the ion implantation area and form a first doped area, a bottom of the first doped area being lower than the bottom of the word line trench, and a top of the first doped area being higher than the bottom of the word line trench;

performing ion implantation of a second conductive type in the substrate to form a second doped area, the second doped area being located above the first doped area and extending to the upper surface of the substrate, the word line trench penetrating the second doped area and extending into the first doped area, the first doped area being a doped area of the first conductive type, and the second doped area being a doped area of the second conductive type;

forming a gate oxide layer on a sidewall and the bottom of the word line trench;

forming a word line conductive layer on a surface of the gate oxide layer, a top of the word line conductive layer being lower than a top of the word line trench; and

forming a filling dielectric layer in the word line trench, the filling dielectric layer being located on the top of the word line conductive layer and at least filling up the word line trench.

2. The manufacturing method of a semiconductor structure according to claim 1, wherein, fluorine ions or boron ions are implanted into the substrate to form the ion implantation area.

3. The manufacturing method of a semiconductor structure according to claim 2, wherein, an ion concentration of the ion implantation area is 1×10^{17} per cm^3 to 1×10^{22} per cm^3; and

the distance between the upper surface of the ion implantation area and the upper surface of the substrate is 100 nm to 200 nm.

4. The manufacturing method of a semiconductor structure according to claim 1, wherein, widening the initial word line trench to form the word line trench comprises:

forming a sacrificial dielectric layer on a sidewall and a bottom of the initial word line trench by an in-situ growth process, a thickness of the sacrificial dielectric layer located in the ion implantation area being greater than a thickness of the remaining sacrificial dielectric layer; and

removing the sacrificial dielectric layer to form the word line trench.

5. The manufacturing method of a semiconductor structure according to claim 1, wherein, the first conductive type is P-type; and the second conductive type is N-type.

6. The manufacturing method of a semiconductor structure according to claim 1, wherein, an ion concentration in the first doped area is 1×10^{16} per cm^3 to 1×10^{20} per cm^3; and an ion concentration in the second doped area is 1×10^{16} per cm^3 to 1×10^{20} per cm^3.

7. A manufacturing method of a semiconductor structure, comprising:

providing a substrate;

forming an ion implantation area in the substrate, an upper surface of the ion implantation area having a distance from an upper surface of the substrate;

forming an initial word line trench in the substrate, the initial word line trench extending from the upper surface of the substrate into the ion implantation area; and

widening the initial word line trench to form a word line trench, a width of a bottom of the word line trench being greater than a minimum width of the word line trench;

wherein, the ion implantation area is a first doped area; and

before the ion implantation area is formed in the substrate, the manufacturing method of a semiconductor structure further comprises:

forming a second doped area in the substrate, the second doped area being located above the first doped area and extending to the upper surface of the substrate, the initial word line trench penetrating the second doped area and extending into the first doped area, the first doped area being a doped area of a first conductive type, and the second doped area being a doped area of a second conductive type.

8. The manufacturing method of a semiconductor structure according to claim 7, wherein, widening the initial word line trench to form the word line trench comprises:

wet etching the initial word line trench with a wet etching solution to obtain the word line trench, an etching rate of the wet etching solution to a part of the initial word line trench in the first doped area being greater than an etching rate of the wet etching solution to a part of the initial word line trench in the second doped area.

9. The manufacturing method of a semiconductor structure according to claim 8, wherein, the first conductive type is P-type, the second conductive type is N-type, and the wet etch solution comprises a mixture of ammonia water and hydrogen peroxide.

10. The manufacturing method of a semiconductor structure according to claim 7, wherein, an ion concentration in the first doped area is 1×10^{16} per cm^3 to 1×10^{20} per cm^3, and an ion

concentration in the second doped area is 1×10^{16} per cm^3 to 1×10^{20} per cm^3; and

the distance between the upper surface of the first doped area and the upper surface of the substrate is 100 nm to 200 nm.

11. The manufacturing method of a semiconductor structure according to any one of claims 7 to 10, wherein, after the word line trench is formed, the manufacturing method of a semiconductor structure further comprises:

forming a gate oxide layer on a sidewall and the bottom of the word line trench;

forming a word line conductive layer on a surface of the gate oxide layer, a top of the word line conductive layer being lower than a top of the word line trench; and

forming a filling dielectric layer in the word line trench, the filling dielectric layer being located on the top of the word line conductive layer and at least filling up the word line trench.