CLAIMS

What is claimed is:

1. A memory cell, comprising:

a substrate;

at least one first electrode disposed above the substrate;

at least one second electrode disposed above the at least one first electrode;

a moveable electrode disposed between the at least one first electrode and the at least one second electrode;

wherein the moveable electrode is configured to move between the at least one first electrode and the at least one second electrode;

wherein the moveable electrode comprises metal.

2. The memory cell of claim 1,

wherein the moveable electrode is configured to move from the at least one first electrode to the at least one second electrode when a voltage applied to the at least one second electrode is larger than a voltage applied to the at least one first electrode.

3. The memory cell of claim 2,

wherein the voltage applied to the at least one second electrode causes a first electrostatic force in a direction towards the at least one second electrode to be applied to the moveable electrode.

4. The memory cell of claim 2 or 3,

wherein the voltage applied to the at least one first electrode causes a second electrostatic force in a direction towards the at least one first electrode to be applied to the moveable electrode.

5. The memory cell of claim 4,

wherein the first electrostatic force is larger than the second electrostatic force and an adhesion force between the moveable electrode and the at least one first electrode.

6. The memory cell of any one of claims 2 to 5,

wherein the moveable electrode is configured to contact the at least one second electrode when no voltage is applied to the at least one first electrode and the at least one second electrode.

7. The memory cell of claim 1,

wherein the moveable electrode is configured to move from the at least one second electrode to the at least one first electrode when a voltage applied to the at least one first electrode is larger than a voltage applied to the at least one second electrode.

8. The memory cell of claim 7,

wherein the voltage applied to the at least one first electrode causes a first electrostatic force in a direction towards the at least one first electrode to be applied to the moveable electrode.

9. The memory cell of claim 7 or 8,

wherein the voltage applied to the at least one second electrode causes a second electrostatic force in a direction towards the at least one second electrode to be applied to the moveable electrode.

10. The memory cell of claim 9,

wherein the first electrostatic force is larger than the second electrostatic force and an adhesion force between the moveable electrode and the at least one second electrode.

11. The memory cell of any one of claims 7 to 10,

wherein the moveable electrode is configured to contact the at least one first electrode when no voltage is applied to the at least one first electrode and the at least one second electrode.

12. The memory cell of any one of claims 1 to 11,

further comprising an insulator layer disposed between the at least one first electrode and the at least one second electrode.

13. The memory cell of claim 12,

wherein the insulator layer, the at least one first electrode and the at least one second electrode define a cavity for guiding the movement of the moveable electrode between the at least one first electrode and the at least one second electrode.

14. The memory cell of claim 12 or 13,

further comprising a further insulator layer disposed between the substrate and the at least one first electrode.

15. The memory cell of any one of claims 1 to 14,

wherein the at least one first electrode comprises a gate electrode, and wherein the at least one second electrode comprises a drain electrode and a source electrode.

16. The memory cell of claim 15,

further comprising a further gate electrode disposed above the drain electrode and the source electrode.

17. The memory cell of any one of claims 1 to 14,

wherein the at least one first electrode comprises a drain electrode and a source electrode, and wherein the at least one second electrode comprises a gate electrode.

18. The memory cell of any one of claims 1 to 14,

wherein the at least one first electrode comprises a gate electrode, a drain electrode and a source electrode, and wherein the at least one second electrode comprises a drain electrode and a source electrode.

19. A method of manufacturing a memory cell, the method comprising:

providing a first metal layer and patterning the first metal layer to form at least one first electrode;

depositing a first sacrificial layer above the first metal layer;

depositing a second metal layer above the first sacrificial layer;

depositing a second sacrificial layer above the second metal layer;

depositing a third metal layer above the second sacrificial layer;

depositing a first sacrificial pillar structure at one side of the first sacrificial layer, the second metal layer, the second sacrificial layer and the third metal layer, and a second sacrificial pillar structure at the other side of the first sacrificial layer, the second metal layer, the second sacrificial layer and the third metal layer;

depositing a first insulator layer above the third metal layer, the first sacrificial pillar structure, the second sacrificial pillar structure and the first metal layer;

etching an opening in the first insulator layer to expose a portion of the third metal layer;

depositing a fourth metal layer above the first insulator layer and the exposed portion of the third metal layer;

etching an opening in the fourth metal layer and the third metal layer to form at least one second electrode;

removing the first sacrificial layer, the second sacrificial layer, the first sacrificial pillar structure and the second sacrificial pillar structure to form a moveable electrode and to provide a cavity for guiding movement of the moveable electrode between the at least one first electrode and the at least one second electrode.

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20. The method of claim 19,

wherein the first metal layer is deposited above a second insulator layer,

wherein the second insulator layer is deposited above a substrate.

CLAIMS

What is claimed is:

1. A memory cell, comprising:

a substrate;

at least one first electrode disposed above the substrate;

at least one second electrode disposed above the at least one first electrode; and

a moveable electrode disposed between the at least one first electrode and the at least one second electrode;

wherein the moveable electrode is configured to move between the at least one first electrode and the at least one second electrode;

wherein the moveable electrode comprises metal;

wherein the at least one first electrode comprises a gate electrode, and wherein the at least one second electrode comprises a drain electrode and a source electrode.

2. The memory cell of claim 1, wherein the moveable electrode is configured to move from the at least one first electrode to the at least one second electrode when a voltage applied to the at least one second electrode is larger than a voltage applied to the at least one first electrode.

3. The memory cell of claim 2, wherein the voltage applied to the at least one second electrode causes a first electrostatic force in a direction towards the at least one second electrode to be applied to the moveable electrode.

4. The memory cell of claim 3, wherein the voltage applied to the at least one first electrode causes a second electrostatic force in a direction towards the at least one first electrode to be applied to the moveable electrode.

5. The memory cell of claim 4, wherein the first electrostatic force is larger than the second electrostatic force and an adhesion force between the moveable electrode and the at least one first electrode.

6. The memory cell of claim 2, wherein the moveable electrode is configured to contact the at least one second electrode when no voltage is applied to the at least one first electrode and the at least one second electrode.

7. The memory cell of claim 1, wherein the moveable electrode is configured to move from the at least one second electrode to the at least one first electrode when a voltage applied to the at least one first electrode is larger than a voltage applied to the at least one second electrode.

8. The memory cell of claim 7, wherein the voltage applied to the at least one first electrode causes a first electrostatic force in a direction towards the at least one first electrode to be applied to the moveable electrode.

9. The memory cell of claim 8, wherein the voltage applied to the at least one second electrode causes a second electrostatic force in a direction towards the at least one second electrode to be applied to the moveable electrode.

10. The memory cell of claim 9, wherein the first electrostatic force is larger than the second electrostatic force and an adhesion force between the moveable electrode and the at least one second electrode.

11. The memory cell of claim 7, wherein the moveable electrode is configured to contact the at least one first electrode when no voltage is applied to the at least one first electrode and the at least one second electrode.

12. The memory cell of claim 1, further comprising an insulator layer disposed between the at least one first electrode and the at least one second electrode.

13. The memory cell of claim 12, wherein the insulator layer, the at least one first electrode and the at least one second electrode define a cavity for guiding the movement of the moveable electrode between the at least one first electrode and the at least one second electrode.

14. The memory cell of claim 12, further comprising a further insulator layer disposed between the substrate and the at least one first electrode.

15. The memory cell of claim 1, further comprising a further gate electrode disposed above the drain electrode and the source electrode.

16. A method of manufacturing a memory cell, the method comprising:

providing a first metal layer and patterning the first metal layer to form at least one first electrode;

depositing a first sacrificial layer above the first metal layer;

depositing a second metal layer above the first sacrificial layer;

depositing a second sacrificial layer above the second metal layer;

depositing a third metal layer above the second sacrificial layer;

depositing a first sacrificial pillar structure at one side of the first sacrificial layer, the second metal layer, the second sacrificial layer and the third metal layer, and a second sacrificial pillar structure at the other side of the first sacrificial layer, the second metal layer, the second sacrificial layer and the third metal layer;

depositing a first insulator layer above the third metal layer, the first sacrificial pillar structure, the second sacrificial pillar structure and the first metal layer;

etching an opening in the first insulator layer to expose a portion of the third metal layer;

depositing a fourth metal layer above the first insulator layer and the exposed portion of the third metal layer;

etching an opening in the fourth metal layer and the third metal layer to form at least one second electrode;

removing the first sacrificial layer, the second sacrificial layer, the first sacrificial pillar structure and the second sacrificial pillar structure to form a moveable electrode and to provide a cavity for guiding movement of the moveable electrode between the at least one first electrode and the at least one second electrode;

wherein the at least one first electrode comprises a gate electrode, and wherein the at least one second electrode comprises a drain electrode and a source electrode.

17. The method of claim 16:

wherein the first metal layer is deposited above a second insulator layer; and

wherein the second insulator layer is deposited above a substrate.