CLAIMS

1. A method, comprising:

determining a desired logic state of a self-selecting memory cell comprising a chalcogenide alloy, the desired logic state representing one or more bits of data;

determining a threshold voltage of the self-selecting memory cell that corresponds to the desired logic state of the self-selecting memory cell;

determining, from a plurality of shapes of programming pulses, a shape of a programming pulse having a single polarity in order to obtain the threshold voltage of the self-selecting memory cell, wherein each shape of the plurality of shapes produces a respective profile of an asymmetric spatial distribution of at least one constituent of the chalcogenide alloy between a first side of the chalcogenide alloy and a second side of the chalcogenide alloy, and wherein the shape of the programming pulse having the single polarity is determined based at least in part on a profile of the respective profiles corresponding to the desired logic state; and

applying the programming pulse to the self-selecting memory cell based at least in part on determining the shape of the programming pulse to produce the profile of the asymmetric spatial distribution of at least one constituent of the chalcogenide alloy between the first side of the chalcogenide alloy and the second side of the chalcogenide alloy.

2. The method of claim 1, wherein determining the shape of the programming pulse comprises:

determining one or more time durations during which a fixed voltage amplitude is maintained.

3. The method of claim 1, further comprising:

varying a current level flowing through the self-selecting memory cell to cause variations of the shape of the programming pulse when the programming pulse is applied to the self-selecting memory cell.

4. The method of claim 1, wherein variations of the shape of the programming pulse produce different threshold voltages of the self-selecting memory cell.

5. The method of claim 4, wherein the variations of the shape of the programming pulse comprise a second voltage level greater than a first voltage level or a

second current level greater than a first current level based at least in part on that the second voltage level or the second current level establishes a greater threshold voltage of the self-selecting memory cell than the first voltage level or the first current level does.

6. The method of claim 1, wherein the first side of the chalcogenide alloy interfaces with a first electrode and the second side of the chalcogenide alloy interfaces with a second electrode.

7. The method of claim 1, wherein the threshold voltage of the self-selecting memory cell is set based at least in part on a local composition of the chalcogenide alloy at the first side of the chalcogenide alloy or at the second side of the chalcogenide alloy.

8. The method of claim 1, wherein the chalcogenide alloy comprises at least one of silicon (Si), selenium (Se), arsenic (As), or germanium (Ge).

9. The method of claim 1, wherein the at least one constituent of the chalcogenide alloy producing the asymmetric spatial distribution is selenium (Se).

10. The method of claim 1, further comprising:

varying the shape of the programming pulse to produce different profiles of the asymmetric spatial distribution of the at least one constituent of the chalcogenide alloy between the first side of the chalcogenide alloy and the second side of the chalcogenide alloy.

11. The method of claim 1, wherein applying the programming pulse to the self-selecting memory cell comprises:

producing a current flowing through the chalcogenide alloy;

heating the chalcogenide alloy based at least in part on producing the current flowing through the chalcogenide alloy; and

initiating a net movement of at least one constituent of the chalcogenide alloy between the first side of the chalcogenide alloy and the second side of the chalcogenide alloy based at least in part on heating the chalcogenide alloy.

12. The method of claim 11, wherein the threshold voltage of the self-selecting memory cell is set by a concentration of the at least one constituent of the chalcogenide alloy at the first side of the chalcogenide alloy or at the second side of the chalcogenide alloy.

13. The method of claim 11, wherein the threshold voltage of the self-selecting memory cell is proportional to a local concentration of the at least one constituent of the chalcogenide alloy at the first side of the chalcogenide alloy or at the second side of the chalcogenide alloy.

14. The method of claim 1, wherein the self-selecting memory cell is a part of a three-dimensional cross-point memory array comprising one or more decks of memory array and each deck of memory array is placed either on top of a substrate or another deck of memory array.

15. The method of claim 1, wherein the self-selecting memory cell is a part of a three-dimensional memory array comprising vertically-disposed first access lines crossing horizontally-disposed second access lines.

16. The method of claim 1, further comprising:

applying one or more read pulses having a single polarity;

detecting the threshold voltage of the self-selecting memory cell based at least in part on applying the one or more read pulses; and

determining a logic state of the self-selecting memory cell based at least in part on detecting the threshold voltage of the self-selecting memory cell.

17. The method of claim 16, wherein the polarity of the one or more read pulses is different from the polarity of the programming pulse.

18. A method, comprising:

determining a desired threshold voltage of a self-selecting memory cell that comprises a chalcogenide alloy, the desired threshold voltage corresponding to a logic state of the self-selecting memory cell representing one or more bits of data;

determining, from a plurality of shapes of programming pulses, a shape of a programming pulse having a single polarity producing a current flowing through the self-selecting memory cell in order to obtain the desired threshold voltage of the self-selecting memory cell, wherein each shape of the plurality of shapes produces a respective profile of a spatial distribution of at least one part of the chalcogenide alloy, and wherein the shape of the programming pulse having the single polarity is determined based at least in part on a profile of the respective profiles corresponding to the desired logic state; and

altering the spatial distribution of the at least one part of the chalcogenide alloy along a direction of the current by applying the programming pulse to the self-selecting memory cell based at least in part on determining the shape of the programming pulse, wherein the desired threshold voltage of the self-selecting memory cell is based at last in part on the spatial distribution of the at least one part of the chalcogenide alloy.

19. The method of claim 18, wherein determining the shape of the programming pulse comprises:

determining one or more time durations during which a fixed voltage amplitude is maintained to produce the current flowing through the self-selecting memory cell during each time duration.

20. The method of claim 18, wherein applying the programming pulse to the self-selecting memory cell comprises:

establishing an electric field across the chalcogenide alloy based at least in part on a fixed voltage amplitude to cause net movements of the at least one part of the chalcogenide alloy; and

heating the chalcogenide alloy based at least in part on the current flowing through the self-selecting memory cell to assist the net movements of the at least one part of the chalcogenide alloy.

21. The method of claim 18, wherein the self-selecting memory cell comprises a first interface between a first electrode in contact with a first side of the chalcogenide alloy and a second interface between a second electrode in contact with a second side of the chalcogenide alloy, the method further comprising:

setting the desired threshold voltage of the self-selecting memory cell based at least in part on a concentration of the at least one part of the chalcogenide alloy at either the first interface or the second interface.

22. The method of claim 18, further comprising:

applying one or more read pulses having the same polarity as the programming pulse; and

determining the logic state of the self-selecting memory cell based at least in part on applying the one or more read pulses that detect a threshold voltage of the self-selecting memory cell.

23. A method, comprising:

determining a threshold voltage of a self-selecting memory cell comprising a chalcogenide alloy having an interface with an electrode, the threshold voltage corresponding to a desired logic state representing one or more bits of data;

determining, from a plurality of shapes of programming pulses, a shape of a programming pulse having a single polarity based at least in part on determining the threshold voltage of the self-selecting memory cell, wherein each shape of the plurality of shapes produces a respective local concentration of at least one part of the self-selecting memory cell at the interface with the electrode, and wherein the shape of the programming pulse having the single polarity is determined based at least in part on a first local concentration of the respective local concentrations corresponding to the threshold voltage; and

altering a second local concentration of the at least one part of the self-selecting memory cell at the interface with the electrode by applying the programming pulse to the self-selecting memory cell based at least in part on determining the shape of the programming pulse to produce the first local concentration corresponding to the threshold voltage.

24. The method of claim 23, wherein the threshold voltage of the self-selecting memory cell is set based at least in part on the first local concentration of the chalcogenide alloy at the interface.

25. The method of claim 23, wherein the threshold voltage of the self-selecting memory cell is proportional to a concentration of at least one constituent of the chalcogenide alloy at the interface.

26. A memory device, comprising:

a cross-point memory array comprising a self-selecting memory cell, the self-selecting memory cell comprising a chalcogenide alloy; and

a controller coupled with the cross-point memory array, the controller being operable to:

determine a desired logic state of the self-selecting memory cell, the desired logic state representing one or more bits of data;

determine a threshold voltage of the self-selecting memory cell that corresponds to the desired logic state of the self-selecting memory cell;

determine, from a plurality of shapes of programming pulses, a shape of a programming pulse having a single polarity in order to obtain the threshold voltage of the self-selecting memory cell, wherein each shape of the plurality of shapes produces a respective profile of an asymmetric spatial distribution of at least one constituent of the chalcogenide alloy between a first side of the chalcogenide alloy and a second side of the chalcogenide alloy, and wherein the shape of the programming pulse having the single polarity is determined based at least in part on a profile of the respective profiles corresponding to the desired logic state; and

apply the programming pulse to the self-selecting memory cell based at least in part on determining the shape of the programming pulse to produce the profile of the asymmetric spatial distribution of at least one constituent of the chalcogenide alloy between the first side of the chalcogenide alloy and the second side of the chalcogenide alloy.

27. The memory device of claim 26, wherein the cross-point memory array comprises two or more decks of self-selecting memory cells each comprising the chalcogenide alloy, a first side of the chalcogenide alloy interfacing with a first electrode and a second side of the chalcogenide alloy interfacing with a second electrode.

28. The memory device of claim 26, wherein the controller is further operable to:

apply one or more read pulses having a single polarity;

detect the threshold voltage of the self-selecting memory cell based at least in part on applying the one or more read pulses; and

determine a logic state of the self-selecting memory cell based at least in part on detecting the threshold voltage of the self-selecting memory cell.

29. The memory device of claim 28, the memory device further comprising:

a periphery circuit that produces the polarity of the one or more read pulses and the polarity of the programming pulse that is different than the polarity of the one or more read pulses.