MULTI-CHIP MODULE

This invention relates generally to the field of semiconductor device manufacture and more particularly to the packaging of microchip devices with integrated circuit chips to be used in an electronic assembly, such as a printed circuit board.

In the electronics industry, the quest for smaller electronic devices which perform better at a lower cost is ongoing. This is especially true for the portable electronics and wireless communications sector which has undergone recent rapid growth. In particular, there is a strong demand for very small and light microchip packages. One possibility to reduce the package size and weight per packaged microchip is to combine two or more microchips in one and the same package. The resulting package is commonly known as a multi-chip module (MCM) or multi-chip package (MCP). The microchip components which are combined during the process of multi-chip packaging can be unpackaged microchips and/or already packed microchips, such as chip scale packages (CSP) i.e. packages having about the same size as the packaged microchips. One advantage of a MCM is that the correspondingly required space on a printed circuit board can be reduced. Furthermore, the length of electrical interconnections between the microchips inside the package can significantly be reduced. As a result, parasitic electrical effects are smaller and there is almost no delay in the transportation of high-speed electrical signals. The types of microchips which are packaged in the same MCM can be the same. However, in many applications the types are different, for example different types of memory chips or a logic controller chip combined with a memory chip.

There are different methods of producing a MCM. In stack die packaging, at least one microchip having a smaller cross-sectional area than a second microchip or packaged microchip is mounted on the surface of the second microchip or packaged microchip. A plurality of electrical conducts are used to connect the microchips with external electrical contacts. Inside the package, electrical connections are made between the microchips and/or between the electrical conducts and the microchips.

After having established the different electrical interconnections the microchips are encapsulated, for example using a resin.

In another method, the different microchips are arranged side-by-side to each other on the surface of an interposer, i.e. a separate mounting component. The interposer can be used for establishing the electrical interconnections between the microchips or between the electrical conducts and the microchips. In a known construction, the interposer carries electrically conductive tracks and contact pads, similar to a printed circuit board.

With the increasing degree of integration of integrated circuits, the number of electrical contacts of a microchips has increased significantly. As a result, there are many electrical interconnections to be established inside a MCM. Usually, very small electrically conductive wires are used for this purpose ("wire bonding"). If all the internal interconnections were to be established by wire bonding the handling would be very difficult and in many cases an electrical shortcut between two or more wires would occur due to the crossing paths of the extension of the wires.

It has therefore been proposed to avoid the crossing of wire paths using an interposer with an appropriate design of electrical paths on its surface and/or underneath its surface. However, in many cases the design of the interposer has to be adapted to the particular type of MCM. As a result, the costs of packaging are high, especially when there are many electrical interconnections to be made and the interposer comprises more than one layer with electrically conductive paths and/or so-called vias where one electrical path bypasses another electrical path. To avoid a complicated structure of the internal electrical interconnections the microchips can be re-designed. However, the costs for a re-design of microchips are usually even higher than the costs for the design of an interposer.

It is therefore desirable to reduce the costs of manufacture multi-chip modules, in particular if there are many electrical interconnections to be made within the package. Furthermore, it is desirable to manufacture a small and light MCM, at the same time.

Accordingly, the following arrangement for packaging a plurality of

microchips is provided. The arrangement comprises:

a first microchip;

at least one electrically conductive track which is mounted on the surface of the first microchip; and

an electrical conduct which is connected to the conductive track for electrical connection of the conductive track to the outside of the microchip package to be made.

The conductive track can be considered as an extension to the electrical conduct. The conduct is, for example, part of a lead frame. Preferably, the surface of the conductive track is not covered during the manufacturing of the package and the conductive track can therefore be contacted at any location along the path of the track. In particular, the track can be connected to a wire for establishing a wire bond to an electrical contact of the first microchip or another microchip.

Preferably, the track can be a self-supporting part which is fixed to the surface of the first microchip. In the mode which is currently considered as the best mode, the conductive track is fixed to the surface of the first microchip by means of an adhesive layer, such as an adhesive tape.

If the conductive track is a self-supporting part, it can be used to hold the first microchip during the manufacturing of a multi-chip module. For example, the track can be firmly connected to a lead frame which is then used to hold the conductive track and, thereby, the first microchip.

Preferably, the conductive track is flat, but has a sufficiently large cross-sectional area to transmit electrical signals without significant losses due to electrical resistance. The shape of the cross-section is, for example, similar to a track on a printed circuit board. However, it is preferred that the track width is sufficiently large so that a bonding wire can be connected to the track at any location along the track path. On the other hand, it is also possible that the track width is smaller, but that there are several contact pads electrically connected to the track and that electrical connection to the track can be made at the contact pads.

One advantage of the proposed arrangement is that the track increases the

number of locations where a bonding wire or another type of electrical connection can be connected to the track and thereby to the electrical conduct which leads to the outside of the package. This helps to avoid crossing paths of electrical connections of this type in regions where the connections are distant to the surface of the first microchip and/or other microchips. In particular, electrical shortcuts between electrical bonding wires or other electrical connection parts which are flexible can be avoided. Further, the distance between these electrical interconnections can be increased. As a result, a wider range of types of microchips can be used in MCM without the need for a re-design of the microchips. Furthermore, the length of bonding wires or of other flexible parts of the electrical interconnections can be reduced.

The present invention is particularly useful for packaging of microchips in stack die format. In this case, there is no need for an interposer with a substrate that carries parts of the electrical interconnections between the microchips or between one of the microchips and an electrical conduct leading to the outside of the package, or the package to be made. The costs for manufacturing such an interposer are comparatively high and increase the overall cost of the package. Further, the interposer must be designed especially for one type of MCM, in some cases. Moreover, a stack die package is more compact than a MCM with microchips that are arranged side-by-side to each other. Since the mounting of the conductive track to the surface of the first microchip does not significantly increase the dimensions of the first microchip, the present invention can even be used in chip scale packaging.

Although the stack die format is preferred, the present invention can also be used in combination with an interposer. In this case, the present invention may help to reduce the number of electrical paths provided by the interposer, and may in particular help to reduce the number of layers with electrical connections in the interposer and/or the number of vias in the interposer.

The conductive track on the surface of the first microchip may comprise a plurality of branches and/or at least one bifurcation. Further, more than one electrically conductive track can be mounted to the surface of the first microchip.

The track can be connected to the same and/or different electrical conducts which lead to the outside of the package.

Preferably, the conductive track at least partly embraces the outline of a surface area of the first microchip. In this area, a second microchip with a smaller base area than the first microchip can be mounted to the first microchip. If viewed from an arbitrary point inside the surface area, which possibly coincides with the location of an electrical contact of the second microchip, there is a great variety of possible electrical connections from this point to the conductive track. This means, depending on other electrical connections to be made, that an appropriate electrical connection to the conductive track can be established. It is preferred that at least one electrical contact for electrically connecting the first microchip and the surface area for mounting the second microchip are located on opposite sides of the conductive track.

The conductive track can be made of the same material as the electrical conduct leading to the outside of the package. The electrical connection between the conductive track and the electrical conduct can be established by known methods, such as soldering or welding, before or after mounting the conductive track on the surface of the first microchip.

In addition to the above-described arrangement, there is proposed a method of packaging a plurality of microchips. The method comprises:

mounting at least one electrically conductive track on the surface of the first microchip; and

electrically connecting the conductive track to an electrical conduct for connection of the conductive track to an electrical contact accessible from the outside of the package to be made.

The present invention will now be described by way of non-limitative examples only, with reference to the accompanying schematic drawings, in which:

Figure 1 illustrates the problem of crossing wire paths in stack die packaging;

Figure 2 is a plan view of an embodiment of the present invention in a top

view;

Figure 3 shows a part of the arrangement of Figure 2;

Figure 4 shows a cross-section along line IV-IV in Figure 2;

Figure 5 depicts an enlarged view of a part of Figure 4; and

Figure 6 is a plan view of an alternative embodiment of the present invention.

In the description of the drawings, the same reference numerals refer to equal and equivalent parts.

Figure 1 shows a schematic top view of the rectangular surface of a first microchip which is referred to hereinafter as the mother die 3. The first microchip can be an unpackaged microchip or a packaged microchip, for example, in chip scale format.

On the surface of the mother die 3, a plurality of chip contacts 13 are provided in order to electrically connect the mother die 3 with other microchips of a multi-chip module to be made and/or with the exterior of the module. The chip contacts 13 of the mother die 3 are arranged near the two longer edges of the rectangular surface. In practice, there are usually more than the twelve chip contacts shown. Figure 1 also shows end portions of electrical conducts 9 which are mounted on the surface of the mother die 3. On the left-hand and right-hand side of Figure 1, next to the shorter edges of the surface of the mother die 3, there is each one group of seven end portions of the conducts 9. In addition, there are each two end portions of the conducts 9 next to the longer edges of the surface of the mother die. The end portions extend in a direction which is transverse to the direction of the surface edges. From the edges, the end portions extend towards the central area of the surface of the mother die 3, but leave the bigger part of the surface free for mounting of other components. Within this area, a second microchip, which is referred to hereinafter as the daughter die 5, is mounted on the surface of the mother die 3. The daughter die 5 has a significantly smaller base area than the mother die 3. The daughter die 5 comprises seven chip contacts 13 for electrically connecting the daughter die 5 with the mother die 3 and/or with the conducts 9.

In order to illustrate the problems which might arise if arbitrary electrical connections are to be made between the conducts 9 and the chip contacts 13, Figure 1 shows a plurality of bonding wires 19. It can be seen that some of the bonding wires 19 cross other bonding wires 19 in the top view shown in Figure 1. In this arrangement, it is difficult to avoid electrical shortcuts between these bonding wires 19. Even if an electrical shortcut can be avoided during the wire bonding procedure, further manufacturing steps, in particular the encapsulation of the microchips, might lead to a shortcut. A further problem is related to the distances of the places where different wires 19 are connected with the same conduct 9 or the same chip contact 13. In the arrangement shown in Figure 1, there is very little space for such multiple connections. As a result, it is difficult to handle the wires 19 during the bonding process and, possibly, some of the connections may be faulty or non-reliable.

Figures 2 and 3 show the same arrangement as Figure 1, but with additional electrically conductive tracks 15 on the surface of the mother die 3. There are five conductive tracks 15 which are electrically connected to each one or more than one of the end portions of the conducts 9. As shown in Figure 2, the conducts 9 lead to the outside of a multi-chip module 1 where external contacts 11 are located. The external contacts 11 can be used, for example, to connect the module 1 to a printed circuit board.

The conductive tracks 15 are differently shaped. One of the tracks 15 comprises a bifurcation and is connected to the end portions of different conducts 9. Each one of the tracks 15 is connected to the end portion located at the central line of a group of seven of the conducts 9 on the right-hand and left-hand side, next to the shorter edges of the surface of the mother die 3. This pair of tracks 15 embraces the outline of the area in which the daughter die 5 is mounted on the surface of the mother die 3. Each of the tracks 15 of this pair of tracks comprises a bifurcation at a point where two branches of the respective track 15 start to extend into different directions towards opposite sides of the mounting area for the daughter die 5. The other three tracks 15 shown in Figures 2 and 3 extend within the peripheral area defined by the pair of embracing tracks 15. Each of these three tracks 15 partly

embraces the outline of the area for mounting the daughter die 5 by following a cornered path of extension along the outline of the mounting area for the daughter die 5.

Figure 2 shows a plurality of bonding wires 19 (straight, thick, solid lines). These bonding wires 19 establish, together with the conductive tracks 15, electrical interconnections between the mother die 3 and the daughter die 5 and between one of the dies 3,5 and the conducts 9. These interconnections are equivalent to the electrical interconnections shown in Figure 1. However, none of the paths of the bonding wires 19 crosses the path of another bonding wire 19 in the top view of Figure 2. Further, although plural electrical connections are made to some of the conducts 9, the tracks 15 provide larger areas for this compared to the arrangement shown in Figure 1.

In the embodiment shown in Figures 2 to 5, the conductive tracks 15 as well as the end portions of the conducts 9 are fixed to the mounting surface 4 (Figure 5) of the mother die 3 by means of adhesive layers 17, preferably adhesive tapes. As can be seen from Figure 2, there are four areas with adhesive layers 17, each one where the groups of each seven conducts 9 terminate and each one next to the longer edges of the mounting surface 4 of the mother die 3. The layered configuration of the module 1 can be seen from Figures 4 and 5 wherein Figure 5 shows an enlarged view of a part of Figure 4. The mother die 3 and the components which are mounted to the mounting surface 4 are encapsulated by an encapsulant 21, such as a resin. As can be seen from Figure 4, the electrical conducts 9 extend along a curved path to the external contacts 11 which are at about the same level as the daughter die 5. The shape of the external contacts 11 can be different compared to the shape shown in the schematic drawings of Figures 2 to 5. For example, the external contacts can terminate on the level of the lower boundaries of the module 1 in order to facilitate the mounting of the module 1 to a printed circuit board.

In an alternative embodiment, shown in Figure 6, only the conductive tracks 15 are fixed by the adhesive layers 17 to the surface of the mother die 3, but not the end portions of the conducts 9. In this embodiment, the conducts terminate outside

of the outline of the mother die. Some electrical interconnections between the mother and daughter dies and the electrical conducts can be established by wire bonding (omitted from Figure 6 for clarity). It is also possible in this embodiment that at least some of the conductive tracks are directly connected, for example by welding or soldering, to the conducts. As shown, the conductive tracks 15 are formed as extensions of respective ones of the conducts 9. However, they may also be formed separately, and may then not extend outside the outline of the mother die, with electrical connection to the respective conducts also made by wire bonding.

In a further alternative embodiment, the at least one conductive track and the corresponding electrical conduct which is used to electrically connect the conductive track to the exterior of a multi-chip module are integrally manufactured as one part, i.e. without the need for connecting two separate parts during the manufacturing of the multi-chip module. In one variant of this embodiment, the conduct is part of a lead frame with a plurality of conducts and some of the conducts are extended by the conductive tracks in order to facilitate the electrical interconnections inside the multi-chip module in the same manner as described above. In particular, the conductive tracks can have the same features as the tracks 15 shown in Figures 2 to 5. The lead frame can be fabricated by etching or stamping and can be made of any suitable metal such as copper or "alloy 42" (a nickel-iron controlled-expansion alloy containing 42% nickel). The lead frame may have a thickness in the range of from 0.10mm t0 0.25mm.

REFERENCE NUMERALS

1	multi-chip module
3	mother die
4	mounting surface
5	daughter die
7	lead frame
9	conduct
11	external contact
13	chip contact
15	conductive track
17	adhesive tape
19	wire
21	encapsulant

CLAIMS

1. An arrangement for packaging a plurality of microchips (3,5) comprising:

a first microchip (3);

at least one electrically conductive track (15) which is mounted on the surface (4) of the first microchip (3); and

an electrical conduct (9) which is connected to the conductive track (15) for electrical connection of the conductive track (15) to the outside of the package of the microchips (3,5) to be made.

2. An arrangement according to claim 1, wherein the conductive track (15) is fixed to the surface (4) of the first microchip (3) by means of an adhesive layer (17).

3. An arrangement according to claim 1 or 2, wherein the conductive track (15) at least partly embraces the outline of a surface area of the first microchip (3) where a second microchip (5) with a smaller base area than the first microchip (3) can be mounted to the first microchip (3).

4. An arrangement according to one of claims 1 to 3, wherein at least one electrical contact (13) for electrically connecting the first microchip (3) and a surface area for mounting the second microchip (5) are located on opposite sides of the conductive track (15).

5. An arrangement according to one of claims 1 to 4, wherein a second microchip (5) is mounted on the surface of the first microchip (3) and wherein electrical contacts (13) of the first and second microchips (3,5) are electrically connected to the same conductive track (15) by means of electrical connections (19).

6. An arrangement according to any one of claims 1 to 5 wherein said electrical conduct (9) comprises a lead of a lead frame which extends farther than other leads

of said lead frame to form said electrically conductive track (15).

7. A multi-chip module (1) which comprises an arrangement according to one of claims 1 to 6, wherein a second micro-chip (5) is mounted on the surface of the first microchip (3) and wherein an electrical connection from at least one of the microchips (3,5) is made via the conductive track (15) and via the electrical conduct (9) to an electrical contact (11) which can be electrically contacted from outside of the module.

8. A method of packaging a plurality of microchips, the method comprising:

mounting at least one electrically conductive track (15) on the surface of a first microchip (3); and

electrically connecting the conductive track (15) to an electrical conduct (9) for connection of the conductive track (15) to an electrical contact (11) accessible from the outside of the package to be made.

9. A method according to claim 8, wherein the first microchip (3) and/or a second microchip (5) are/is electrically connected to the conductive track (15) by wire bonding.