ABSTRACT

A METHOD TO PRODUCE DUAL GATES (ONE METAL AND ONE POLY OR METAL SILICIDE) FOR CMOS DEVICES USING SPUTTERED METAL DEPOSITION, METALLIC ION IMPLANTATION, OR SILICON IMPLANTATION, AND LASER ANNEALING

A method of fabricating first and second gates comprising the following steps. A substrate having a gate dielectric layer formed thereover is provided. The substrate having a first gate region and a second gate region. A thin first gate layer is formed over the gate dielectric layer. The thin first gate layer within the second gate region is masked to expose a portion of the thin first gate layer within the first gate region. The exposed portion of the thin first gate layer is converted to a thin third gate layer portion. A second gate layer is formed over the thin first and third gate layer portions. The second gate layer and the first and third gate layer portions are patterned to form a first gate within first gate region and a second gate within second gate region.

FIGURE 5