It is known to manufacture embedded DRAMs based on wafers with a pre-doped n-layer formed in the handle substrates, directly underneath the BOX and rather thick to contain the entire DRAM capacitor trench, typically several microns. For example, a phosphorous n^+ layer with a concentration of 10^{19} cm^{-3} may serve as a capacitor bottom plate. The n^+ layer is crucial in terms of scaling of the eDRAMs. However, there arises a problem when a logic part comprising back-biased planar fully or partially depleted SOI transistors shall be integrated together with embedded DRAMs, since the pre-doped n^+ layer heavily hampers the manufacture of the back-biasing features. Back bias regions must be electrically insulated one from another in order for them to be biased at different voltages without high leakage current. To achieve that insulation, we will need reverse-biased junctions on the current path from one back bias region to another. We will typically have N and P layers on top of the handle substrate creating the need junctions, and cut then vertically by STI structures to insulate one region from the others.

Such multilayer structure can potentially be manufactured starting with the thick N+ layer required for the eDRAM, but would require high implantation doses to be implanted through the SOI and BOX layers. This is not desirable because it might create defects and also dope the SOI layer.

In view of this, embodiments of~~it is a problem underlying~~ the present invention seek to provide a method for the integrated manufacture of both embedded DRAMS and back-biased transistors.

Description of the Invention

According to an aspect of the present invention, there~~In order to address the above-mentioned problem, it~~ is provided a method for the manufacture of a semiconductor device~~wafer~~, comprising the steps of

growing~~providing (e.g., forming)~~ a doped layer on a semiconductor substrate;

growing an intrinsic~~providing (e.g., forming) a~~ first semiconductor layer on the doped layer;

providing ~~(e.g., forming)~~ a buried oxide layer on the intrinsic first semiconductor layer; ~~and~~

providing ~~(e.g., forming)~~ a second semiconductor layer on the buried oxide layer~~.~~;

forming an embedded DRAM device in a first region of the wafer; and

forming a back-biased transistor in a second region of the wafer that is different from the first region;

and wherein

forming the back-biased transistor comprises forming a back-biasing region in the intrinsic first semiconductor layer by doping at least a part of the intrinsic first semiconductor layer of the already provided wafer with n or p dopants.

There is also disclosed~~The above-mentioned problem is also solved by the herein provided~~ wafer comprising

a semiconductor substrate;

a doped layer formed on the semiconductor substrate;

a first semiconductor layer formed on the semiconductor substrate;

a buried oxide layer formed on the first semiconductor layer; and

a second semiconductor layer formed on the buried oxide layer.

The thus provided wafer may facilitates the manufacture of an embedded DRAM integrated together with a logic part comprising SOI transistors that are back-biased for control of the threshold voltage. Contrary to the art there is no need for any complicated processing of a conventional wafer for preparation for the formation of back-biasing regions required by the provision of the heavily doped embedded doped layer. Rather, the provision of the first (intrinsic) semiconductor layer may allows for easy conversion into n or p doped back-biasing regions for the SOI transistors of the logic part enabling a first level of Vt tuning by changing the back bias region doping between N or P.

According to particular examples, the substrate is made of or comprises (poly- or mono) silicon. Both the first and the second semiconductor layer may comprise or consist of silicon. The buried oxide layer may comprise an SiO_2 compound. The doped layer may, for example, be n^+ doped silicon, for example, silicon comprising phosphorus dopants. The concentration of such phosphorus dopants may be in the range of some 10^{18} to 10^{20} cm^{-3}, in particular, about 10^{19} cm^{-3}.

As far as the thicknesses of the individual layers of the provided wafer concerns the following choices are, for example, suitable: The thickness of the first semiconductor layer may be in the range of 10 to 300 nm, in particular, 50 to 150 nm. The thickness of the second semiconductor layer may be in the range of 5 to 100 nm, in particular, 5 to 20 nm. An extra thin second semiconductor layer (5 to 15 nm) may be provided, if a fully depleted SOI transistor shall be formed in a logic part of the wafer. A somewhat thicker second semiconductor layer (up to some 100 nm) may be provided, if a partially depleted SOI transistor shall be formed in a logic part of the wafer. The thickness of the buried oxide layer may be in the range of 5 to 200 nm, in particular, 5 to 25 nm and the thickness of the doped layer may be in the range of 1 to 10 µm.

According to an example,~~embodiment~~ the wafer may be manufactured on the basis of some wafer transfer process, for instance, a wafer transfer process comprising the Smart Cut© process. The doped layer and the first semiconductor layer may be grown on the semiconductor substrate and the second semiconductor layer may be grown on a donor substrate and the wafer may be obtained by bonding the first and the second semiconductor layers by the buried oxide layer and detaching the donor substrate.

In some detail, the manufacture of the wafer according to an example comprises the steps of growing the epitaxial doped layer on the semiconductor substrate and growing the first semiconductor epitaxial layer on the doped layer. The above-mentioned step of forming the second semiconductor layer on the buried oxide layer may comprise growing the second semiconductor layer on a donor substrate to obtain a donor wafer; forming a first oxide layer on the second semiconductor layer grown on the donor substrate; and/or forming a second oxide layer on the epitaxial first semiconductor layer grown on the doped layer; and bonding the donor wafer to the epitaxial first semiconductor layer grown on the doped layer by the first and/or second intermediate buried layer, wherein the first and/or second oxide layer form the buried oxide layer, and detaching the donor substrate (see also detailed description below). In such a manner the desired wafer can reliably be formed avoiding significant defects of the semiconductor layers.

5. The method according to claim 4, wherein forming the second semiconductor layer on the buried oxide layer comprises

growing the second semiconductor layer on a donor substrate to obtain a donor wafer;

forming a first intermediate oxide layer on the second semiconductor layer grown on the donor substrate;

forming a second intermediate oxide layer on the epitaxial intrinsic first semiconductor layer grown on the doped layer;

bonding the donor wafer to the intrinsic first semiconductor layer grown on the doped layer by the first and second intermediate oxide layers, wherein the first and second intermediate oxide layers form the buried oxide layer, and

detaching the donor substrate.

6. The method for the manufacture of a semiconductor device according to claim 1, wherein