CLAIMS:

1. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; at least one of the first and second electrodes having an electrochemically active surface directly against the ion conductive material; the second electrode being elevationally outward of the first electrode; and

the first electrode extending laterally in a first direction, the ion conductive material extending laterally in a second direction different from and intersecting the first direction, the first electrode being directly against the ion conductive material only where the first and second directions intersect.

2. The integrated circuit of claim 1 wherein the second electrode has an electrochemically active surface directly against the ion conductive material.

3. The integrated circuit of claim 1 wherein the first electrode has an electrochemically active surface directly against the ion conductive material.

4. The integrated circuit of claim 1 wherein the second electrode has a lateral outermost sidewall and the ion conductive material has a transverse outermost sidewall directly against the second electrode lateral outermost sidewall.

5. The integrated circuit of claim 4 wherein the lateral outermost sidewall and the transverse outermost sidewall are vertically oriented.

6. The integrated circuit of claim 1 wherein the ion conductive material comprises an elevationally outermost surface, the second electrode being directly against the elevationally outermost surface of the ion conductive material.

7. The integrated circuit of claim 1 wherein at least one of the first electrode and the ion conductive material has a transverse thickness where received directly against the other of the first electrode or ion conductive material which is less than F, where F is a minimum feature dimension of lithographically-defined features.

8. The integrated circuit of claim 1 wherein each of the first electrode and the ion conductive material has a transverse thickness where received directly against the other of the first electrode or ion conductive material which is less than F, where F is a minimum feature dimension of lithographically-defined features.

9. The integrated circuit of claim 1 wherein the first and second directions intersect at an angle from about 45° to 90°.

10. The integrated circuit of claim 9 wherein the first and second directions intersect at an angle from 80° to 90°.

11. The integrated circuit of claim 1 wherein each of the first electrode and the ion conductive material is platelike.

12. The integrated circuit of claim 1 wherein each of the first electrode and the ion conductive material is platelike and are intersecting at about 90°.

13. The integrated circuit of claim 1 comprising a plurality of said nonvolatile memory cells within a memory array.

14. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first platelike electrode, a second platelike electrode, and a platelike ion conductive material between the first and second platelike electrodes; at least one of the first and second platelike electrodes having an electrochemically active surface directly against the platelike ion conductive material; the second platelike electrode being elevationally outward of the first platelike electrode; and

each of the first platelike electrode, the second platelike electrode, and the platelike ion conductive material being oriented perpendicularly relative each other.

15. The integrated circuit of claim 14 wherein the second platelike electrode comprises an electrochemically active surface directly against the platelike ion conductive material.

16, The integrated circuit of claim 14 wherein the second platelike electrode comprises an electrochemically active material having an electrochemically active surface directly against the platelike ion conductive material, the electrochemically active material of the second platelike electrode having an elevationally outermost surface that is not received against the platelike ion conductive material.

17. The integrated circuit of claim 16 wherein the ion conductive material has an elevationally outermost surface which is elevationally outward of the elevationally outermost surface of the electrochemically active material of the second platelike electrode.

18. The integrated circuit of claim 14 wherein the platelike ion conductive material comprises an elevationally outermost surface, the platelike second electrode being directly against the elevationally outermost surface of the platelike ion conductive material.

19. The integrated circuit of claim 14 wherein each of the first platelike electrode and platelike ion conductive material is of a respective uniform transverse thickness.

20. The integrated circuit of claim 14 wherein each of the first platelike electrode and the platelike ion conductive material are of a respective uniform transverse thickness which is less than F, where F is a minimum feature dimension of lithographically-defined features.

21. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; at least the second electrode comprising an electrochemically active material having a surface directly against the ion conductive material; the second electrode being elevationally outward of the first electrode; and

the electrochemically active material having an elevationally outermost surface, the ion conductive material having an elevationally outermost surface which is elevationally outward of the elevationally outermost surface of the electrochemically active material.

22. The integrated circuit of claim 21 wherein the second electrode comprises an electrochemically inactive material received elevationally outward of the second electrode electrochemically active material, the electrochemically inactive material comprising an elevationally outermost surface which is elevationally coincident with the elevationally outermost surface of the ion conductive material.

23. The integrated circuit of claim 21 wherein the first electrode extends laterally in a first direction, the ion conductive material extends laterally in a second direction different from and intersecting the first direction, the first electrode being directly against the ion conductive material only where the first and second directions intersect.

24. The integrated circuit of claim 21 wherein each of the first electrode, the second electrode, and the ion conductive material is platelike.

25. The integrated circuit of claim 24 wherein each of the platelike first electrode, the platelike second electrode, and the platelike ion conductive material is oriented perpendicularly relative each other.

26. The integrated circuit of claim 21 wherein the second electrode has a lateral outermost sidewall and the ion conductive material has a transverse outermost sidewall directly against the second electrode lateral outermost sidewall.

27. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; at least one of the first and second electrodes having an electrochemically active surface directly against the ion conductive material; the second electrode being elevationally outward of the first electrode and having a lateral outermost sidewall; and

the ion conductive material comprising a transverse outermost sidewall directly against the second electrode lateral outermost sidewall.

28. The integrated circuit of claim 27 wherein each of the first electrode, the second electrode, and the ion conductive material is platelike.

29. The integrated circuit of claim 28 wherein each of the platelike first electrode, the platelike second electrode, and the platelike ion conductive material is oriented perpendicularly relative each other.

30. The integrated circuit of claim 27 wherein the lateral outermost sidewall and the transverse outermost sidewall are vertically oriented.

31. A method of forming a nonvolatile memory cell, comprising:

forming first and second electrodes, at least one of the first and second electrodes having an electrochemically active surface; and

after forming the first and second electrodes, depositing an ion conductive material directly against the electrochemically active surface.

32. The method of claim 31 comprising providing a dielectric between the first and second electrodes, the dielectric having a lateral sidewall, the ion conductive material being deposited directly against the dielectric lateral sidewall.

33. The method of claim 31 wherein the second electrode is elevationally outward of the first electrode, the second electrode has a lateral outermost surface, and the ion conductive material is deposited directly against the lateral outermost surface of the second electrode.

34. The method of claim 33 wherein the lateral outermost surface of the second electrode is an electrochemically active surface directly against which the ion conductive material is deposited.

35. The method of claim 31 wherein the second electrode is elevationally outward of the first electrode, the first electrode comprises a platelike structure, and the ion conductive material is deposited directly against an edge surface of the platelike structure of the first electrode.

36. The method of claim 35 wherein the edge surface is electrochemically inactive.

37. A method of forming a nonvolatile memory cell, comprising:

forming a first sidewall;

forming a first current conductive electrode material over the first sidewall;

forming a second sidewall elevationally outward of the first current conductive material, the first and second sidewalls being formed at an angle relative one another;

forming an ion conductive material over the second sidewall and directly against an elevationally outer surface of the first current conductive material, the ion conductive material and the first current conductive material contacting one another at a maximum contacting area defined by a transverse thickness of the ion conductive material and a transverse thickness of the first current conductive electrode where such cross at said angle; and

providing a second current conductive electrode directly against the ion conductive material, at least one of the first current conductive electrode and the second current conductive electrode having an electrochemically active surface directly against the ion conductive material.

38. The method of claim 37 wherein the angle from about 45° to 90°.

39. The method of claim 38 wherein the angle from 80° to 90°.

40. The method of claim 37 wherein the first sidewall is vertically oriented.

41. The method of claim 37 wherein the second sidewall is vertically oriented.

42. The method of claim 37 wherein the first and second sidewalls are vertically oriented.

43. The method of claim 37 comprising forming the ion conductive material after forming the second current conductive electrode.

44. The method of claim 37 comprising forming the ion conductive material before forming the second current conductive electrode.

45. The method of claim 37 comprising providing a transverse sidewall of the ion conductive material directly against a lateral sidewall of the second electrode.

46. The method of claim 37 comprising forming the ion conductive material to a transverse thickness where such cross which is less than F, where F is a minimum feature dimension of lithographically-defined features.

47. The method of claim 37 comprising forming the first current conductive electrode to a transverse thickness where such cross which is less than F, where F is a minimum feature dimension of lithographically-defined features.

48. The method of claim 37 comprising forming the first current conductive electrode and the ion conductive material to respective transverse thicknesses where such cross which are less than F, where F is a minimum feature dimension of lithographically-defined features.

The invention claimed is:

1. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; the second electrode having an electrochemically active surface directly against the ion conductive material and an electrochemically inactive surface directly against the ion conductive material; the second electrode being elevationally outward of the first electrode;

the first electrode extending laterally in a first direction, the ion conductive material extending laterally in a second direction different from and intersecting the first direction, the first electrode being directly against the ion conductive material only where the first and second directions intersect, the second electrode having a lateral outermost sidewall and the ion conductive material having a transverse outermost sidewall directly against the second electrode lateral outermost sidewall, the second electrode being directly against the ion conductive material only at the transverse outermost sidewall of the ion conductive material; and

the first electrode being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the first electrode, the first platelike electrode having an elevationally outermost surface; the ion conductive material being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the ion conductive material, the platelike ion conductive material having an elevationally innermost surface that is directly against the elevationally outermost surface of the first platelike electrode; the first platelike electrode and the platelike ion conductive material intersecting at an angle relative one another.

2. The integrated circuit of claim 1 wherein the lateral outermost sidewall and the transverse outermost sidewall are vertically oriented.

3. The integrated circuit of claim 1 wherein at least one of the first electrode and the ion conductive material has its thinnest transverse thickness where received directly against the other of the first electrode or ion conductive material which is less than F, where F is a minimum feature dimension of lithographically-defined features.

4. The integrated circuit of claim 1 wherein each of the first electrode and the ion conductive material has its thinnest transverse thickness where received directly against the other of the first electrode or ion conductive material which is less than F, where F is a minimum feature dimension of lithographically-defined features.

5. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; the second electrode having an electrochemically active surface directly against the ion conductive material and an electrochemically inactive surface directly against the ion conductive material; the second electrode being elevationally outward of the first

electrode; the first electrode extending laterally in a first direction, the ion conductive material extending laterally in a second direction different from and intersecting the first direction, the first electrode being directly against the ion conductive material only where the first and second directions intersect, the first and second directions intersecting at an angle from 45^0 to less than 90^0; and

the first electrode being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the first electrode, the first platelike electrode having an elevationally outermost surface; the ion conductive material being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the ion conductive material, the platelike ion conductive material having an elevationally innermost surface that is directly against the elevationally outermost surface of the first platelike electrode.

6. The integrated circuit of claim 1 wherein the second electrode is platelike.

7. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first electrode, a second electrode, and an ion conductive material between the first and second electrodes; the second electrode having an electrochemically active surface directly against the ion conductive material and an electrochemically inactive surface directly against the ion conductive material; the second electrode being elevationally outward of the first electrode;

the first electrode extending laterally in a first direction, the ion conductive material extending laterally in a second direction different from and intersecting the first direction, the first electrode being directly against the ion conductive material only where the first and second directions intersect, each of the first electrode and the ion conductive material being platelike and intersecting at an angle other than 90^0; and

the first electrode being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the first electrode, the first platelike electrode having an elevationally outermost surface; the ion conductive material being platelike and having an elevational thickness which is greater than thinnest transverse thickness of the ion conductive material, the platelike ion conductive material having an elevationally innermost surface that is directly against the elevationally outermost surface of the first platelike electrode.

8. The integrated circuit of claim 1 comprising a plurality of said nonvolatile memory cells within a memory array.

9. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first platelike electrode, a second platelike electrode, and a platelike ion conductive material between the first and second platelike electrodes; the second platelike electrode having an electrochemically active surface directly against the platelike ion conductive material and an electrochemically inactive surface directly against the ion conductive

material; the second platelike electrode being elevationally outward of the first platelike electrode; and

the first platelike electrode having an elevational thickness which is greater than thinnest transverse thickness of the first electrode, the first platelike electrode having an elevationally outermost surface; the platelike ion conductive material having an elevational thickness which is greater than thinnest transverse thickness of the ion conductive material, the platelike ion conductive material having an elevationally innermost surface that is directly against the elevationally outermost surface of the first platelike electrode; the first platelike electrode and the platelike ion conductive material intersecting at an angle relative one another.

10. An integrated circuit comprising a nonvolatile memory cell, the nonvolatile memory cell comprising:

a first platelike electrode, a second platelike electrode, and a platelike ion conductive material between the first and second platelike electrodes; the second platelike electrode having an electrochemically active surface directly against the platelike ion conductive material and an electrochemically inactive surface directly against the ion conductive material; the second platelike electrode being elevationally outward of the first platelike electrode;

the platelike ion conductive material being oriented perpendicularly relative to the first platelike electrode, the second platelike electrode being oriented perpendicularly relative to the plate like ion conductive material, the second platelike electrode being oriented perpendicularly relative to the first platelike electrode;

the first platelike electrode having an elevational thickness which is greater than thinnest transverse thickness of the first electrode, the first platelike electrode having an elevationally outermost surface; the platelike ion conductive material having an elevational thickness which is greater than thinnest transverse thickness of the ion conductive material, the platelike ion conductive material having an elevationally innermost surface that is directly against the elevationally outermost surface of the first platelike electrode;

the second platelike electrode comprising an electrochemically active material having an elevationally outermost surface that is not received against the platelike ion conductive material; and

the ion conductive material having an elevationally outermost surface which is elevationally outward of the elevationally outermost surface of the electrochemically active material of the second platelike electrode.

11. The integrated circuit of claim 9 wherein each of the first platelike electrode and platelike ion conductive material is of a respective uniform transverse thickness.

12. The integrated circuit of claim 9 wherein each of the first platelike electrode and the platelike ion conductive material are of a respective uniform transverse thickness which is less than F, where F is a minimum feature dimension of lithographically-defined features.

13. The integrated circuit of claim 9 wherein the elevationally outermost surface of the first platelike electrode has a minimum cross dimension equal to the thinnest transverse thickness of the first platelike electrode.

14. The integrated circuit of claim 9 wherein the elevationally innermost surface of the ion conductive material has a minimum cross dimension equal to the thinnest transverse thickness of the ion conductive material.

15. The integrated circuit of claim 9 wherein,

the elevationally outermost surface of the first platelike electrode has a minimum cross dimension equal to the thinnest transverse thickness of the first platelike electrode; and

the elevationally innermost surface of the ion conductive material has a minimum cross dimension equal to the thinnest transverse thickness of the ion conductive material.