(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 September 2004 (02.09.2004)

PCT

(10) International Publication Number
WO 2004/075265 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number:
PCT/US2004/005818

(22) International Filing Date: 17 February 2004 (17.02.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/448,096 18 February 2003 (18.02.2003) US

(71) Applicant *(for all designated States except US)*: **UNITIVE ELECTRONICS, INC.** [US/US]; 140 South Center Court, Suite 600, Morrisville, North Carolina 27560 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **JAN, Jong-Rong** [CN/CN]; No. 176, Fu-Xing Rd., Bei-Bu Village, Hsin-Cheng Hsiang, Hualian Hsien, 971 (TW). **LU, Tsai-Hua** [CN/CN]; No. 5, Lane 210, Lin-Sen Rd., Hisn-Chu City, 300 (TW). **CHIU, Sao-Ling** [CN/CN]; 15, ALY 16, LN 576,, Kuang-Fu Rd., Sec. 1, Hisn-Chu City, 300 (TW). **KUNG, Ling-Chen** [CN/CN]; 5F, No. 241, Guandung Rd, Hisn-Chu City, 300 (TW).

(74) Agent: **MYERS BIGEL SIBLEY & SAJOVEC, P.A.**; P.O. Box 37428, Raleigh, North Carolina 27627 (US).

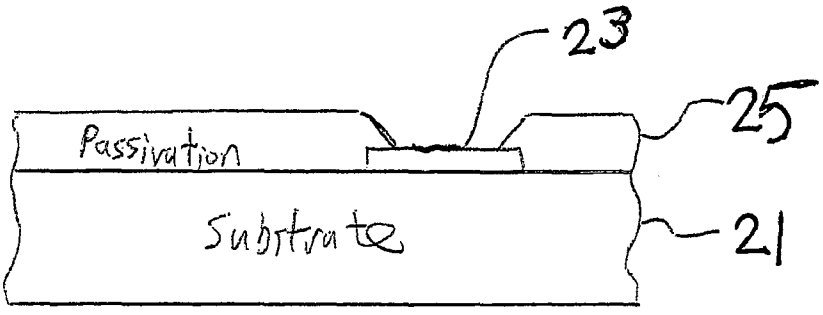
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS FOR SELECTIVELY BUMPING INTEGRATED CIRCUIT SUBSTRATES AND RELATED STRUCTURES



(57) Abstract: Bumping a substrate having a metal layer thereon may include forming a barrier layer on the substrate including the metal layer and forming a conductive bump on the barrier layer. Moreover, the barrier layer may be between the conductive bump and the substrate, and the conductive bump may be laterally offset from the metal layer. After forming the conductive bump, the barrier layer may be removed from the metal layer thereby exposing the metal layer while maintaining a portion of the barrier layer between the conductive bump and the substrate. Related structures are also discussed.

WO 2004/075265 A2