CLAIMS

1. A semiconductor field-effect transistor (FET) device, comprising: at least one gate disposed on a substrate;

source and drains on opposite sides of the at least one gate, wherein at least one of the source and drains has a sloped surface;

a surface dopant-semiconductor alloy contact layer disposed on the at least one of the source and drains but along only the sloped surface;

a buried power rail embedded in the substrate; and

a buried contact that connects the buried power rail to the sloped surface of the at least one source and drain.

2. The semiconductor FET device of claim 1, further comprising:

sidewall spacers alongside the buried power rail that separate the buried power rail from the substrate, wherein the sidewall spacers also separate the buried contact from the substrate.

3. The semiconductor FET device of claim 2, wherein the sidewall spacers comprise a material selected from the group consisting of: silicon carbide (SiC), silicon oxycarbide (SiOC), and combinations thereof.

4. The semiconductor FET device of claim 1, wherein a top of the sloped surface of the at least one source and drain is above a top surface of the buried contact.

5. The semiconductor FET device of claim 1, wherein the buried power rail comprises a metal selected from the group consisting of: copper (Cu), cobalt (Co), ruthenium (Ru), tungsten (W), and combinations thereof.

6. The semiconductor FET device of claim 1, wherein the sloped surface of the at least one source and drain is sloped at an angle θ of from about 95º to about 150º and ranges therebetween.

7. The semiconductor FET device of claim 1, further comprising:

a trench epitaxial layer disposed on the sloped surface.

8. The semiconductor FET device of claim 1, wherein the buried contact comprises a metal selected from the group consisting of: Cu, Co, Ru, W, and combinations thereof.

9. The semiconductor FET device of claim 1, further comprising:

a bottom dielectric layer separating the source and drains from the substrate.

10. The semiconductor FET device of claim 1, further comprising: at least one active layer interconnecting the

source and drains.

11. A semiconductor FET device , comprising:

at least one gate disposed on a substrate;

source and drains on opposite sides of the at least one gate, wherein at least one of the source and drains has a sloped surface;

a surface dopant-semiconductor alloy contact layer disposed on the at least one of the source and drains but along only the sloped surface;

a buried power rail embedded in the substrate below the sloped surface;

sidewall spacers separating the buried power rail from the substrate; and

a buried contact that connects the buried power rail to the sloped surface of the at least one source and drain, wherein a top of the sloped surface of the at least one source and drain is above a top surface of the buried contact.

12. The semiconductor FET device of claim 11, wherein the sloped surface of the at least one source and drain is sloped at an angle θ of from about 95° to about 150° and ranges therebetween.

13. The semiconductor FET device of claim 11, further comprising:
a trench epitaxial layer disposed on the sloped surface.

14. The semiconductor FET device of claim 11, further comprising:
a bottom dielectric layer separating the source and drains from the substrate.

15. The semiconductor FET device of claim 11, further comprising:
at least one active layer interconnecting the source and drains.

16. The semiconductor FET device of claim 15, further comprising:
multiple vertically stacked active layers interconnecting the source and drains.

17. A method of forming a semiconductor FET device, the method comprising the steps of:

forming a device structure comprising at least one gate disposed on a substrate, source

and drains on opposite sides of the at least one gate, and a buried power rail embedded in the substrate;

etching at least one of the source and drain to produce a sloped surface along a portion of the at least one source and drain; and

forming a buried contact that connects the buried power rail to the sloped surface of the at least one source and drain, wherein a top of the sloped surface of the at least one source and drain is above a top surface of the buried contact.

18. The method of claim 17, further comprising the step of:

growing a trench epitaxy layer on the sloped surface of the at least one source and drain.

19. The method of claim 17, further comprising the step of:

performing epitaxial re-growth to form a surface dopant-semiconductor alloy contact layer on the sloped surface.

20. A method of forming a semiconductor FET device, the method comprising the steps of:

forming a device structure comprising at least one gate disposed on a substrate, source and drains on opposite sides of the at least one gate, an interlayer dielectric (ILD) surrounding the at least one gate, and a buried power rail embedded in the substrate;

patterning a contact trench in the ILD to expose at least one of the source and drains;

etching that at least one source and drain to produce a sloped surface along a portion of the at least one source and drain exposed in the contact trench;

performing epitaxial re-growth to form a surface dopant-semiconductor alloy contact layer on the sloped surface; and

forming a buried contact in the contact trench that connects the buried power rail to the sloped surface of the at least one source and drain, wherein a top of the sloped surface of the at least one source and drain is above a top surface of the buried contact.

21. The method of claim 20, further comprising the step of:

growing a trench epitaxy layer on the sloped surface of the at least one source and drain.