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(54) CHARGE STORAGE TARGET AND DEVICE

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to charge storage targets of the type having an array of diodes and to devices having such a charge storage target scanned by a reading means.

One type of charge storage device is the vidicon camera tube. A vidicon has an evacuated envelope of which one end is a transparent faceplate. On the inside surface of the faceplate is first a transparent conductive signal plate, and on that signal plate is a charge storage target. Inside the other end of the envelope is an electron gun for forming an electron beam to be directed toward the target. In one type of vidicon, electrostatic deflection means are included in the tube for causing the beam to scan a raster on that target surface facing the gun.

Among the types of targets that are used in vidicons are photodiode array targets. Generally, such targets include a semiconductor wafer with bulk region of one conductivity type and having an array of discrete regions of another conductivity type on one of its major surfaces. The discrete regions form PN junctions with the bulk region of the wafer. The bulk region surface separating the discrete regions is covered completely with an insulating layer.

One problem with previous targets is that the beam does not land properly on the discrete regions. Charge accumulating on the

surface of the insulating layer tends to repel the beam from that surface. When the discrete regions are very small, the amount of insulator surface compared to the amount of discrete region surface that is exposed to the beam is relatively large. As a result, a significant portion of the beam is prevented from landing on the discrete regions by the charge on the insulating layer immediately surrounding the discrete region. To improve the beam landing, separate round metal pads are placed over and in electrical contact with the surface of the discrete regions and overlapping the insulating layer surrounding the discrete regions. The pads increase the amount of landing area for the discrete regions and decrease the amount of exposed insulating area, to result in improved beam landing. Such pads have the disadvantage that when any part of them contacts the bulk region there is a direct short circuit between the bulk region and the beam. Such short circuit shows in the picture from the target as a bright spot blemish. Contact to the bulk region occurs, for instance, when there is misregistration of the openings in the insulating layer with the discrete regions, or when the metal contacts the bulk region through a fault in the insulating layer, such as a pinhole. Moreover, the evaporation method of forming metal pads results in a relatively high percentage of inoperative diodes, since frequently a formed pad fails to make direct contact to a clean portion of the discrete region surface.

During diffusion to make the discrete regions, a thin insulator coating forms on the discrete region surface. It is necessary to remove this coating before putting the pads on the discrete regions. Removal of the coating results in considerable undercutting of the



insulating layer on the bulk region surface. Thus there is a greater likelihood that the bulk region might be exposed and contacted by a pad to create a short circuit.

5 According to the present invention there is provided a charge storage target comprising a wafer of semiconductor material of a first conductivity type having on a major surface thereof an array of effectively discrete regions of a second conductivity type forming individual diodes with said wafer, and electrically insulating layer covering said major surface between said discrete regions and further semiconductor material on said insulating material and in contact with said discrete regions, said further semiconductor material containing a dopant suitable to cause the material of said wafer to be of said second conductivity type.

20 The semiconductor pads improve the contact of the reading means to the discrete areas and can be used as the diffusion source for the discrete regions. In addition, contact of a pad to the bulk region, such as may result from misregistration of discrete regions with openings in the insulating layer or from entry of the pad material into a pinhole in the insulating layer, does not result in a short circuit there. Instead, it results in the formation of a separate PN junction at the place of contact, since there will be a diffusing into the bulk region there. This separate PN junction does not affect the performance quality of the target, as it is unnoticeable in the target signal. Since the diffusion is from the pads, no insulating coating forms on the discrete regions. Thus, the step of removing such a coating before putting pads on the discrete regions is entirely eliminated to result in an improved target.

Reference is now made to the accompanying drawings in which:—

45 FIGURE 1 is a side sectional view of an improved vidicon camera tube utilizing the invention;

FIGURE 2 is a fragmentary sectional view of the target in the tube of FIGURE 1;

50 FIGURE 3 is a view of a fragment of the scanned surface of the target of FIGURE 2;

FIGURE 4 is a fragmentary side sectional view of another embodiment of the target, and

55 FIGURE 5 is a fragmentary side sectional view of yet another embodiment of the target;

FIGURE 6 is a view of a fragment of the scanned surface of the target of FIGURE 2 with a solid state scanning system shown schematically and connected to the target.

60 A preferred embodiment of the invention is a vidicon type camera tube 10 as shown in FIGURE 1, having an evacuated envelope 12, a transparent faceplate 14 at one end of the envelope 12, an electron gun 16 inside the envelope for forming an electron beam, and a

target 18 adjacent the inside surface of the faceplate 14. Means (not shown) for directing the beam toward the target 18 and for causing the beam to scan the target 18 surface may be disposed inside the envelope 12.

70 The target 18, a fragment of which is shown in FIGURE 2, is a silicon photodiode target. It is conveniently formed with a round single crystal of silicon about 1.0 inch in diameter and about 20 microns thick. The bulk region 20 of the wafer is doped N type with phosphorus to a level within the range of 2×10^{13} atoms/cm³ to 10^{16} atoms/cm³ thus yielding a conductivity range of 0.5 to 200 ohm-centimeters.

80 On one major surface of the wafer is an array of P type discrete regions 22. The discrete regions are spaced at about 25.4 microns from center to center, are about 7 microns across and extend about 3 microns into the wafer. Each discrete region 22 forms a PN junction photodiode with the N type bulk region 20 of the wafer. The dopant in the discrete regions 22 is boron.

90 Covering the surface of the N type bulk region 20 which separates the P type discrete regions 22 is an insulating layer 24 of silicon dioxide to a thickness within the range of 0.4 to 1.5 microns.

95 Covering the surface of each P type discrete region 22 and overlapping the edge of the insulating layer 24 is a polycrystalline pad 26 of degenerately doped silicon about 0.6 microns thick. The dopant in the pads is boron, whose concentration is in the order of 10^{19} atoms per cubic centimeter. The resistivity of the pads 26 is of the order of 30 Ω -cm.

105 The target 18 may be fabricated by the following process: First a silicon dioxide insulating layer 24 about 0.8 microns thick is grown on one major surface of a 127 microns thick very high purity silicon wafer by heating the wafer for about one hour at about 1100°C in an atmosphere of steam. Using well known photoresist techniques, an array of openings about 7 microns in diameter with a spacing of about 25.4 microns from center to center is etched through the insulating layer 24 to expose discrete areas of the wafer surface. A layer of silicon about 0.6 micron thick heavily doped with boron is then vapor phase deposited on the exposed discrete areas and on the insulating layer 24. The layer of silicon is then etched, using photoresist techniques, to form pads 26 in the openings and overlapping to some extent the adjacent insulating layer 24. The pads 26 do not contact each other. The pads are generally square-shaped, measuring about 17 microns on a side. The wafer is then baked in a dry furnace at about 1200°C for about 5 minutes, slowly cooled to about 750°C over a period of about 2 hours, and then cooled to room temperature. During the baking some of the dopant in the pads 26

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diffuses into the wafer and forms P type discrete regions 22 therein. These discrete regions 22 form PN junctions with the N type bulk regions 20 and extend into the wafer a distance of about 3 microns. The non-diffused face of the wafer is then etched chemically until the wafer thickness is about 20 microns. A thicker region may be retained around the periphery for structural support.

The non-diffused side of the target 18 is placed adjacent the inside surface of the faceplate 14 with the opposite side, that having the pads 26, toward the scanning means 16.

When the target 18 is operated in the vidicon 10, the N type bulk region 20 is normally biased at a potential "v" a few volts positive in relation to the cathode potential of the gun 16. The scanning beam impinges in turn on each pad 26. Beam electrons are conducted through the pads 26 to the P type region 22. Addition of electrons to the discrete region 22 puts the PN junction there in a state of back-bias, allowing the charge to accumulate until the discrete region 22 and the pad 26 reach cathode potential and repel the beam. In the dark, a relatively good diode can retain most of the charge in its discrete region 22 for a considerable time. However, if light is absorbed in the N type bulk region 20, charge carriers are formed there which migrate of the PN junction and result in leakage of charge from the discrete region 22. When the beam next scans the pad 26 of the discharged discrete region 22, it brings the discrete region quickly back to cathode potential. The sudden fluctuation of potential in the discrete region 22 results by capacitive coupling in a corresponding current fluctuation in the N type bulk region 20. The N type bulk region 20 is sufficiently conductive to serve as a signal plate for the target 18, and the current fluctuations in it may be transferred through an electrical contact 28 to conventional video signal processing equipment (not shown).

Although after diffusion the pads 26 have a doping level of the order of 10^{19} atoms/cm³ and a resistivity of the order of 30 ohm-centimetres, a somewhat higher resistivity than metals, their action in conducting the beam electrons to the P type regions 22 is quite adequate for normal video frame rates. The beam is a high enough impedance source that such pad 26 resistance is relatively immaterial.

While the preferred embodiment of the invention is a vidicon camera tube, the invention encompasses other types of charge storage devices which have a charge storage target addressed by a reading means. Such devices may be, for example, storage tubes, scan conversion tubes, or solid state image sensors. For instance, in use in the secondary emission mode, the conductivity type of the discrete regions 22 and the bulk region 20 are re-

versed, so that the discrete regions 22 are made N type whereas the bulk region 20 is P type. The scanned side of the target 18 is brought to the potential of the accelerating mesh of the gun 16 by secondary emission.

The novel target 18 may be comprised of a monocrystalline wafer of silicon as in the preferred embodiment, of a polycrystalline wafer of silicon, or of a single of polycrystalline wafer of another semiconductor such as germanium, gallium arsenide, or gallium arsenide phosphide. The diodes may be of the mesa type or any other type. The pads 26 need not necessarily be of the same semiconductor material as the bulk region 20 so long as they are doped semiconductor material of relatively low resistance. The pad 26 material should itself be a material or contain a material that is a conductivity modifier capable of altering the conductivity type of the wafer material to form discrete regions and, therewith, PN junctions. Such conductivity modifiers may be, for example, elements of Group III and V of the Periodic Table in the case of silicon or germanium and elements of the Group II, IV and VI in the case of Groups III-V compounds such as gallium arsenide. Such conductivity modifiers may also be diffused through pads 26 which were formed on the target 18 in an undoped state.

For optimum sensitivity of the target 18 it is desirable that the wafer thickness be on the order of the average carrier diffusion length in the wafer. This assures that enough of the light-generated carriers will be able to reach one of the discrete regions 22. For best response to short wavelengths such as blue and for good resolution, the wafer should be made as thin as possible. In operation, the field-free region of the wafer should preferably be minimized by applying voltages to the wafer which bring the depletion region almost to the lighted target 18 surface. In this condition, light-generated carriers in the field free region will be more likely to reach the depletion region. Once they reach the depletion region they are very likely under the influence of the relatively strong field there to reach the discrete regions. Trapping of carriers at the lighted surface can be minimized by the formation of an accumulation region there to drive the carriers away from the surface. The accumulation region can be formed by a shallow diffusion of N type impurities on the lighted surface.

The pads 26 of the preferred embodiment are of a generally square shape in order that the ratio of pad 26 surface to insulting layer 24 surface exposed to the beam be a maximum while at the same time there be sufficient insulting layer 24 surface to prevent leakage between pads 26. The pads 26 could, of course, be any of a variety of shapes.

The pads 26 need not be electrically isolated

from one another to perform their function. Moreover, they may be monocrystalline, polycrystalline, amorphous, or a combination thereof. They may be provided in the form of a single, amorphous, doped contact layer forming discrete but electrically joined pads 26 on the beam side of the target 18 as is shown in FIGURE 4. The contact layer may be of uniform thickness or may be thinned where it lies upon the insulating layer 24, as shown in FIGURE 5, for example, by etching. The layer would serve as the diffusion source for the discrete regions 22. Even a uniformly thick contact layer may function according to the present invention. The contact layer thickness may be chosen to give a lateral resistance great enough so that there is no appreciable surface current between one effectively discrete region 22 and another one near it. Yet at the same time, the resistance through the small thickness of the contact layer can be relatively low, allowing each pad 26 to act in a rather independent fashion.

The insulating layer 24 separating the bulk region 20 surface from the beam may be made of any of a number of insulating materials, such as for instance glass, that are suitable as an insulating coating under the conditions required for fabrication of the target and for operation of the tube 10. For the case of a silicon wafer, we prefer to use silicon dioxide because of its refractory properties and the relative ease with which it may be formed.

The lighted side of the target may be supplied with anti-reflective, transparent coatings to improve the optical coupling between the target and any associated optics such as the faceplate of the vidicon 10. It may also be provided with an N⁺ type accumulation region to reduce surface recombination at the lighted surface.

In a vidicon, the reading of the target is accomplished by contacting the individual target elements, such as the diodes in an array, with an electron beam. When a target has discrete elements, such as in a diode array, however, the function of the electron beam may be performed by contacting each element with an electrical conductor and then scanning the conductors with solid state circuitry. FIGURE 6 shows a fragment of the scanned surface of a target 30 of the same general structure as the target of FIGURE 3 but whose pads 32 are connected by the conductors 34 to a solid state scan generator 36 shown schematically. The scan generator 36 successively connects each pad to a reference potential "v" which may be the same potential to which the beam in a vidicon brings the pads. Aside from the manner in which the pads are returned to a reference potential, the operation of a vidicon and the solid state device of Figure 4 are substantially the same.

Each of the embodiments may be operated

with voltages, currents and frequencies normally used for devices of the particular type. In this respect the targets are compatible with existing structures and do not require special treatment for successful operation.

WHAT WE CLAIM IS:—

1. A charge storage target comprising a wafer of semiconductor material of a first conductivity type having on a major surface thereof an array of effectively discrete regions of a second conductivity type forming individual diodes with said wafer, an electrically insulating layer covering said major surface between said discrete regions and further semiconductor material on said insulating material and in contact with said discrete regions, said further semiconductor material containing a dopant suitable to cause the material of said wafer to be of said second conductivity type.

2. A charge storage target in accordance with claim 1 wherein said wafer is of N-type silicon.

3. A charge storage target in accordance with claim 2 wherein said wafer has a conductivity within the range of 0.5 to 200 ohm-centimetres.

4. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material is in the form of discrete pads each in contact with a said discrete region.

5. A charge storage target in accordance with claim 4 wherein said pads are generally square in shape.

6. A charge storage target in accordance with claim 1, claim 2 or claim 3 wherein said further semiconductor material comprises a continuous layer of material overlying said insulating material and said discrete regions.

7. A charge storage target in accordance with claim 6 wherein said continuous layer of material is of uniform thickness.

8. A charge storage target in accordance with claim 6 wherein said continuous layer of material is thinned in the regions of said insulating material.

9. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material and said discrete regions contain the same dopant.

10. A charge storage target in accordance with claim 2 or in accordance with any one of claims 3 to 9 as dependent upon claim 2, wherein said further semiconductor material contains a dopant which causes silicon to have P-type conductivity.

11. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material is doped to degeneracy.

12. A charge storage target substantially as described with reference to the accompanying drawings.

from one another to perform their function. Moreover, they may be monocrystalline, polycrystalline, amorphous, or a combination thereof. They may be provided in the form of a single, amorphous, doped contact layer forming discrete but electrically joined pads 26 on the beam side of the target 18 as is shown in FIGURE 4. The contact layer may be of uniform thickness or may be thinned where it lies upon the insulating layer 24, as shown in FIGURE 5, for example, by etching. The layer would serve as the diffusion source for the discrete regions 22. Even a uniformly thick contact layer may function according to the present invention. The contact layer thickness may be chosen to give a lateral resistance great enough so that there is no appreciable surface current between one effectively discrete region 22 and another one near it. Yet at the same time, the resistance through the small thickness of the contact layer can be relatively low, allowing each pad 26 to act in a rather independent fashion.

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2. A charge storage target in accordance with claim 1 wherein said wafer is of N-type silicon.

3. A charge storage target in accordance with claim 2 wherein said wafer has a conductivity within the range of 0.5 to 200 ohm-centimetres.

4. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material is in the form of discrete pads each in contact with a said discrete region.

5. A charge storage target in accordance with claim 4 wherein said pads are generally square in shape.

6. A charge storage target in accordance with claim 1, claim 2 or claim 3 wherein said further semiconductor material comprises a continuous layer of material overlying said insulating material and said discrete regions.

7. A charge storage target in accordance with claim 6 wherein said continuous layer of material is of uniform thickness.

8. A charge storage target in accordance with claim 6 wherein said continuous layer of material is thinned in the regions of said insulating material.

9. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material and said discrete regions contain the same dopant.

10. A charge storage target in accordance with claim 2 or in accordance with any one of claims 3 to 9 as dependent upon claim 2, wherein said further semiconductor material contains a dopant which causes silicon to have P-type conductivity.

11. A charge storage target in accordance with any one of the preceding claims wherein said further semiconductor material is doped to degeneracy.

12. A charge storage target substantially as described with reference to the accompanying drawings.



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- 5 13. A charge storage device including a charge storage target in accordance with any one of the preceding claims and reading means for selectively bringing the individual discrete regions to a predetermined potential. 10 substantially as described with reference to the accompanying drawings.
14. A charge storage device substantially as described with reference to the accompanying drawings.
15. An electron beam charge storage device

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