What is Claimed is:

1. A semiconductor package comprising:

a package substrate;

an interposer mounted on the package substrate;

a first semiconductor chip mounted on the interposer;

a plurality of second semiconductor chips mounted on the interposer to surround at least a portion of the first semiconductor chip;

a heat radiation member arranged on the first semiconductor chip and the plurality of second semiconductor chips; and

a heat blocking member extending from a portion of the heat radiation member and arranged in at least one space among a first space between the first semiconductor chip and at least one of the plurality of second semiconductor chips and a second space between at least two of the plurality of second semiconductor chips,

a lower surface of the heat blocking member is spaced apart from an upper surface of the interposer in a vertical direction.

2. The semiconductor package of claim 1, wherein a material of the heat blocking member has a thermal conductivity that is lower than a thermal conductivity of a material of the heat radiation member.

3. The semiconductor package of claim 1, wherein a material of the heat blocking member is identical to a material of the heat radiation member, and

the heat blocking member is integrated with the heat radiation member.

4. The semiconductor package of any one of claims 1 to 3, wherein the heat blocking member comprises a heat blocking wall extending from a portion of the heat radiation member in the vertical direction and arranged in the first space between the first semiconductor chip and the at least one of the plurality of second semiconductor chips.

5. The semiconductor package of any one of claims 1 to 3, wherein the heat blocking member comprises a heat blocking wall extending from a portion of the heat radiation member in the vertical direction and arranged in the second space between the at least two of the plurality of second semiconductor chips.

6. The semiconductor package of claim 5, wherein a surface toward the first semiconductor chip among surfaces of the heat blocking wall is coplanar with a surface toward the first semiconductor chip among surfaces of the plurality of second semiconductor chips.

7. The semiconductor package of any one of claims 1 to 3, wherein the heat blocking member comprises:

a first heat blocking wall extending from a first portion of the heat radiation member in the vertical direction and arranged in the first space between the first semiconductor chip and the at least one of the plurality of second semiconductor chips; and

a second heat blocking wall extending from a second portion of the heat radiation member in the vertical direction and arranged in the second space between the at least two of the plurality of second semiconductor chips.

8. The semiconductor package of any one of claims 1 to 3, wherein the heat blocking member comprises:

a first heat blocking wall extending from a portion of the heat radiation member in the vertical direction and arranged in the first space between the first semiconductor chip and at least one of the plurality of second semiconductor chips;

a second heat blocking wall extending from the first heat blocking wall and arranged in the second space between the at least two of the plurality of second semiconductor chips; and

a third heat blocking wall arranged outside the plurality of second semiconductor chips, surrounding the first semiconductor chip and the plurality of second semiconductor chips, and connecting the first heat blocking wall to the second heat blocking wall.

9. The semiconductor package of any one of claims 1 to 8, wherein, when the semiconductor package is seen in a planar view, the heat blocking member has a quadrangular shape that surrounds a side portion of the first semiconductor chip.

10. The semiconductor package of any one of claims 1 to 9, wherein the heat blocking member comprises:

a plurality of first protrusions protruding in a direction toward the first semiconductor chip; and

a plurality of second protrusions protruding in a direction toward at least one of the plurality of second semiconductor chips.

11. The semiconductor package of any one of claims 1 to 10, wherein a thickness of the heat blocking member is 50 micrometers to 500 micrometers.

12. A semiconductor package comprising:

a package substrate;

an interposer mounted on the package substrate;

a first semiconductor chip mounted on the interposer;

a plurality of semiconductor stack structures mounted on the interposer to surround at least a portion of the first semiconductor chip, and comprising a plurality of semiconductor chips stacked in a vertical direction;

a heat radiation member arranged on the first semiconductor chip and the plurality of semiconductor stack structures, the heat radiation member comprising:

a first heat radiation wall extending on the first semiconductor chip and the plurality of semiconductor stack structures in a horizontal direction; and

at least one second heat radiation wall extending from a portion of the first heat radiation wall in the vertical direction and surrounding the first semiconductor chip and the plurality of semiconductor stack structures; and

a heat blocking member extending from a portion of the heat radiation member and arranged in at least one space among a first space between the first semiconductor chip and at least one of the plurality of semiconductor stack structures and a second space between at least two of the plurality of semiconductor stack structures,

wherein a lower surface of the heat blocking member is spaced apart from an upper surface of the interposer in the vertical direction.

13. The semiconductor package of claim 12, wherein

the at least one second heat radiation wall is a plurality of second heat radiation walls that extend from respective portions of the first heat radiation wall in the vertical direction, and

the heat blocking member comprises:

a first heat blocking wall extending between at least two of the plurality of second heat radiation walls, that face each other, and arranged in the first space between the first semiconductor chip and the at least two of the plurality of semiconductor stack structures; and

a second heat blocking wall extending from a portion of one of the plurality of second heat radiation walls and arranged in the second space between the at least two of the plurality of semiconductor stack structures.

14. The semiconductor package of claim 13, wherein a thickness of the first heat blocking wall is greater than a thickness of the second heat blocking wall.

15. The semiconductor package of any one of claims 12 to 14, wherein a material of the heat blocking member has a thermal conductivity that is lower than a thermal conductivity of a material of the heat radiation member.

16. The semiconductor package of claim 15, wherein the material of the heat radiation member comprises copper, and

the material of the heat blocking member comprises stainless steel.

17. The semiconductor package of any one of claims 12 to 16, wherein the interposer comprises:

an interposer substrate mounted on the package substrate;

an interposer through electrode passing through at least a portion of the interposer substrate in the vertical direction;

an interposer connection terminal connected to the interposer through electrode and arranged between the interposer substrate and the package substrate; and

a redistribution structure arranged on the interposer substrate and comprising: a redistribution insulating layer; and a redistribution pattern extending within the redistribution insulating layer and connected to the interposer through electrode.

18. A semiconductor package comprising:

a package substrate;

an interposer mounted on the package substrate and comprising:

an interposer substrate;

an interposer through electrode passing through at least a portion of the interposer substrate in a vertical direction;

an interposer connection terminal connected to the interposer through electrode and arranged between the interposer substrate and the package substrate; and

a redistribution structure arranged on the interposer substrate;

a logic semiconductor chip arranged on the redistribution structure of the interposer;

a plurality of semiconductor stack structures arranged on the redistribution structure of the interposer to surround at least a portion of the logic semiconductor chip, and comprising a plurality of memory semiconductor chips stacked in the vertical direction;

a heat radiation member arranged on the logic semiconductor chip and the plurality of semiconductor stack structures; and

a heat blocking member extending from at least a portion of the heat radiation member and arranged in at least one space among a first space between the logic semiconductor chip and at least one of the plurality of semiconductor stack structures and a second space between at least two of the plurality of semiconductor stack structures,

wherein a lower surface of the heat blocking member is spaced apart from an upper surface of the interposer in the vertical direction.