MULTI-STATE MEMORY CELL WITH ASYMMETRIC CHARGE TRAPPING

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to memory cells and in particular the present invention relates to multi-state non-volatile memory cells.

BACKGROUND OF THE INVENTION

[0002] Memory devices are available in a variety of styles and sizes. Some memory devices are volatile in nature and cannot retain data without an active power supply. A typical volatile memory is a DRAM which includes memory cells formed as capacitors. A charge, or lack of charge, on the capacitors indicate a binary state of data stored in the memory cell. Dynamic memory devices require more effort to retain data than non-volatile memories, but are typically faster to read and write.

[0003] Non-volatile memory devices are also available in different configurations. For example, floating gate memory devices are non-volatile memories that use floating gate transistors to store data. The data is written to the memory cells by changing a threshold voltage of the transistor and is retained when the power is removed. The transistors can be erased to restore the threshold voltage of the transistor. The memory may be arranged in erase blocks where all of the memory cells in an erase block are erased at one time. These non-volatile memory devices are commonly referred to as flash memories.

[0004] Flash memories may use floating gate technology or trapping technology. Floating gate cells include source and drain regions that are laterally spaced apart to form an intermediate channel region. The source and drain regions are formed in a common horizontal plane of a silicon substrate. The floating gate, typically made of doped polysilicon, is disposed over the channel region and is electrically isolated from the other cell elements by oxide. The non-volatile memory function for the floating gate technology is created by the absence or presence of charge stored on the isolated floating gate. The trapping technology functions as a non-volatile memory by the absence or presence of charge stored in isolated traps that capture and store electrons or holes.

[0005] In order for memory manufacturers to remain competitive, memory designers are constantly trying to increase the density of flash memory devices. Increasing the density of a flash memory device generally requires reducing spacing between memory cells and/or

making memory cells smaller. Smaller dimensions of many device elements may cause operational problems with the cell. For example, the channel between the source/drain regions becomes shorter possibly causing severe short channel effects. Additionally, possible charge migration from one corner of the cell to the other becomes more of a concern with smaller cell size.

[0006] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for higher density memory devices.

SUMMARY

[0007] The above-mentioned problems with memory density and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0008] The present invention encompasses a multi-state NAND memory structure. The structure comprises a substrate comprising a first conductive material. First and second active areas are formed within the substrate. The first and second active areas are made up of a second conductive material. In one embodiment, the first conductive material is a p-type material and the second conductive material is an n-type material.

[0009] A control gate is located above and between the first and second active areas. A trapping layer is located between the control gate and the substrate. The trapping layer is isolated from the control gate by a first dielectric layer and from the substrate by a second dielectric layer. The trapping layer is capable of asymmetrical charge trapping in response to asymmetrical biasing of the first and second active areas. This permits storage of a first data bit adjacent to the first active area and a second data bit adjacent to the second active area.

[0010] Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 shows a cut away view of one embodiment for programming a multi-state NAND memory cell with asymmetric charge trapping of the present invention.

[0012] Figure 2 shows a cut away view of another embodiment for programming a multi-state NAND memory cell with asymmetric charge trapping of the present invention.

[0013] Figure 3 shows a cut-away view of an embodiment for erasing a multi-state NAND memory cell with asymmetric charge trapping of the present invention.

[0014] Figure 4 shows a cut-away view of yet another embodiment of a multi-state NAND memory cell with asymmetric charge trapping of the present invention.

[0015] Figure 5 shows a cut-away view of an embodiment for reading the multi-state NAND memory cell with asymmetric charge trapping of the present invention.

[0016] Figure 6 shows a portion of a multi-state NAND memory cell array of the present invention.

[0017] Figure 7 shows a table of voltages for operation of the embodiment of Figure 6.

[0018] Figure 8 shows a block diagram of one embodiment of an electronic system of the present invention.

DETAILED DESCRIPTION

[0019] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer or substrate, used in the following description, include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions. The following

detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0020] The charge on a floating gate memory forms a Gaussian surface that spreads across the floating gate. The charge in a trapping based memory of the present invention is localized and does not spread. This property permits asymmetric charge and the ability to form multi-state cells.

[0021] Figure 1 illustrates a cut-away view of one embodiment for programming a multi-state NAND memory cell with asymmetric charge trapping. This embodiment is comprised of a substrate 101 with two active areas 105 and 107. Each region 105 and 107 acts alternatively as a drain or source region, depending on the operation performed and voltages that are applied.

[0022] In one embodiment, the drain and source regions 105 and 107 are n-type conductive material while the substrate 101 is a p-type conductive material. In an alternate embodiment, these conductive material types are switched.

[0023] Above the channel between the drain/source regions 105 and 107 is an oxide – nitride – oxide (ONO) structure 103, 109, and 111. The nitride layer 103 is isolated from the substrate by a first oxide layer 111 and from a control gate 100 by a second oxide layer 109. The nitride layer 103 is the trapping layer that stores the asymmetric charges of the present invention. The present invention is not limited to any certain quantity of dielectric and/or trapping layers.

[0024] The present invention is also not limited in the composition of the dielectric/trapping layers. In one embodiment, the oxide material can be aluminum oxide. The trapping layer may be a silicon nanocrystal material. Alternate embodiments use other types of dielectric materials and/or other trapping layer materials.

[0025] The embodiment of Figure 1 illustrates the programming of one data bit in the left side of the trapping layer 103. This is accomplished by applying a relatively high negative voltage to the control gate 100. This voltage turns off the channel in order to prevent leakage from the drain region 105 to the source region 107. In one embodiment, the gate voltage is between –10V and –15V. Alternate embodiments may use other gate voltage ranges.

[0026] An asymmetric bias is applied to the drain 105 and source regions 107. In one embodiment, a positive 5V is applied to the drain region 105 and the source region 107 is

grounded (i.e., 0V). The large potential on the left side of the junction from both the gate 100 and junction field causes a gate induced drain leakage (GIDL) condition that injects holes into the trapping layer 103 near the left junction. The injected holes neutralize the electrons from a previous erased condition thus resulting in a reduced threshold voltage.

[0027] The right junction has a reduced field since the junction bias is zero. This results in a bias condition that does not inject holes. The electrons on the right side of the channel are not compensated by holes thus resulting in the initial programmed or erased condition remaining.

[0028] Figure 2 illustrates a cut-away view of a second embodiment for programming a multi-state NAND memory cell with asymmetric charge trapping. The embodiment of Figure 2 illustrates the programming of one data bit in the right side of the trapping layer 103. This is accomplished by applying a relatively high negative voltage to the control gate 100. This voltage turns off the channel in order to prevent leakage from the drain region 107 to the source region 105. In one embodiment, the gate voltage is between –10V and –15V. Alternate embodiments may use other gate voltage ranges.

[0029] An asymmetric bias is applied to the drain 107 and source regions 105. In one embodiment, a positive 5V is applied to the drain region 107 and the source region 105 is grounded (i.e., 0V). The large potential on the right side of the junction from both the gate 100 and junction field causes a GIDL condition that injects holes into the trapping layer 103 near the right junction. The injected holes neutralize the electrons from a previous erased condition thus resulting in a reduced threshold voltage.

[0030] The left junction has a reduced field since the junction bias is zero. This results in a bias condition that does not inject holes. The electrons on the left side of the channel are not compensated by holes thus resulting in the above-described programmed condition remaining.

[0031] Figure 3 illustrates a cut-away view of an embodiment for erasing a multi-state NAND memory cell with asymmetric charge trapping. The erase operation is performed by tunneling electrons into the trapping layer 303 from a uniform sheet of charge in the inversion region 301. This forms a high threshold level by a continuous uniform sheet of trapped charge in the trapping layer 103. The erase operation is accomplished in one embodiment by applying a positive gate voltage in the range of 10 – 20V. Both the drain and

source regions are grounded (i.e., 0V). Alternate embodiments may use other voltages and voltage ranges.

[0032] Figure 4 illustrates a cut-away view of yet another embodiment of a multi-state NAND memory cell with asymmetric charge trapping. This embodiment creates a discontinuous trapping layer 403 by extending the control gate into the trapping layer 403. This results in better sensing, better data retention, and resistance to secondary emissions.

[0033] Figure 5 illustrates a method for reading the left side of the multi-state NAND memory cell of the present invention using asymmetrical biasing of the source/drain regions. The left data bit 500 can be read by applying a relatively high bias to the right source/drain region 501 of the cell. In one embodiment, this drain voltage is in the range of 1 – 3V. The left drain/source region 503, acting as a source, is grounded and V_G is a positive voltage in the range of 3 – 6V. Alternate embodiments may use other voltages and voltage ranges.

[0034] The right data bit 502 is read using an inverse process. In this embodiment, the left drain/source region 503 is grounded while the right source/drain region 501 has a relatively high voltage applied (e.g., 1 – 3V). V_G in this read embodiment is also in the range of 3 – 6V. Alternate embodiments may use other voltages and voltage ranges.

[0035] Figure 6 illustrates two string arrays of multi-state NAND memory cells of the present invention. A table of voltages for different modes of operation of a selected column of this memory array is illustrated in Figure 7.

[0036] The portion of the NAND memory array of Figure 6 is comprised of two columns 601 and 602 of multi-state NAND memory cells as described above. One column 601 is selected while the second column 602 is unselected. The selected column 601 is comprised of a select gate 605 for the drain voltage, V_d, and a select gate 606 for the source voltage V_s. The selected column 601 is also comprised of three multi-state NAND memory cells 610 – 612 that are connected to control gate voltages V_{WL1} – V_{WL3} respectively. The columns of Figure 6 are for purposes of illustration only since a real memory column is comprised of a substantially larger quantity of cells.

[0037] Referring to the voltage table of Figure 7, two versions of an erase operation are illustrated. In one option, as described above, the drain and source voltages, V_d and V_s, are 0V and the control gate voltage, V_H, are in the range of 10 – 20V. In this embodiment, the

control gates of the select gates 605 and 606 are connected to $V_H/2$. Other erase operation embodiments may use GIDL hole injection from both sides of the array simultaneously.

[0038] The second option for an erase operation leaves the drain and source connections floating as an open connection (O/C). In this embodiment, the select gates 605 and 606 are also floating.

[0039] During a program operation of the left bit in the middle cell 611, V_{WL2} is $-V_H$ (e.g., -10 to -20V), V_d is V_{DP} (e.g., 3 to 6V), and V_S is connected to ground. The control gates of the select gates 605 and 606 are connected to V_{X1} and the control gates of the other cells 610 and 612 in the column 601 are connected to V_{X2}. In one embodiment V_{X1} is approximately equal to V_{X2} which is approximately equal to $V_{DP} + V_T$. V_T is the threshold voltage of the cell as is well known in the art. The program operation of the right bit in the middle cell 611 uses substantially the same voltages as the left bit but in this case V_S is connected to V_{DP} and V_d is connected to ground. Alternate embodiments use other embodiments to achieve substantially similar results.

[0040] During a read operation of the left bit in the middle cell 611, V_{WL2} is V_R (e.g., 3 – 6 V), V_d is V_{DR}, and V_S is connected to ground. The control gates of the select gates 605 and 606 are connected to V_{Y1} and the control gates of the other cells 610 and 612 in the column 601 are connected to V_{Y2}. In one embodiment, V_{Y1} is approximately equal to V_{Y2} which is approximately equal to $V_{DR} + V_T$ where V_{DR} in the range of 4 – 6V. The read operation of the right bit in the middle cell 611 uses substantially the same voltages as the left bit but in this case V_S is connected to ground and V_d is connected to V_{DR}. Alternate embodiments use other embodiments to achieve substantially similar results.

[0041] Figure 8 illustrates a functional block diagram of a memory device 800 that can incorporate multi-state NAND memory cells of the present invention. The memory device 800 is coupled to a processor 810. The processor 810 may be a microprocessor or some other type of controlling circuitry. The memory device 800 and the processor 810 form part of an electronic system 820. The memory device 800 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

[0042] The memory device includes an array of memory cells 830. In one embodiment, the memory cells are non-volatile floating-gate memory cells and the memory array 830 is arranged in banks of rows and columns.

[0043] An address buffer circuit 840 is provided to latch address signals provided on address input connections A0-Ax 842. Address signals are received and decoded by a row decoder 844 and a column decoder 846 to access the memory array 830. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 830. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

[0044] The memory device 800 reads data in the memory array 830 by sensing voltage or current changes in the memory array columns using sense/buffer circuitry 850. The sense/buffer circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 830. Data input and output buffer circuitry 860 is included for bi-directional data communication over a plurality of data connections 862 with the controller 810). Write circuitry 855 is provided to write data to the memory array.

[0045] Control circuitry 870 decodes signals provided on control connections 872 from the processor 810. These signals are used to control the operations on the memory array 830, including data read, data write, and erase operations. The control circuitry 870 may be a state machine, a sequencer, or some other type of controller.

[0046] The flash memory device illustrated in Figure 8 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

CONCLUSION

[0047] In summary, the multi-state NAND cell of the present invention is a trapping based memory that allows asymmetric charges to be stored, thereby providing storage for two data bits. The memory cell provides high memory density, low power operation, and improved reliability due to the trapping function.

[0048] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is

manifestly intended that this invention be limited only by the following claims and equivalents thereof.

CLAIMS

1. A memory array comprising:

a plurality of multi-state NAND memory cells arranged in a column, each cell comprising a drain region, a source region, and a nitride trapping layer that is capable of asymmetrical charge trapping, in response to asymmetrical biasing of the drain and source regions, of a first data bit adjacent the drain region and a second data bit adjacent the source region; and

a plurality of select gates, a first select gate at one end of the column and a second select gate at the remaining end of the column, wherein during a programming operation of a first multi-state NAND memory cell a voltage differential substantially equal to 20V between a control gate of the first cell and the source region and a voltage differential substantially equal to 25V between the control gate and the drain region when the first data bit is being programmed and a voltage differential substantially equal to 20V between the control gate and the drain region and a voltage differential substantially equal to 25V between the control gate and the source region when the second data bit is being programmed.

2. The memory array of claim 1 wherein the source voltage is substantially equal to 0V and the drain voltage is substantially equal to 5V when the first data bit is being programmed and the drain voltage is substantially equal to 0V and the source voltage is substantially equal to 5V when the second data bit is being programmed.

3. The memory array of claim 1 wherein a voltage substantially equal to -20V is applied to the control gate of the first multi-state NAND memory cell.

4. An electronic system comprising:

a processor that controls operation of the system; and

a NAND flash memory device having a plurality of memory cells, each memory cell comprising:

a substrate comprising a first conductive material;

first and second active areas within the substrate, the first and second active areas comprised of a second conductive material;

a control gate above and between the first and second active areas; and

a trapping layer between the control gate and the substrate such that the trapping layer is capable of asymmetrical charge trapping, in response to asymmetrical biasing of the first and second active areas, of a first data bit adjacent the first active area and a second data bit adjacent the second active area wherein during a programming operation of a first memory cell a voltage differential substantially equal to 20V between the control gate of the first cell and the second active area and a voltage differential substantially equal to 25V between the control gate and the first active area when the first data bit is being programmed and a voltage differential substantially equal to 20V between the control gate and the first active area and a voltage differential substantially equal to 25V between the control gate and the second active area when the second data bit is being programmed.