

ABSTRACT

A semiconductor device includes a cell array region, a connection region including first and second regions, a stacking structure including a gate stacking structure and an insulation stacking structure, a channel structure passing through the gate stacking structure, and gate contacts in the second region and electrically connected to at least a part of the gate electrodes in the first region. The gate stacking structure includes gate electrodes and interlayer insulation layers. The insulation stacking structure includes sacrificial insulation layers and the interlayer insulation layers. Each gate contacts includes a conductive portion and a side insulation layer. The conductive portion includes a penetration part and a connection part extending horizontally to have an area greater than an area of the penetration part. The penetration part of a first contact of the gate contacts includes first and second portions on respective first and second surfaces of the connection part.

FIG. 1